Design of Rectifier Power Supplies for Thermal Energy Storage System

by

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Examining Committee:

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

ABSTRACT

Energy storage systems have been brought to focus as means to reduce the high fluctuation in the production side and facilitate integration of renewable energy sources. This work is focused on investigating design and utilizing of cost-effective Thermal Energy Storage System (TESS) which has longer life-time as an alternative to Battery Energy Storage System. Both thermal and electrical design aspects are investigated in this work. For thermal part; detailed analysis of electrical properties of the heating element (i.e. graphite) is conducted to design the heating element used to heat up the storage material (i.e. molten salt). For electrical part; asymmetric and symmetric power electronic rectifier are investigated and compared with low frequency modulation and pulse width modulation techniques, based on their power factor (PF) and total harmonic distortion (THD). Finally, direct output voltage control and cascaded current voltage control are implemented and compared.

Keywords: Thermal Energy Storage (TESS), Battery Energy Storage system (BESS), Asymmetric converter, Symmetric converter

STATEMENT OF CONTRIBUTIONS

Part of the work described in the thesis has been published as:

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Finally, I cannot forget to mention the inspiration I got from Allah (God) and my final appreciation is to those who I may have failed to mention.

DEDICATION

This thesis is dedicated to my mother and sisters (Asmat Sharif, Raheela Sipra and Rumma Sami), without their continuous love and inspiration it would not have been possible to complete this work. I would also like to dedicate this work to my late father (Arshad Ramzan), whose teachings during my upbringing taught me never to give up and work hard.

ABBREVIATIONS

AC	Alternating Current
AR	Argon (element)
BESS	Battery Energy Storage System
CM	Common Mode
CDS	Contract for Deferral Scheme
SCM	Cascaded Multilevel Converters
degs.	Degrees
DC	Direct Current
DPC	Direct Power Control
Fig.	Figure
HCC	Hysteresis Current Control
IGBT	Insulated-Gate Bipolar Transistor
IC	Integrated Circuit
LPF	Low Pass Filter
MV	Multi-Voltage
pu	Per Unit
PCM	Phase Change Material
PLL	Phase Lock Loop
PV	Photovoltaic
PCC	Point of Common Coupling
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation

SHE	Selective Harmonic Elimination
TESS	Thermal Energy Storage System
ROI	Return Over Investment
THD	Total Harmonic Distortion
VICC	Voltage Current Cascaded Control
VOC	Voltage Oriented Control
VSC	Voltage Source Converter
ZOH	Zero Order Hold

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CHAPTER 1: BACKGROUND

1.1. Introduction

The challenges facing the modern electrical grid are improving its efficiency and operating capabilities, while meeting the projected energy demand with the integration of renewable energy sources, such as wind, solar, thermal etc. In order to meet these challenges, energy storage systems play a vital role. The energy storage deployments in the grid help to ensure a high flexibility and reliability of the system, as well as aid in the cost reduction to meet the peak load demand [1] [2].

There are various types of technologies available for energy storage, such as batteries, thermal storage, super capacitors etc.. Each technology involves unique advantages and disadvantages depending upon the application. Two well-known solutions that are being researched and implemented for energy storage deployment are:

1. Battery energy storage system (BESS)
2. Thermal energy storage system (TESS)

Selecting the most appropriate technology will ensure the cost-effectiveness for the power generation facility in which it will be implemented [3].

1.2. Battery Energy Storage System (BESS)

In BESS, electrical energy is stored as chemical energy in a battery. Lead-acid, Lithium-ion and Nickel Cadmium battery technologies are commonly utilized, out of which the latter are less than 40 years old. These technologies have dominated the low-

power electronics industry and are now increasingly being implemented in the high-power transportation and utility industries [2].

Renewable energy (RE) generation increases the demand for BESS to offset a number of limitations. As an example, energy generation by wind turbines or solar panels is sporadic which limits the usefulness of these sources. Another reason for the system's popularity and effective accessibility is due to the increasing popularity of electric vehicles (EVs) in the transportation industry; EVs exemplify environmental friendliness, improved performance and cost-effectiveness in comparison to fossil fuel vehicles. Thus, battery demand is increasing rapidly with newer and more innovative designs emerging in the market.

In the automotive industry, applications for energy storage solutions range beyond EV's. In fact, according to energy capital, the battery market is expected to grow at a substantial rate [4]. Presently it is very profitable to use battery storage systems in the automotive industry, however it might not be economical for other energy storage scenarios [3]. For example, lead-acid batteries, which are largely utilized for energy storage in electrical grids, also have high maintenance costs. As a result of the increasing share of RE sources in the automobile industry, large energy storage systems are required to ensure overall grid stability. However, the integration of these novel systems can lead to high maintenance costs, thereby making BESS a less effective solution [5]. Hence, even though batteries have beneficial characteristics, there are other energy storage technologies that may be better suited for certain tasks, such as the management of a power facility's energy costs [3].

1.3. Thermal Energy Storage System (TESS)

TESS compared to BESS is a better choice for high power usage (grid application) due to the following reasons:

- Long term return over investment (ROI) because batteries may only last for up to fifteen years before they require maintenance or replacement, while the thermal storage system has the capability to provide reliable performance for at least thirty years [3].

- With proper insulation in a tank for TESS, the energy can be usefully stored for weeks [6] and is capable of delivering at least 20 MW of power for up to 36 days continuously [7]. In comparison with TESS, the maximum capacity capability of BESS is limited for a few hours only for loads up to several megawatts [8].

- Furthermore, in TESS there is no chemical waste material, as found in lithium ion or other batteries, which saves the companies from the burden of disposal of batteries ultimately saving time and the money [3].

In TESS, energy is stored as heat. Power generation technologies, renewable or non-renewable, can easily be coupled with TESS. However, concentrating solar thermal power (CSP) is distinctive, despite it being similar to PV or wind. The CSP is unique because it concentrates direct solar radiation to heat in a fluid (i.e. molten salt is commonly used [9]) which can directly be stored into TESS, whereas others sources (i.e. wind, solar etc.) might require conversion to heat for later usage. TESS, when compared

with mechanical or chemical storage technologies, has higher efficiency and lower capital costs [10].

The principle options for using TESS depend on the daily and yearly variations of radiation and on electricity demand which are mostly based on the following [11]:

- Conserve energy during transient weather conditions
- Dispatch ability or time-shifting
- Increase of annual capacity factor
- More even distribution of electricity production

A TESS consists of three sub-systems:

1. **Storage System**

TESS stores the thermal energy either in the form of sensible heat, latent heat of fusion or vaporization, or in the form of reversible chemical reactions. Sensible heat materials in the form of synthetic oil and molten salt are the most widely used storage materials in large-scale CSP systems, while systems that utilize latent heat, thermo-chemical, and other sensible heat materials are still being developed [12].

2. **Heat Transfer System**

The purpose of the energy transfer mechanism is to supply or extract heat from the storage medium [12].

3. **Containment System**

The containment system holds the storage medium as well as the energy transfer equipment and insulates the system from the surroundings [12].

There are different topologies that are being investigated for improvement in TESS. In the case of direct steam generation power plants, phase change material (PCM) storage can be deployed for two-phase evaporation, while concrete storage can be used for storing sensible heat (i.e. for preheating of water and superheating of steam), thereby making TESS extremely favourable for direct steam generation power plants in the future [13]. Additionally, usage of hot water is well-known for the purposes of energy conservation in water heating systems based on solar energy and in co-generation energy supply systems. This is a very cost-effective storage option and has considerable room for improvement in its efficiency by ensuring an optimal water stratification in the tank and by highly effective thermal insulation [12].

The motivation for this proposal is to be able to use TESS technology during low-cost, off-peak times when the demand for electricity is low. Hence, as opposed to storing electricity in BESS, storing it in TESS seems more beneficial. In the long-term, it is advantageous in using electricity to heat up TESS material using power supplies, during off-peak hours. Therefore, designs of power supplies for heating purposes plays an important role for efficiency and reliability, which in the long term are essential factors to examine for any power plant or business.

Power supply applications based on converters usually suffer from two common problems: low power factor (PF) and high total harmonic distortion (THD) due to the generated harmonics. The aim is to establish the most cost-effective designs for rectifier-based power supplies for TESS, which keeps the power factor close to unity, while reducing the THD to an acceptable level. Since costs can be reduced further by decreasing the number of controllable switches, a feasible option is the half-controlled

converter instead of full control converter. As such, the goal of this research is to investigate and facilitate the integration of TESS with an existing utility grid. At the same time to improve the PF and reduce the THD so that the cost of the external filters can be minimized and, if possible, reduce the number of controllable switches. Heating elements for TESS can be viewed as resistors and inductors for converters in order to be used as load.

Also, similar converter designs and control topologies proposed in this research can be extremely useful for BESS as well for harmonic reduction.

1.4. Converters for Power Supplies

The typical thyristor-based, line-commutated converter provides the basis for most controlled power supply applications. These are widely used in industry for medium- and high-power applications and offer a low-cost solution. However, due to the thyristor control limitations, the main problem with this type of power supply is that it has a low PF and generates a high THD [14], which also varies with the converter operating point. When the output waveform of this type of power supply is examined, it offers an asymmetric waveform that contributes to the harmonic content and low PF.

Utilizing a gate-commutated switch, such as an IGBT, offers a converter option to provide a symmetric waveform with a much-improved PF and THD. Although the cost of the converter is somewhat higher, better control options over the output waveform are feasible [15]. In addition, the ability to use techniques such as pulse width modulation (PWM) allows the harmonics to be shifted towards higher-order frequencies which helps in cost reduction of external filters while also improving the PF.

1.5. Literature Review

This section provides a literature review of research in energy storage systems in the power grid infrastructure, choice of storage systems such as BESS or TESS, switch selection along with control algorithms for converters and modulation techniques. The research will assist in determining an ideal approach to the problem.

In power grid infrastructure, advancement in energy storage is the key for resources, such as wind or solar, because it can be used to reduce the peak power demand and lower the cost of the energy [2]. The benefits of battery storage have been observed for many years in small portable electronic devices and EV automotive industry. Similar benefits can now be expected from the smart grid [4] as well. There is high demand right now for fast responding energy storage as there is a concern over integration of new energy sources [16] with their increased variability. As reported in [16], energy storage is a key technology because it is capable of providing improved and flexible grid services. According to reference [17] "contract for deferral scheme" (CDS) which summarizes how an economically efficient portfolio of distributed generation, storage, demand response and energy efficiency can be integrated together in-order to reduce the grid capacity, showing the importance of the storage system. Likewise, [18] [16] state that energy storage systems are increasingly being deployed to provide grid operators the flexibility needed to maintain demand-load balance. Energy storage also imparts resiliency and robustness to the grid infrastructure. It further emphasizes the storage needs by discussing optimization methods that can be used effectively and utilize the storage system safely as an asset to provide services to power the grid.

The large-scale storage of electricity is both complex and expensive. The current technology of storing electricity in batteries, although gaining in popularity, is still not an entirely-established and competitive solution. Since one of the main uses of electricity is in the generation of heat, thermal energy storage technology offers another option because it can store heat in large amounts and has the capability of storing it for a longer period of time. Paper [19] reviews several energy storage technologies and analyzes their various characteristics including storage properties, current states in the industry and feasibility of future installation. According to this paper, TESS is in its developmental stage, has a 30-60% efficiency and has a lifespan of 5-40 years and is good for 0-300 MW capacity range. Alternatively, lead-acid battery technology is a mature technology and has 70-90% efficiency; however, it has a lifespan of only 5-15 years and is good for 0-40 MW capacity. Similarly, other battery technologies have matured and mostly have similar life spans as the lead-acid battery along with same or higher efficiency levels, but lower storage capacity. TESS requires more research. TESS appears to be more favorable as compared to a BESS for a grid with a high penetration of renewable energy sources. Study [20] assessed that TESS "reduces the levelized cost of electricity of renewable energy process, with the temperature of the storage medium being the most important parameter".

Reference [21] stated that carbon materials such as carbon fibers, nano-graphite particles and expanded graphite (EG) are the ideal choices as heat conductivity enhancers because they have high thermal conductivity, low density, thermo-chemical stability. Furthermore, these materials are also compatible with most PCMs. This article concludes that utilizing these materials could further enhance the heat transfer through the thermal

conductivity. The article further describes that duration for TESS was shortened when a combination of these materials were applied, however, it can be extended with increased density. Thermic Edge Vacuum Heating Technology describe that graphite is an appropriate element for heating in a thermal plant as high-density graphite elements are brittle, inexpensive and can be machined conventionally from large blocks. They also mention that it has low resistivity, so it can work with higher current supplies [22]. Hence, graphite appears to be a fitting choice to design the heating element in the TESS. In order to couple it with a converter for heating purposes, the typical values of the resistance and inductance of a heating element needs to be found.

To come up with cost-effective solutions for converters, with PF close to unity and reduced THD, numerous research papers were studied. In [23]. The authors recognized the problem to fix the PF and tried to shape the input current to a sinusoid (fundamental waveform of current) using a fixed-band technique called Hysteresis Current Control (HCC). They analyzed the cause of imbalance using appropriate models and used HCC methodology to eliminate it. They managed to obtain an efficiency of 96% (i.e. PF close to unity), albeit, with an increase in the cost. Reference [24] presents the different technologies used in the generation of large controlled currents. While analyzing a future alternative for rectification in industrial processes, this paper compares chopper–rectifiers in terms of quality of control, harmonics, power factor, losses, and efficiency. It concludes that chopper–rectifiers have enough field experience to be considered as an alternative in the generation of controlled current in the kilo-amperes range.

In [25], it is shown that elimination of the second harmonic in the DC output voltage of the phase-controlled converter under unbalance can be accomplished by using

an individual asymmetrical firing angle. Significant reduction in the distortion of the converter output voltage with the proposed cancellation approach was noted. But the proposed method can increase as well as decrease the THD factor of the input currents depending on the tuning. Additionally, it was also noted by [26] that the elimination of the second harmonic in the DC output voltage of the phase-controlled converter under unbalanced conditions can be accomplished by using an individual asymmetrical firing angle. It was further noted in [27] that an asymmetrical configuration provides nearly sinusoidal voltages with very low distortion, using fewer switching devices. Moreover, torque ripples are greatly reduced. However, [28] shows that under symmetrical control method, all the power switches conduct uniformly unlike asymmetrical control and hence resulted in non-uniform heat distribution in asymmetrical control. It was further discussed in [29] that the compensation of asymmetrical harmonics is less efficient than symmetrical ones. All devices connected to the grid should be able to withstand higher harmonic distortion. However, the most popular control methods for an AC-DC converter such as Voltage Oriented Control (VOC) or Direct Power Control (DPC) are not a fit to work with higher harmonics. Reference [30] specifies that switching in inverters causes the generation of harmonics. Hence, to improve the performance, harmonics can be reduced by unifying selective harmonic elimination (SHE) of a 3-phase VSI.

According to this paper, it is well known that higher switching frequency reduces the filter size but increases the switching loss. Thus, this paper investigates a novel modulation method where additional notches are introduced with multi-level output voltage along with SHE and PWM. For switch-mode operation, paper [31] provides a solution through dead-time delays using SHE with PWM. This paper investigates the

effect of dead-time distortion on the performance of SHE and sinusoidal PWM techniques for single-phase DC-AC inverters with unipolar voltage switching. Without making any changes to conventional converter design, reference [32] discusses the generalized formulation for SHE-PWM. This paper reports through an experiment describing why SHE-PWM is more suitable for high-voltage, high-power cascaded multilevel voltage source converter (VSC). This paper also confirms that multiple independent sets of solutions exist for VSCs.

Furthermore, [33] also compared symmetrical Cascaded Multilevel Converters (SCM) with the conventional CM converter structures. These noteworthy advantages of the proposed topologies decrease the price, size, and installation area of the common mode (CM) converters rendering them more suitable for medium voltage (MV) high-power applications. Paper [34] presents novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converters. These topologies can produce many levels with a minimum number of power electronic switches, gate driver circuits, power diodes, and DC voltage sources. Another proposal [35] on an advanced structure for symmetric multilevel voltage source inverters showed that the lower number of needed circuit equipment resulted in a remarkable reduction in general costs and installation area, improved reliability and simpler control procedure. In addition to reduce the cost, [36] worked on the reduction of a number of switches and voltage sources and concluded same output can be obtained with less number of switches. A 1-phase and 3-phase 2^{nd} order high performance controller for converter using voltage control is presented in [37]. This paper examines the control system and does the performance evaluation concluding that proposed controller provides extensive control of voltage and current against a set of

uncertainties and loads. Paper [38] discusses the rules for tuning controllers such that non-ideal operating condition including delays, filtration problems and AC phase unbalance can be dealt with. It is an experimentally based paper which resolves these issues on the basis of the analysis of transient behavior and of the steady state harmonic content of DC voltage and of the AC current. This idea is further discussed in paper [39], where a cascaded current voltage control strategy is used to improve the power quality and current exchange with the grid. The control scheme uses an inner voltage loop and outer current loop. This topology can be used in 1-phase or 3-phase converters. It allows grid-connected converters to inject balanced and clean currents to the grid even in non-linear operation modes. Paper [40] discussed advanced vector current control topology for VSC connected to a weak grid which allows high performance regulation of active power and the voltage for viable VSC range of operation. The frequency response and stability are analyzed in this paper of on a conventional vector control showing that it could be a promising approach to tackle the problem of VSC operating with weak AC grids.

Chapter 1 provided a literature background to the topic, pointing out the importance of storage systems as a solution to the apparent problem grid infrastructure. The rest of the thesis is organised as follows: Chapter 2 provides the motivation for this work and the tasks that are required. Chapter 3 elaborates on research regarding the heating materials for TESS in terms of its electrical properties leading towards the designs of power supplies suited for heating. Then, in Chapter 4, heating applications are elaborated upon by comparing two types of 1-phase converters (asymmetric and symmetric) with voltage-oriented control. The advantages and disadvantages of these

approaches are discussed. In Chapter 5, the design selected between the two converters is constructed with a modulation technique and low pass filter (LPF). Subsequently, in Chapter 6 the selected approach is applied to 3-phase converters and compared to an alternative controlling scheme to devise an optimal solution for TESS. Chapter 7 then concludes the thesis.

CHAPTER 2: MOTIVATION FOR THIS WORK

As the transformation towards a low carbon and more decentralised energy grid continues, the flexibility requirements for the electrical grid system are increasing. Energy storage system is now seen as both a disruptive technology and a key enabler in the transition towards a smarter, cleaner energy system [41] . Consequently, improving **energy storage is the next challenge** because, with the current technology, electricity cannot be stored easily or efficiently at significant power levels (i.e. greater than a few MW). In order to attain this, the two main options that are being looked at are BESS and TESS. TESS, when compared to BESS, appears to be a more promising technology for the increasing needs of energy storage in the grid since:

- TESS has more ROI in the long term as described in section 1.3
- TESS is capable of storing energy for longer time periods, and at lower cost
- TESS capacity limit exceeds BESS technology capacity
- TESS is more environmentally friendly i.e. it has less harmful disposal needs unlike batteries (i.e. lead acid)

So, **the motivation of this work is to use TESS to store surplus electricity as heat during off-peak times and utilize it during peak-times, in-order to reduce energy costs and meet the growing need of storage capacity**. The following tasks are required to accomplish this goal:

1. Initially, convert off-peak electricity into heat energy to be stored in TESS. This process of this conversion involves an appropriate converter selection

2. The challenge is to do the conversion process with low cost (reduced size of filters, and reduced number of components), high efficiency (low wastage), and good power quality (less than 5% THD [42] and unity PF), hence not wasting the energy during the conversion process. This necessitates using suitable switches and controller designs.

CHAPTER 3: HEATING MATERIAL FOR THERMAL ENERGY STORAGE SYSTEM (TESS)

3.1. Introduction

In TESS, energy is mostly stored as sensible heat using materials in the form of synthetic oil and molten salt as storage materials. An efficient way to heat up these storage materials with electrical energy is to have a heating element. This element will act as a link for conversion from electrical to heat energy. Therefore, to heat up the storage material with electrical energy; heating element for the TESS needs to be known (in terms of its electrical properties, i.e. resistance and inductance) so that it can be used as a load for the power supply designs. Accordingly, the choice of the heating element, its design and some of the calculations are presented in this chapter.

3.2. TESS Design

3.2.1. Resistance of Heating Element

Graphite is an appropriate element for the heating in an electro-thermal plant as high-density graphite elements are brittle, inexpensive and can be machined conventionally from large blocks. Therefore, large sized elements can be produced in a variety of shapes and sizes. Graphite has a low expansion coefficient and does not degrade due to constant heating and cooling cycles. Its low resistivity means it requires high current power supplies. Moreover, it has a capability of operating up to 2000^{o} C in an inert atmosphere, 1800^{o} C in a vacuum [22]. Graphite materials have been used as important parts in industrial furnaces generating high temperatures above 2000° C [43].

The sample distribution grid that is being used as the test case for this research is rated at 2.15 kV (V_{base}), feeding into the point of common coupling (*PCC*) through the supply transformer rated at 2.5 MVA, and providing about 2 MW (P_{base}) of DC power to the load. Thus, it makes it possible to calculate the base impedance (Z_{base}) that is required, as shown below:

$$Z_{base} = \frac{Vbase^2}{Pbase} = \frac{2150V^2}{2MW} = 2.31\ \Omega \tag{3-1}$$

For a 3-phase converter, it would require three times the load, which would increase the resistance to be 6.93 Ω

3.2.2. Dimensions of the Element:

One element is →

Figure 3.2-1: Graphite Single Heater Element Shape

Fig. 3.2-1 shows a simple design of one element of the Graphite heater coil. In order to find the dimensions of this element the following formula can be used [44]:

$$R = \frac{\dot{\rho} l}{A} \tag{3-2}$$

Where,

R = Resistance, in ohms (Ω)

$\dot{\rho}$ = Resistivity constant of the material, in Ω.m

l = Length of the wire, in meters

A = Cross sectional area of the wire, in m^2

In order to find the cross sectional area **A** and length **l,** since Z_{base} is known, it can be used as resistance, and resistivity constant of the material **ṕ** for pure graphite for one square meter at room temperature is given below [45]:

$$\acute{\rho} = 1380 * 10^{-8}\ \Omega.\text{m}$$

From the literature, it is known that the resistance of graphite materials increases monotonically with increasing temperature up to 3000° C after passing through a minimum at around 1000° C. However, a resistance reduction at around 2000°–2500° C is often observed in Argon (Ar) atmosphere due to ionization of Argon [43].

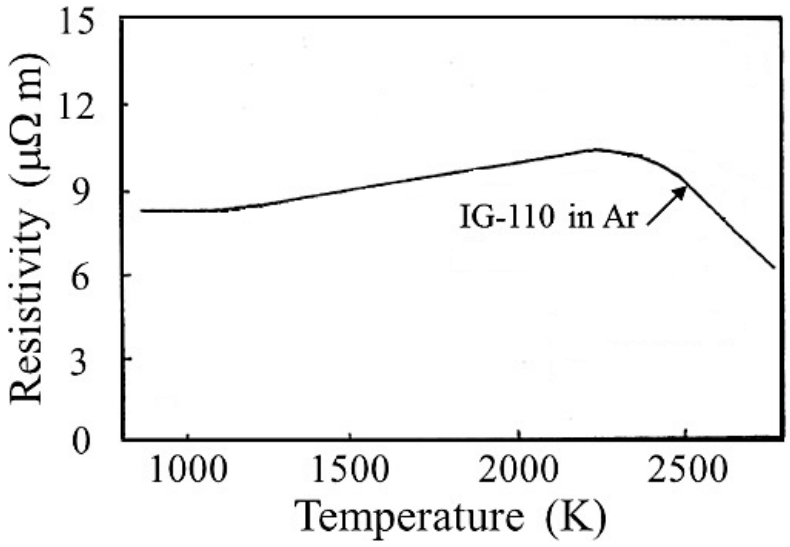


Figure 3.2-2: High-density graphite IG-110 in Ar Atmosphere [43]

The resistivity decreases above 2000° C (2273° K), as shown in Fig. 3.2-2 [43]. Therefore, the converter design for heating purposes should be dynamically able to handle the changes in its non-linear resistive load.

3.2.3. Inductance of Heater Element:

In order to calculate the loop inductance of the graphite heater element, eq. (3-3) below can be used [46]:

$$L_{loop} = \frac{\mu_r \mu_o}{\pi}[-2(w+h) + 2\sqrt{h^2+w^2} + x] \tag{3-3}$$

Where,

$$x = -h\left(ln\left(\frac{h+\sqrt{h^2+w^2}}{w}\right)\right) - w\left(ln\left(\frac{w+\sqrt{h^2+w^2}}{w}\right)\right) + h\left(ln\left(\frac{2h}{\frac{d}{2}}\right)\right) + w\left(ln\left(\frac{2w}{\frac{d}{2}}\right)\right) \tag{3-4}$$

$$\boldsymbol{\mu_r \mu_o = -1.6} \quad \textit{for graphite} \text{ [47]}$$

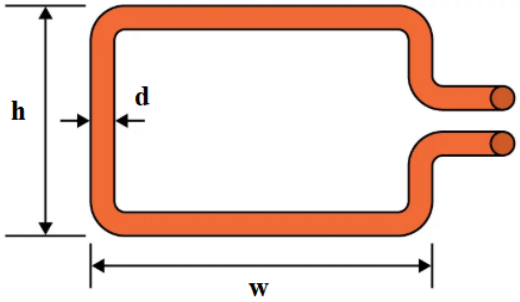


Figure 3.2-3: Dimensions of Single Heater Element [46]

Fig. 3.2-3 shows the dimensions of the single heater element in order to calculate the inductance. By defining width (***w***), height (***h***) and depth ***(d)*** according to resistance using equation (2), the inductance can be found using equation (3) and equation (4). Given a length of single heater element to be *3593.6mm*, the ***w, h*** *and* ***d*** *are as follows:*

w *= 1779.3mm*

h *= 35mm*

d *= 122.47mm*

This gives the inductance of each loop to be ***0.679 μH***

And for three phases, it would be = ***2.037 μH***

This value of inductance per heating element is fairly low; also, it does not include any inductance addition due to any leads etc. that may be needed to connect to the heating rods. Nevertheless, this low value of inductance should not pose serious problems for the dynamic operation of the converter.

3.3. Proposal for replacing AC-AC converter with AC-DC converter

3.3.1. Thyristor based AC-AC converter - Limitations:

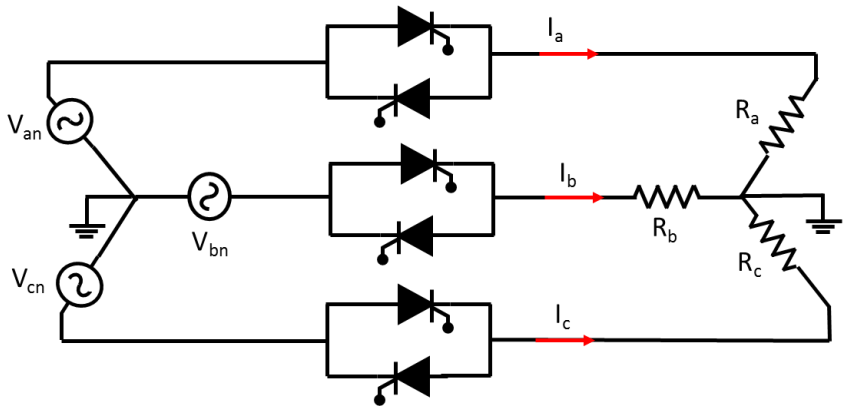


Figure 3.3-1: Circuit diagram of AC-AC Converter

Fig. 3.3-1 displays a simple circuit of an AC-AC converter that is conventionally used. Each phase is connected to two back-to-back thyristors and a load in this circuit. The limitations of the existing AC-AC converters are as follows [15]:

a) Due to line frequency commutation, the characteristic line harmonic currents are of the order of 6n±1, i.e. 5^{th}, 7^{th}, 11^{th}, 13^{th} and so on. Low-order harmonics filtering requires bulky filters (composed of inductors and capacitors). Therefore,

the overall cost of the system is higher, and it also requires more space for installation of the converter.

b) Due to poor power factor, cost penalties imposed by utilities could be significant. Moreover, the kVA rating of the supply transformer will increase and be more expensive than normal.

c) Three tungsten rods (electrodes) per heater assembly are required. Therefore, more investment in material procurement is needed. More terminals (connectors) also mean less reliable systems.

3.3.2. Proposed TESS Overall System Design

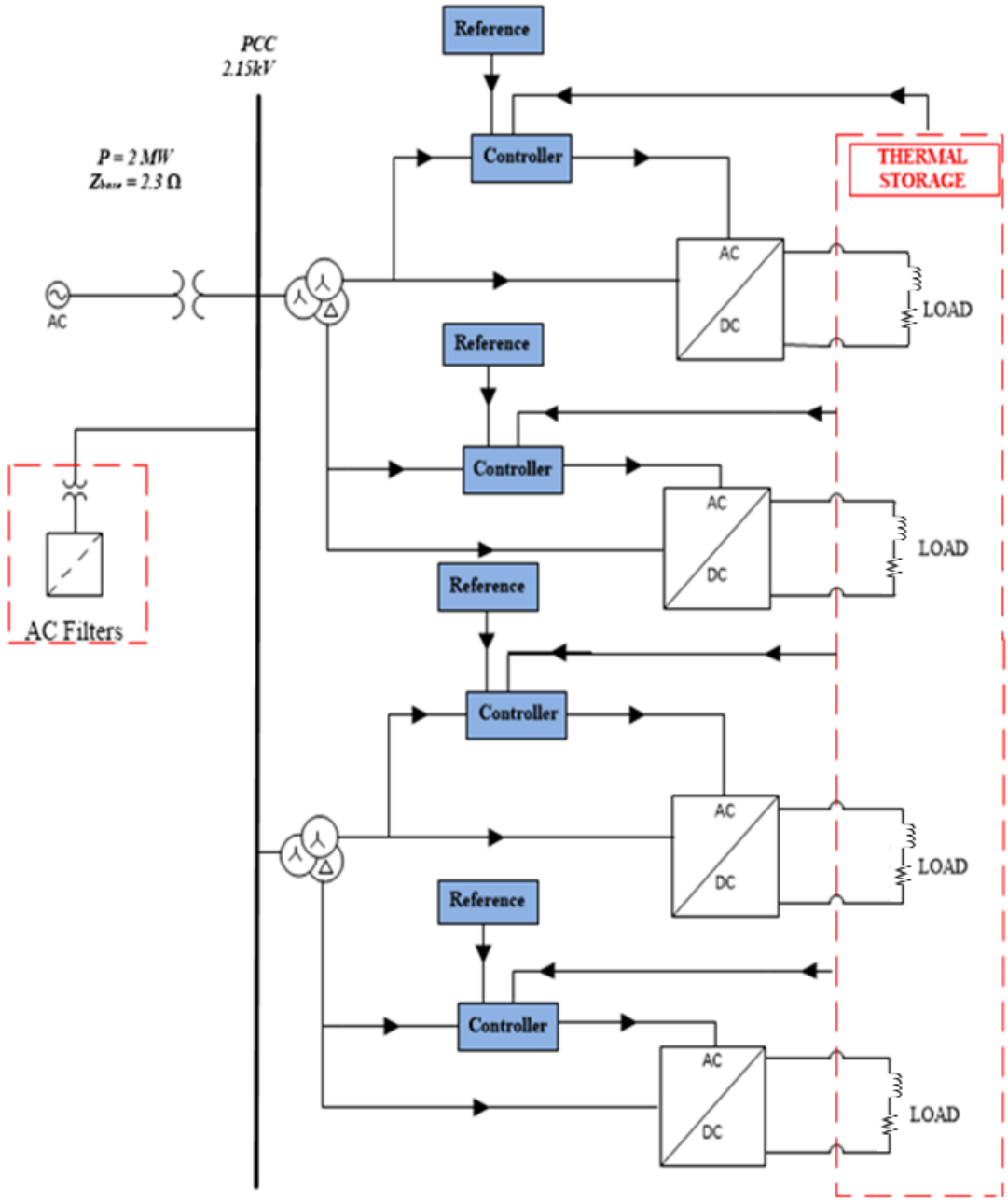


Figure 3.3-2: Illustration of the whole system

The selected model is rated at *2*-MW based on the following reasons:

I. One 3-winding transformer supplies two AC-DC converters, via star-star and star-delta transformer connections, as shown in Fig. 3.3-2. This

introduces a 30 degs. phase shift between AC inputs to the two converters allowing the cancellation of the lower-order (fifth and seventh) harmonic frequencies.

II. This, in turn, leads to a reduction in the size of the harmonic filter at PCC bus.

III. Design provides for multiple converters in parallel, providing redundancy in design and, therefore improved reliability.

IV. On the DC side, the output of the two converters can be connected in bi-polar fashion, with a positive pole, a negative pole and grounded neutral (similar to HVDC converters – a proven topology).

CHAPTER 4: 1-PHASE CONTROL AND SWITCHING TECHNIQUES

4.1. Introduction to Single Phase Rectifier

In a 1-phase, full-wave diode (uncontrolled) rectifier circuit (Fig.4.1-1), diodes D1 and D2 are used for the positive-half-cycle; diodes D3 and D4 are used for the negative-half-cycle. During the positive half-cycle, D1 and D2 conduct in series, allowing the current flow through the load; D3 and D4 remain off due to the negative voltage. Similarly, during the negative half-cycle, D3 and D4 conduct, while D1 and D2 are off. The current flowing through the load is unidirectional, and the average DC voltage across the load is 0.637Vmax in a 1-phase rectifier. To obtain full control, the four diodes are replaced with four controlled switches (i.e. thyristors). However, since the cost of operation is an essential consideration for this application, a half-controlled 1-phase rectifier can be examined, as diodes are more cost-effective than controllable switches [48].

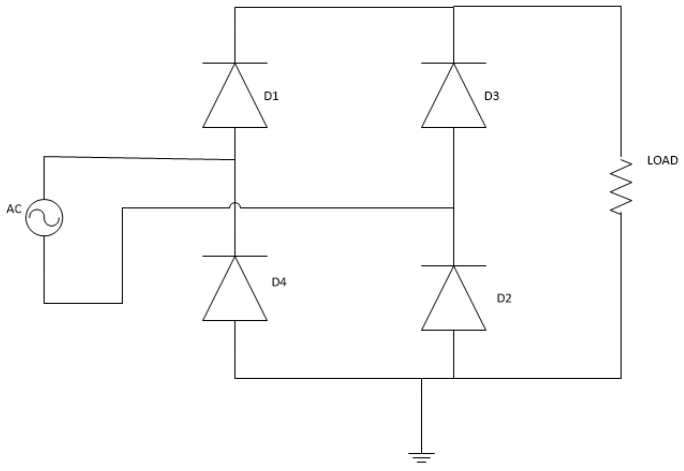


Figure 4.1-1: Single Phase full wave Converter

4.2. Thyristor-based line-commutated converter – asymmetric converter

Fig. 4.2-1 shows a half-controlled, thyristor-based, line-commutated asymmetric converter, rated at approximately 2 MW. Using a 2.15 kV PCC, this converter is fed from a 1.07 kV source using a transformer that feeds a resistive load of 2.3 Ω. The load is not grounded on the DC side.

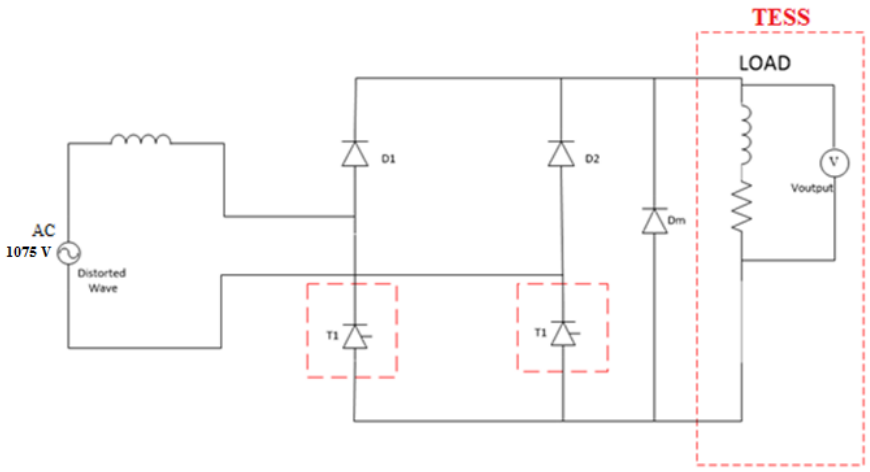


Figure 4.2-1: Half-controlled, thyristor-based, line-commutated asymmetric converter

In Fig. 4.2-1, the converter is composed of two diodes, D_1 and D_2, as well as two controlled thyristors, T_1 and T_2. Additionally, a freewheeling diode, D_m, is connected across the load in order to manage an inductive load. In this converter, T1 and D2 operate as a pair, while T2 and D1 operate as another pair.

4.2.1. Characteristics of Thyristor based AC-DC Converter

A thyristor can be latched on by a single pulse of positive voltage/current applied to its gate terminal, and it will remain on until the end of the positive cycle of the voltage. Thyristors are cost-effective when compared to switching devices such as, GTO's, MOSFETs and IGBTs. In order to be more cost-effective, two thyristors are used in this

converter, whereas fully controlled converters with firing angle control utilize four thyristors [49].

4.2.2. Firing Angle Control in Asymmetric Converter

Using this method, thyristor T1 is turned on at $\omega t = \alpha$ *(Alpha)* and turned off at $\omega t = \pi$, at which point the voltage reverses. Thyristor T2 is turned on *at* $\omega t = \pi + \alpha$ and is turned off naturally at 2π completing one cycle (period). Thus, by varying the firing angle α, the output voltage can be controlled.

In the corresponding control diagram (Fig. 8), the V_{output} is sensed from the load and the firing angle, α, for this converter is inputted manually. Voltage reference (V_{ref}) is directly related to firing angle α. The relationship between them is described by equation (4-1):

$$V_{ref} = \frac{(180 - \alpha)}{180} \tag{4-1}$$

A second order LPF is used on the measured V_{output} to obtain the average value, V_{avg}. The second order LPF performs much better than a first order LPF. The damping factor, ζ, in this system is 0.707 and it directly effects the filter quality (Q) control. The formula below represents the relationship between Q and ζ [50]:

$$\zeta = \frac{1}{2Q} \tag{4-2}$$

Where ζ is used in LPF transfer function as follows:

$$H(s) = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}$$

(4-3)

Where,

$$s = Laplace\ Operator$$

$$\omega_n = natural\ frequency = 2\pi f_n \rightarrow fn = 5Hz$$

This operation is theoretically defined by the following equation (4-4):

$$V_{avg} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_{output}\ sin\omega t\ d(\omega t)$$

(4-4)

$$= \frac{2V_{output}}{\pi}\cos\alpha$$

Followed by that, V_{ref} is compared with the pu value of the average output voltage (V_{avg}) changing the V_{avg} according to V_{ref} (V_{dc}). V_{dc} is then fed through a Proportional Integral (*PI*) controller (with proportional gain Kp = 5 and integral gain Ki = 100) to minimize the error over repetitive cycles (V_{Error}).

A synchronized saw-tooth waveform, V_{saw}, is generated from the fundamental component, V_{in}, and is then compared to V_{Error} to generate the switching pulses.

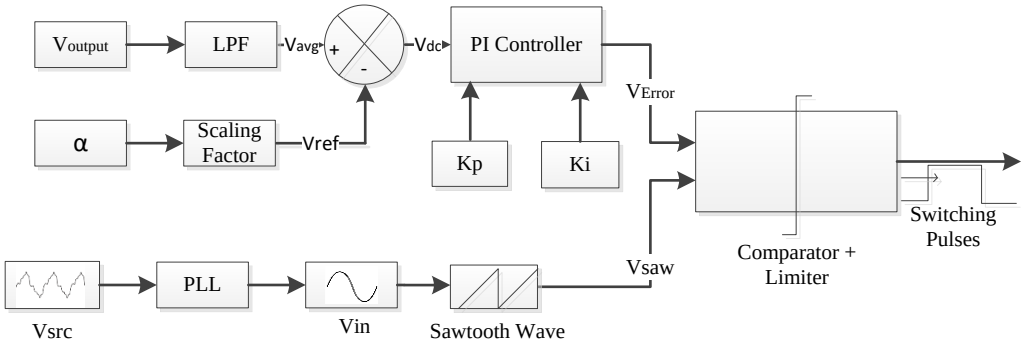


Figure 4.2-2: Algorithm for Asymmetric Controller

The process of obtaining the saw-tooth wave (V_{saw}) from the source is shown in Fig. 4.2-2. The sinusoidal waveform V_{src} of the source is sensed, and a phase locked loop (PLL) is used to derive the fundamental component, V_{in}, of the source voltage with the extraction of harmonic pollution. Limiting the V_{in} between 0 and 1 creates the square wave. This wave is then separated for positive and negative cycles. Integrating and limiting these waves results in the saw-tooth waveform V_{saw} for positive and negative cycles.

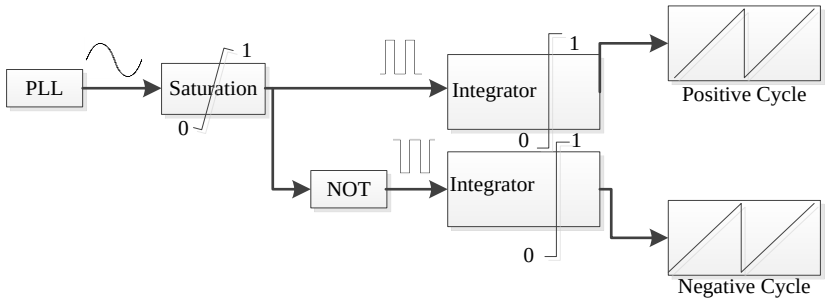


Figure 4.2-3: Algorithm for Generation of Saw-tooth Wave

4.2.3. Results

In conjunction to V_{in}, α plays an important role in determining V_{output}. Fig. 4.2-3 shows the ideal behaviour of V_{output} based on the value of α which is determined by $V_{ref.}$ The variation of α provides a means to control the output voltage due to the change of the load resistance, which can occur due to temperature changes as discussed in section 3.2.2.

4.2.3.1. Output

In Fig. 4.2-4a, the V_{in} from V_{src} is shown, as well as the corresponding saw-tooth waveform for the positive half and negative halves of the sinewave. These are then compared to the V_{ref} voltage to generate the firing pulses (Fig. 4.2-4b) for the positive half (in red) and the negative half (in blue). Fig. 4.2-4c is shows the V_{output} waveform (in pu) at the chosen firing angle. As the magnitude of V_{ref} is varied, the firing angle can be controlled.

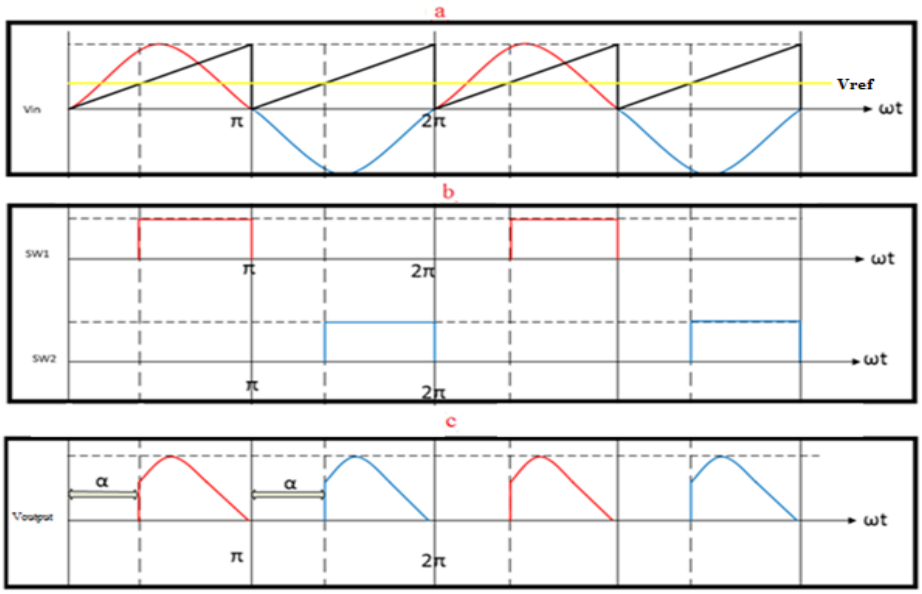


Figure 4.2-4: Expected Resulted Waveform

To compare the behavior of the asymmetric converter, Fig. 4.2-5 to Fig. 4.2-7 show the sampled waveforms at α = 30, 60 and 90 degs. respectively.

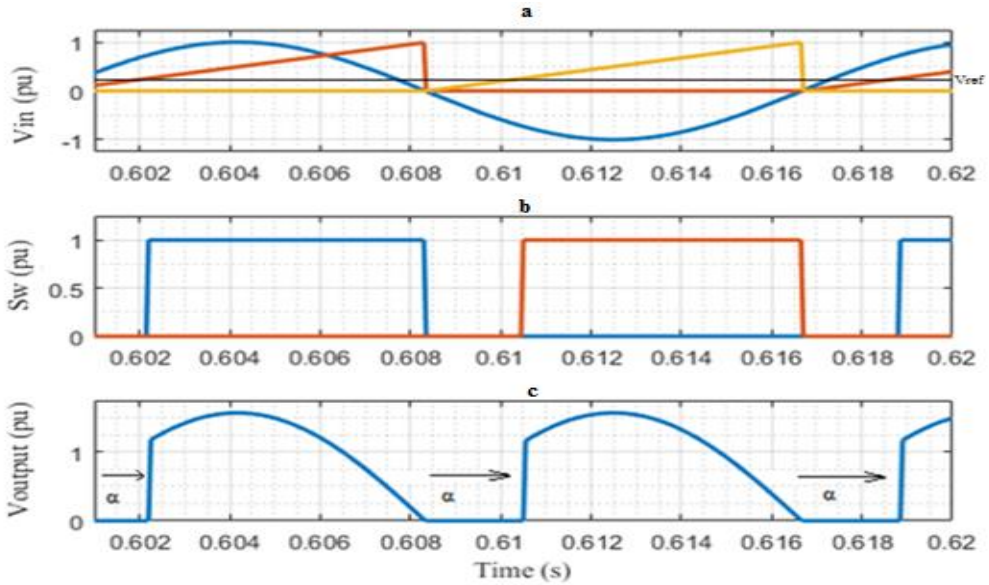


Figure 4.2-5: Sample Resulted Waveform at α =30 degs.

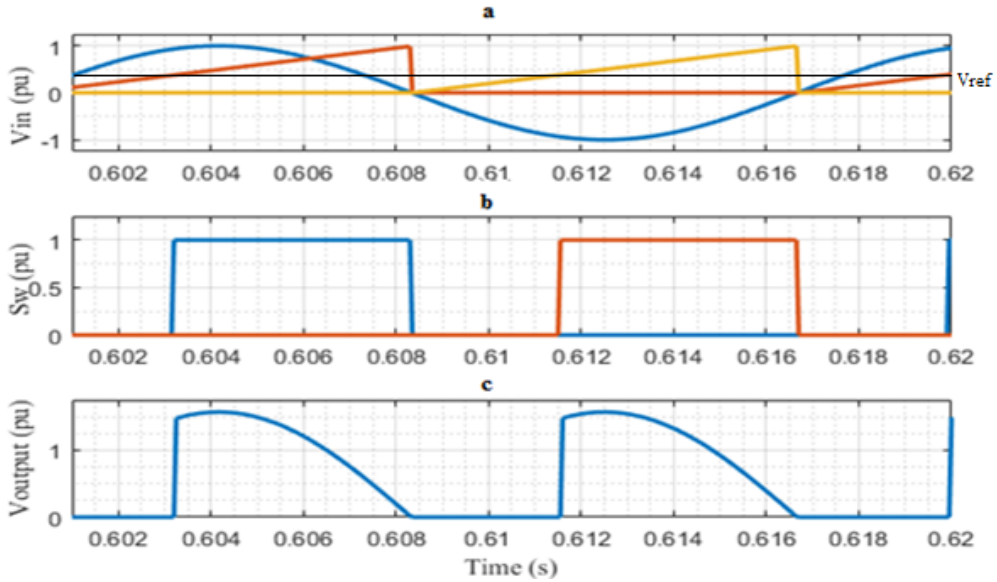


Figure 4.2-6: Sample Resulted Waveform at α =60 degs.

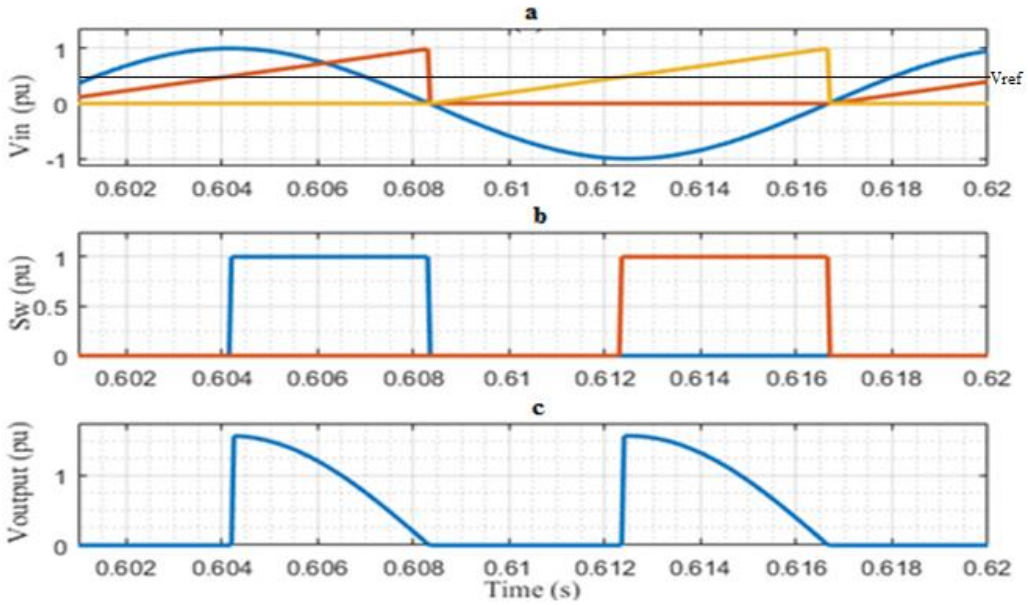


Figure 4.2-7: Sample Resulted Waveform at α =90 degs.

Figs. 4.2-5a to 4.2-7a show the variation of V_{in} (in blue) and the corresponding saw-tooth waveform for the positive (in red) and negative (in yellow), varying from a -1.0 pu to 1.0 pu versus time in seconds (s), varying from 0.602s to 0.62s. Sampling time chosen for Fig. 4.2-5a to Fig. 4.2-7a depict one complete cycle, and shows the V_{in} in comparison to generated saw-tooth waveform and V_{ref} (in black).

Furthermore, Fig. 4.2-5b to 4.2-7b display the variation of switching pulse for positive cycle (in blue) and for negative (in red) in pu, varying from a 0.0 pu to 1.0 pu versus the time in seconds, varying from 0.602s to 0.620s. From these figures, it is evident that the rising switching pulses are determined by the intersection of V_{ref} and the saw-tooth waveform of positive and negative cycles.

Finally, Fig. 4.2-5c to 4.2-7c depicts the variation of V_{output} in pu, varying from a 0.0 pu to 1.3 pu versus time in seconds, varying from 0.602s to 0.62s. V_{output} in the sampled figures are displaying the relation between switching pulse and V_{in}. The width

size of V_{output} is the same as the generated switching pulse, whereas, its shape is determined by V_{in} in the range where the switching pulse is on.

4.2.3.2. Power Factor (PF)

PF plays a vital role in this power supply as it determines the incurred cost of energy. PF is the ratio of actual electrical power dissipated by the AC side to the product of the R.M.S. values of current and voltage. The PF is equal to the cosine of the (phase) angle difference between the voltage and the current. As the phase increases between the two waveforms, the PF moves away from the unity. The other factor that affects the PF are the harmonics in the input current.

Nonetheless, since harmonics are expected, only fundamental waves are compared between the voltage and the current to determine the PF. The relationship between PF angle and firing angle, α, is shown in Fig. 4.2-8:

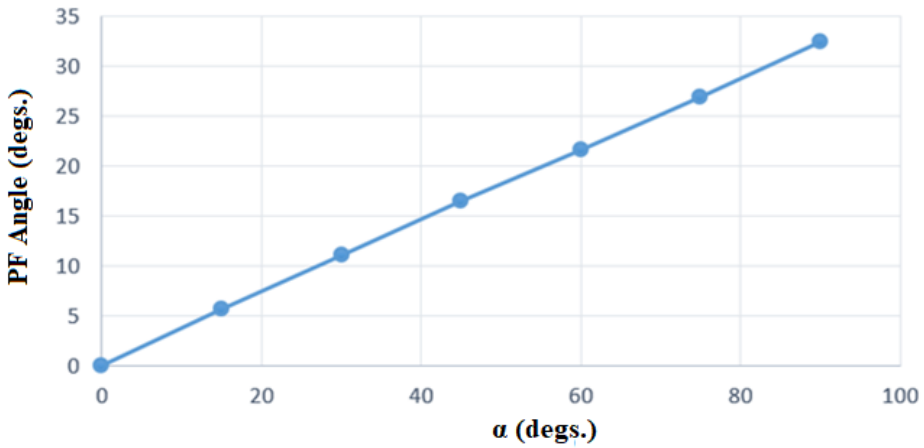


Figure 4.2-8: α versus PF comparison in Asymmetric Converter

Fig. 4.2-8 displays the variation of PF angle in degs., varying from 0 deg. to 35 degs. versus α in degs., varying from 0 deg. to 90 degs.. Fig. 4.2-8 shows that PF varies linearly with firing angle α. At α of 0 degs., the PF angle ϕ is also 0 degs. (i.e. PF = cos (ϕ) is unity). At α of 90 degs., the PF angle is approximately 35 degs..

The measurement of PF is cumbersome within a converter application due to the presence of harmonic distortion in the current and voltage waveforms. The PFC shapes the input current by removing some of the harmonics and cancelling part of the reactive component of current. This not only minimizes the losses due to the harmonics, but also effects the power quality of the grid [51]. PF is defined as the ratio of real power to apparent power:

$$PF = \frac{Real\ Power\ (Watts)}{Apparent\ Power\ (VA)} \tag{4-5}$$

Furthermore, the harmonic distortion varies with the firing angle. The measurement of ϕ was obtained by comparing the fundamental component of input current versus input voltage. Various methods were attempted to derive clean fundamental component waves from the polluted input current, as well as input voltage waveforms including the use of FFTs, Butterworth low-pass and band-stop filters. Finally, the PLL method of deriving the fundamental components proved successful.

4.2.3.3. Harmonics

Fig. 4.2-9 displays the harmonics without using PWM and filters at α = 30, 60 and 90 degs.. These are odd harmonics and well spread out from Harmonic order 3 (180 Hz) and onwards. Due to the fact that they are well spread out, filtering is not an easy and cost-effective task.

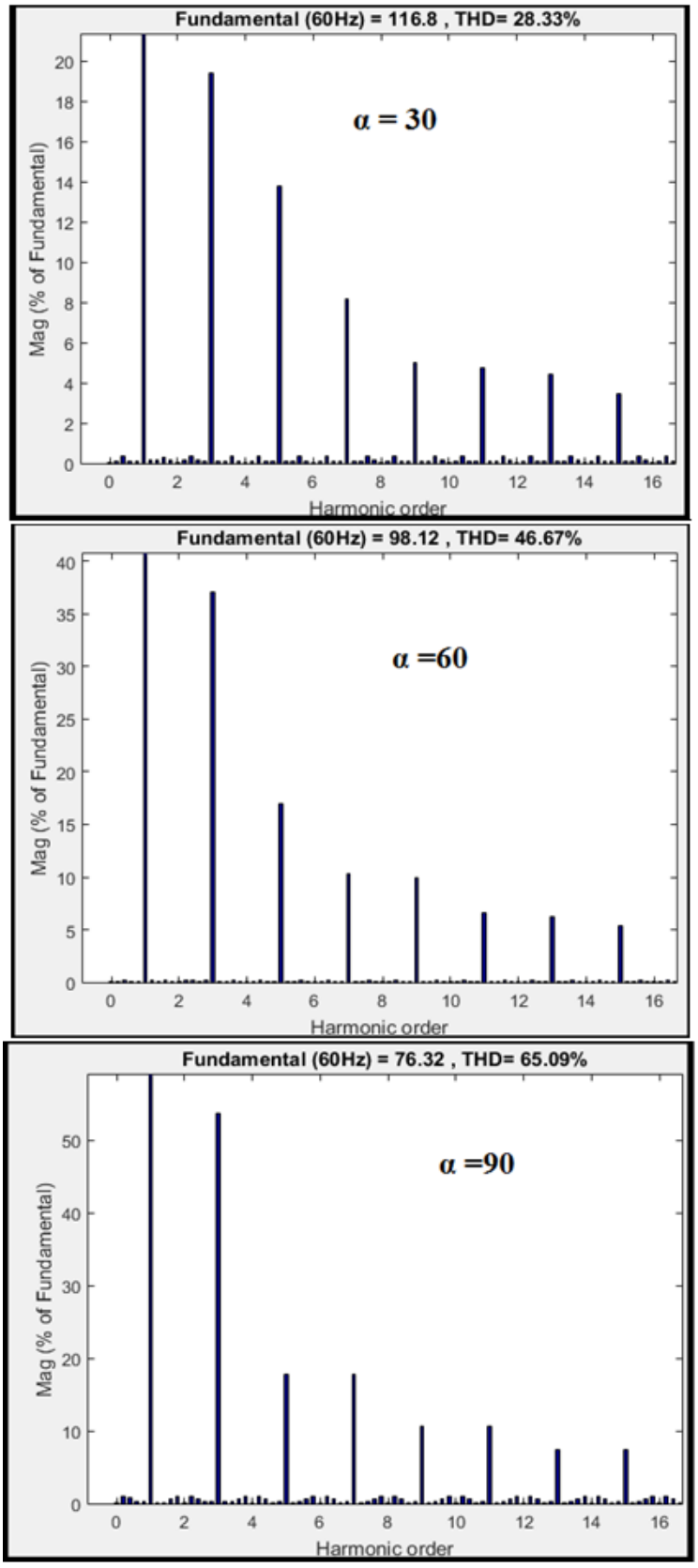


Figure 4.2-9: Harmonics Order at α = 30, 60 & 90 degs.

No LPF is used for the THD above; comparison between THD and firing angle α is shown in Fig. 4.2-9. The waveform shape of the output voltage is close to the input current. These current waveforms are asymmetric; however, they can be considered as quadrant symmetric (positive cycle has a similar shape as the negative cycle). Moreover, the input current shape is asymmetric, similar to V_{output} as can be seen at α = 30, 60 and 90 degs. in Fig. 4.2-10 versus in Figs. 4.2-5c to 4.2-7c. Thus, when positive and negative cycles are combined together, they are compared with a sinusoidal waveform; it can be noted that the shape of the waveform has an increasing opening which is determined by α angle value, which can vary from 0 deg. to 90 degs.. This causes the harmonics to increase because of change in shape as compared to a normal sinusoidal wave. This also can be seen from the following THD formula:

$$THD = \frac{\sqrt{I1^2 + I2^2 + I3^2 + \cdots + In^2}}{I1} \tag{4-6}$$

Where I_1, is the fundamental current, other order currents cause the THD to increase, ultimately also effecting the PF.

The relationship between THD and firing angle, α, is shown in Fig. 16:

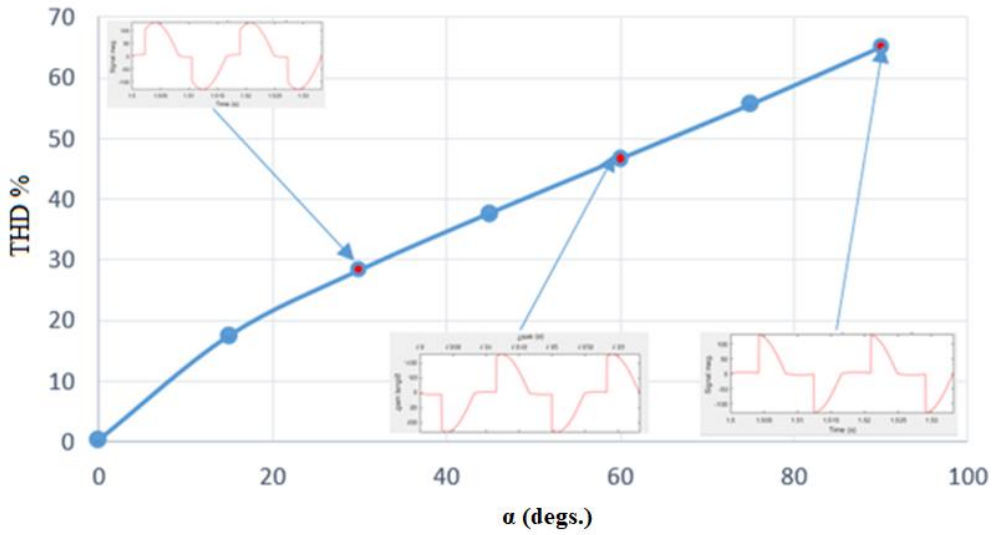


Figure 4.2-10: α versus THD comparison in Asymmetric Converter

Fig. 4.2-10 shows the variation of THD in %, varying from a 0% to 70% versus the α in degs., varying from 0 deg. to 90 degs.. Fig. 16 illustrates that THD is increasing from 0% to almost 66% as the value of α varies between 0-90 degs..

4.3. IGBT-based, force-commutated converter – or symmetric converter

Fig. 4.3-1 shows a half-controlled, IGBT-based, force-commutated symmetric converter rated at about 2 MW. Using 2.15 kV PCC, this converter is fed from 1.07 kV source with the help of a transformer feeding a largely resistive load (2.3 Ω).

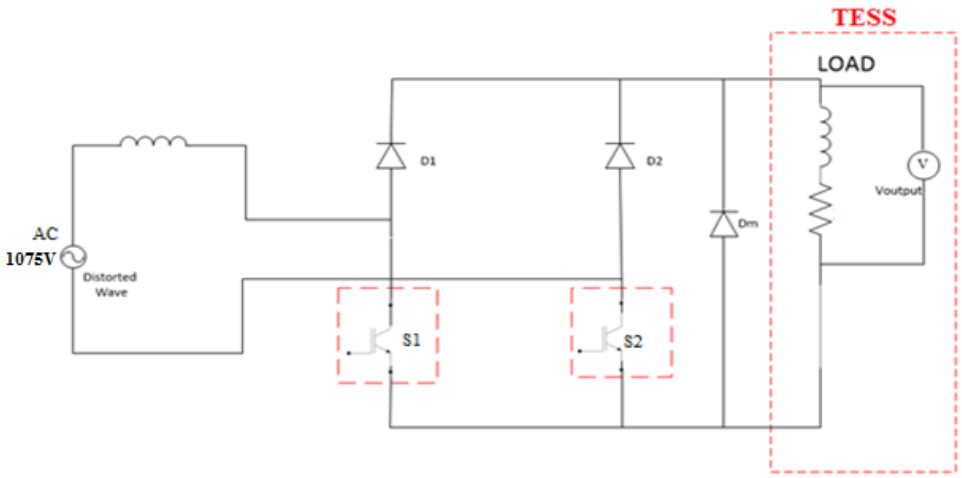


Figure 4.3-1: Half-controlled, IGBT-based, line-commutated symmetric converter

The converter is composed of two diodes D1 and D2, and two controlled IGBT switches S1 and S2. A freewheeling diode, D_m, is connected across the load in-order to handle the inductive load.

4.3.1. IGBT based AC-DC converter

For AC-DC converters, the advantages of using IGBT switches are as follows [15]:

a) IGBTs are capable of switching in kHz range, typically as high as 10 kHz. Since the line harmonic currents occur at multiples of switching frequency, there are no low-frequency harmonics present; filtering becomes easier and, therefore, it is cheaper and easier to meet THD standards.

b) Moreover, PF closer to unity can be achieved. Cost penalties from the utility are not incurred and the size of the main transformer is smaller and is more efficient.

c) Due to DC output, only two terminals are required for the connection of the load. Therefore, only two tungsten rods will be required per heater assembly instead of

three. This leads to a reduction in capital investment as well as improvement in reliability of the system.

d) Moreover, control system of IGBT is simpler than thyristor-based line-commutated converter allowing the flexible control over both turn-on and turn-off instants.

4.3.2. Firing angle control with Symmetric Control

The firing angle control method is being used in this converter, where D1 works together with S1 and D2 works together with S2. S1 performs the switching action such that it goes in on mode at $\omega t = (\pi - \beta)/2$ and off mode at $\omega t = (\pi + \beta)/2$. Similarly, S2 goes into on mode at $\omega t = (3\pi - \beta)/2$ and off mode at $\omega t = (3\pi - \beta)/2$. Thus, by varying the conduction angle Beta β, the output voltage can be controlled.

As shown in Fig 18, V_{output} is sensed from the load and conduction angle β is inputted manually. V_{ref} is produced using firing angle β. V_{ref} is directly related to the conduction angle β, which is in per unit (pu), and is described in equation (4-7):

$$V_{ref} = \frac{180 - \frac{(180 - \beta)}{2}}{180} \tag{4-7}$$

Likewise, a 2nd order, low-pass filter (LPF) is used on the measured V_{output} to obtain the average value V_{avg}. V_{ref} is compared with the pu value of V_{avg}, changing the value accordingly (V_{dc}). V_{dc} is then fed through a PI controller (with proportional gain $Kp = 5$ and integral gain $Ki = 100$) to minimize the error over repetitive cycles (V_{Error}). This operation is theoretically defined by the equation (4-8) [49]:

$$\boldsymbol{V_{avg}} = \frac{\mathbf{1}}{\boldsymbol{\pi}} \int_{(\boldsymbol{\pi}-\boldsymbol{\beta})/2}^{(\boldsymbol{\pi}+\boldsymbol{\beta})/2} \boldsymbol{V_{output}} \, \mathbf{sin\omega t} \, \boldsymbol{d(\omega t)} = \frac{2}{\pi} V_{dc} \, sin(\frac{\beta}{2})$$

(4-8)

The synchronized triangular waveform, V_{tri}, is generated from the source sinusoidal waveform, V_{in}, and is then compared with V_{Error} in order to generate switching pulses.

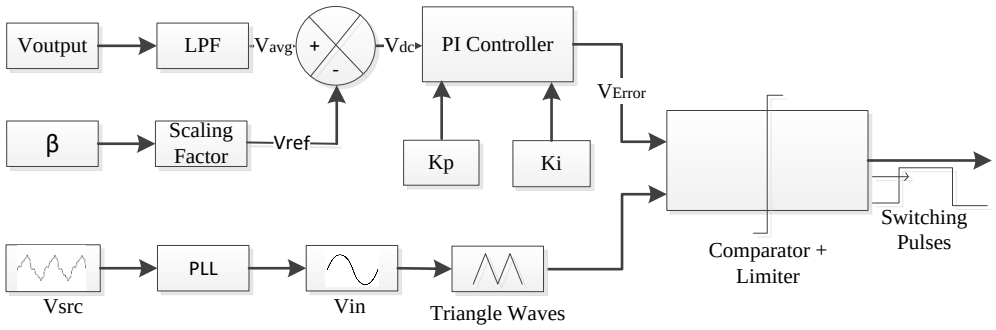


Figure 4.3-2: Algorithm for Symmetric Controller

The generation of V_{tri} is complex as compared to V_{saw},. as can be identified in the case of the Asymmetric Converter. PLL is used to derive the fundamental component V_{in} from V_{src}. Limiting this waveform between 0 and 1 creates the square wave for positive and negative cycles. Each wave is then integrated and limited separately resulting in a saw-tooth wave. Each saw-tooth wave is then inverted ('not') and minimized and maximized according to its original saw-tooth wave. Followed by this, the minimum of the original and inverted wave results in a triangular wave (V_{tri}) for positive and negative cycles. This can be seen in Fig. 4.3-3.

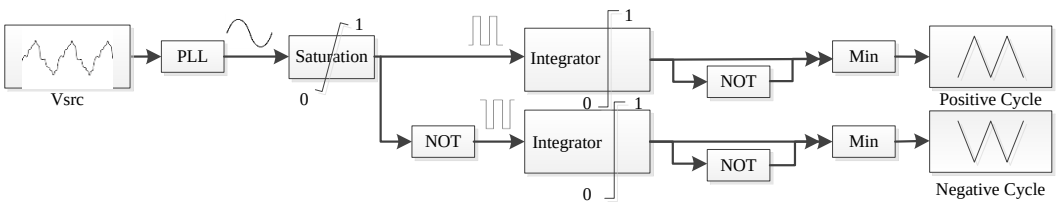


Figure 4.3-3: Algorithm for generating a Triangular Wave

4.3.3. Results

In conjunction to V_{in}, β plays an important role in determining the V_{output}. Fig. 4.3-4 shows the ideal behaviour of V_{output} based on the value of β which is determined by $V_{ref.}$ The variation of α provides a mean to compensate the variation of the output voltage due to the change of the load resistance, which can occur due to temperature change as discussed in section 3.2.2.

4.3.3.1. Output

Fig. 4.3-4a displays V_{in} from V_{src} and the corresponding triangular waveform for the positive and negative halves of the sinewave. These are then compared to the V_{ref} voltage to generate the firing pulses (Fig. 4.3-4b) for the positive half (in red) and the negative half (in blue). Fig. 4.3-4c shows the output voltage waveform (in pu) at the chosen conduction angle. As the V_{ref} magnitude is varied, the conduction angle can be controlled.

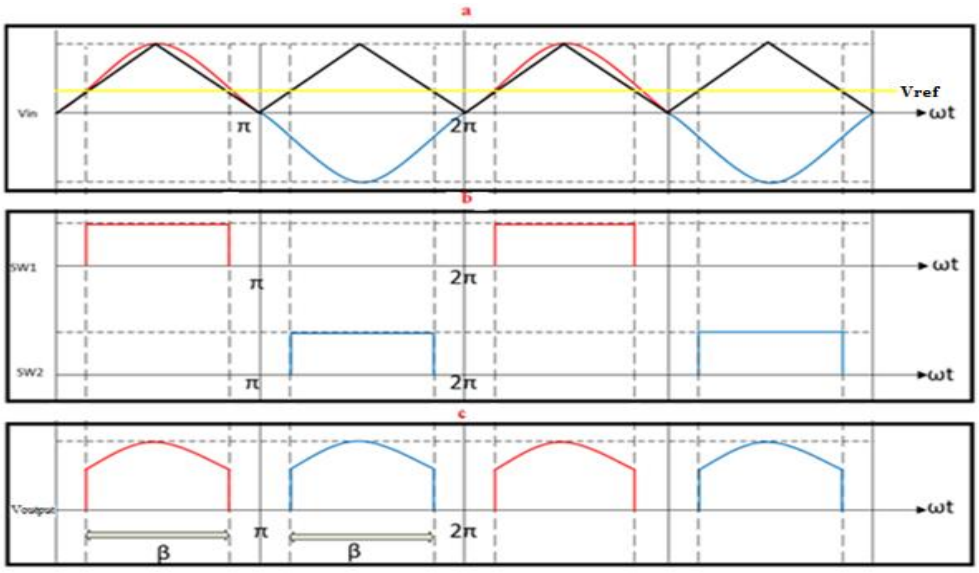


Figure 4.3-4: Expected Resulted Waveform

To compare the results, Fig. 4.3-5 to Fig 4.3-7 show the sampled waveforms at β = 150, 120 and 90 degs. using symmetric converter:

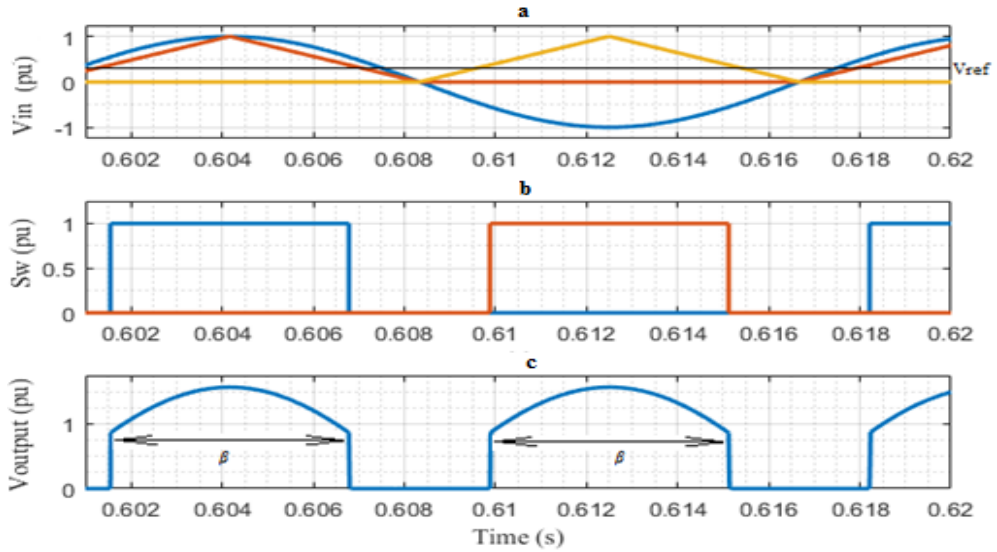


Figure 4.3-5: Sample Resulted Waveform at β = 150 degs.

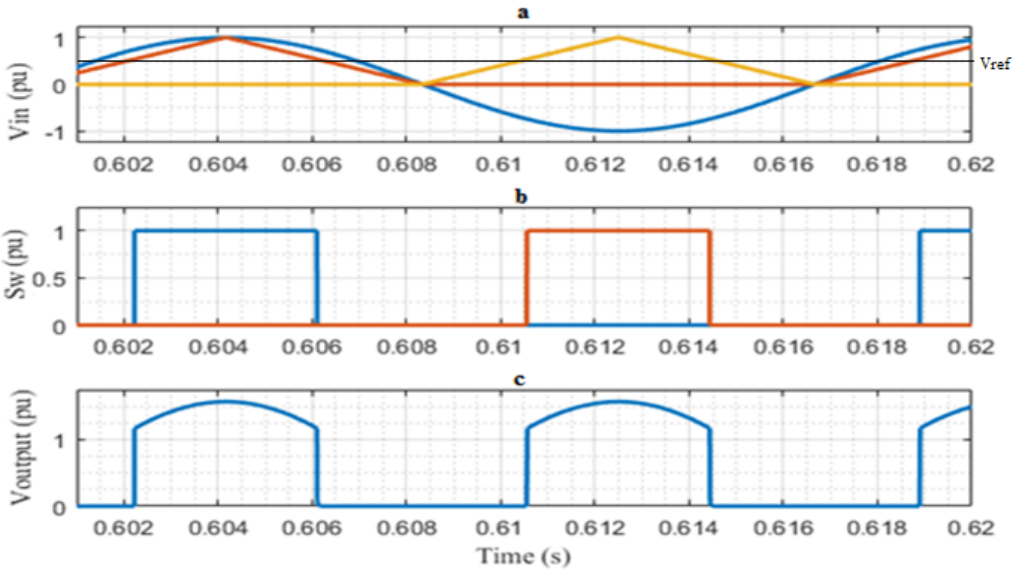


Figure 4.3-6: Sample Resulted Waveform at β = 120 degs.

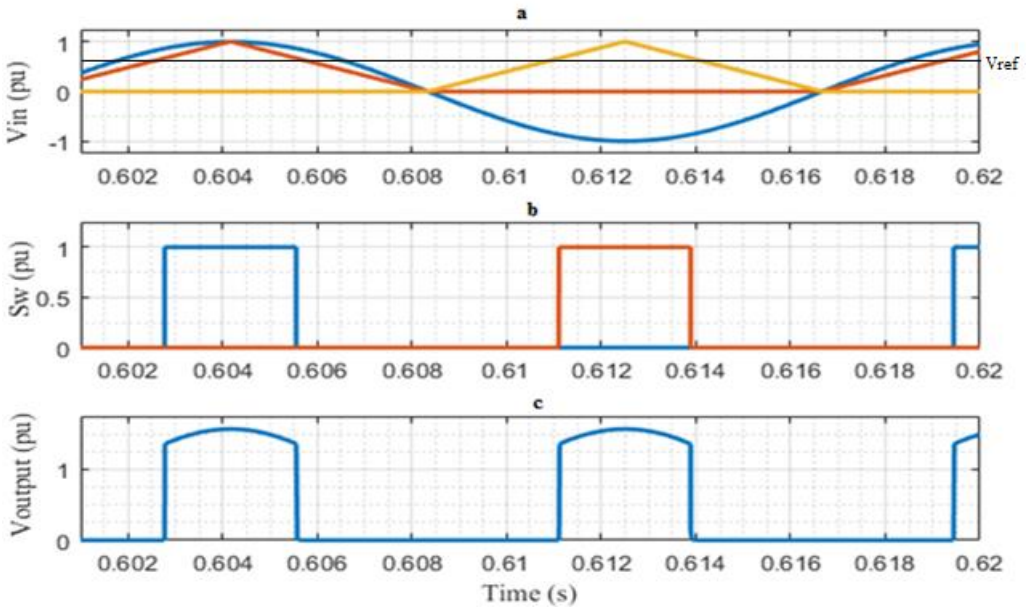


Figure 4.3-7: Sample Resulted Waveform at β = 90 degs.

Fig. 4.3-5a to 4.3-7a show the variation of V_{in} (in blue) and the corresponding triangular waveform for the positive (in red) and negative (in yellow), varying from a -1.0 pu to 1.0 pu versus time in seconds, varying from 0.602s to 0.62s. The sampling time chosen for Fig. 4.3-5a to Fig. 4.3-7a depict one complete cycle, and shows the V_{in} as compared to generated triangular waveform and V_{ref} (in black).

Furthermore, Fig. 4.3-5b to 4.3-7b display the variation of switching pulse for positive cycle (in blue) and for negative (in red) in pu, varying from a 0.0 pu to 1.0 pu versus time in seconds, varying from 0.602s to 0.620s. It is noticeable in these figures that the switching pulse rise and drop are determined by the intersection of V_{ref} and triangular waveform of positive and negative cycles.

Finally, Fig. 4.3-5c to 4.3-7c depict the variation of V_{output} in pu, varying from a 0.0 pu to 1.3 pu versus time in seconds, varying from 0.602s to 0.62s. V_{output} in sampled figures are displaying the relation between switching pulse and V_{in}. The width size of

V_{output} is same as the generated switching pulse, whereas its shape is determined by V_{in} in the range where switching pulse is on.

4.3.3.2. Power Factor (PF)

The relationship between PF angle and firing angle, β, is shown in Fig. 4.3-8:

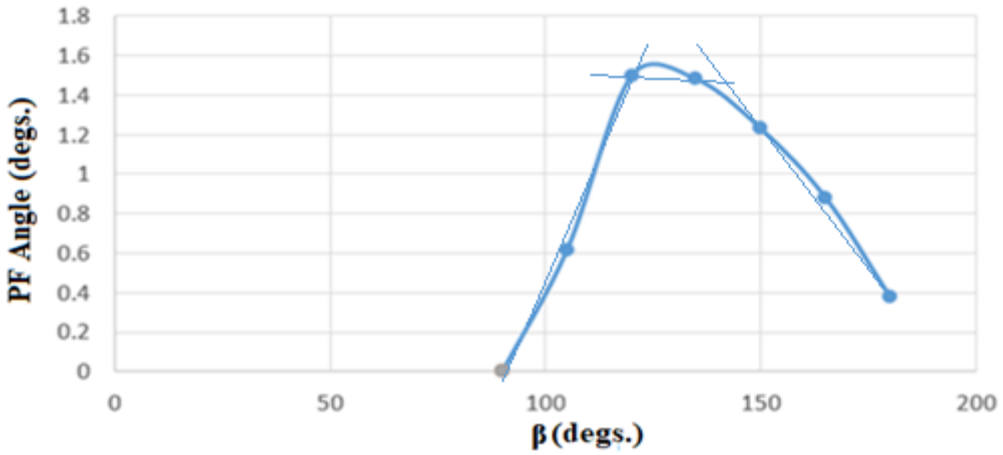


Figure 4.3-8: β versus PF comparison in Symmetric Converter

Fig. 24 displays the variation of PF angle in degs., varying from a 0 deg. to 1.8 degs. versus the β in degs., varying from 90 deg. to 180 degs.. Fig. 4.3-8 depicts that the PF angle changes very little (less than 2 degs.) with the conduction angle β and that is because the output voltage is symmetric with the input source sinewave. The maximum variation in PF angle is observed around the firing angle β = 90 +/- 10 degs.; this is attributed to the width of the firing pulse. It is noteworthy that at precisely β = 90 degs., the firing pulses are expected to disappear. So minimum values, using end stops, for the β angle are desirable.

4.3.3.3. Harmonics

Fig. 4.3-9 displays the harmonics without using PWM and filters at β = 150, 120 & 90 degs..

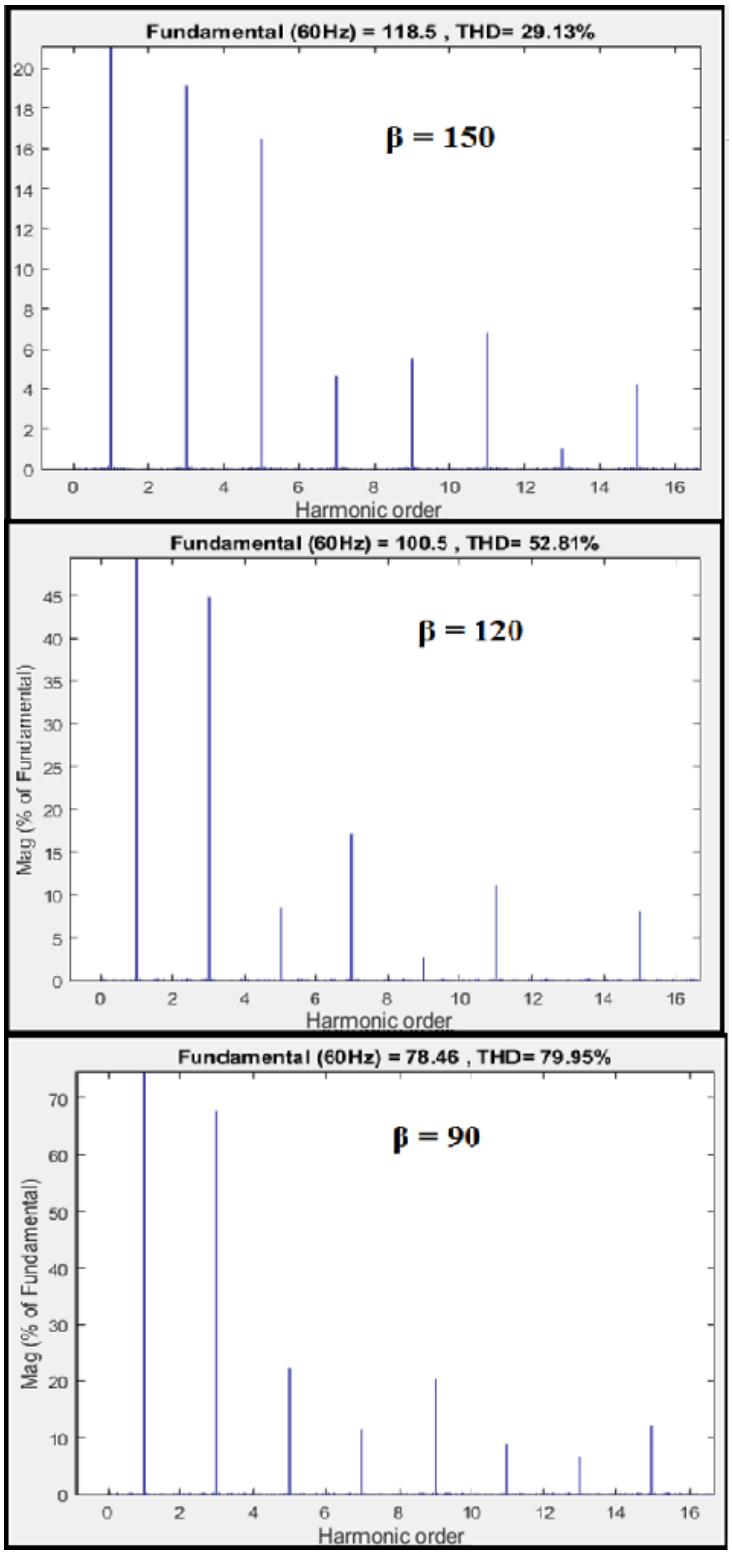


Figure 4.3-9: Harmonics Order at β = 150, 120 & 90 degs.

Fig. 4.3-9 depicts that harmonics are on odd harmonic order and well spread out from Harmonic order 3 (180 Hz) and onwards. Due to the fact that they are well spread out; filtering is not an easy and cost-effective task.

The relationship between THD and firing angle, β, is shown in Fig. 4.3-10:

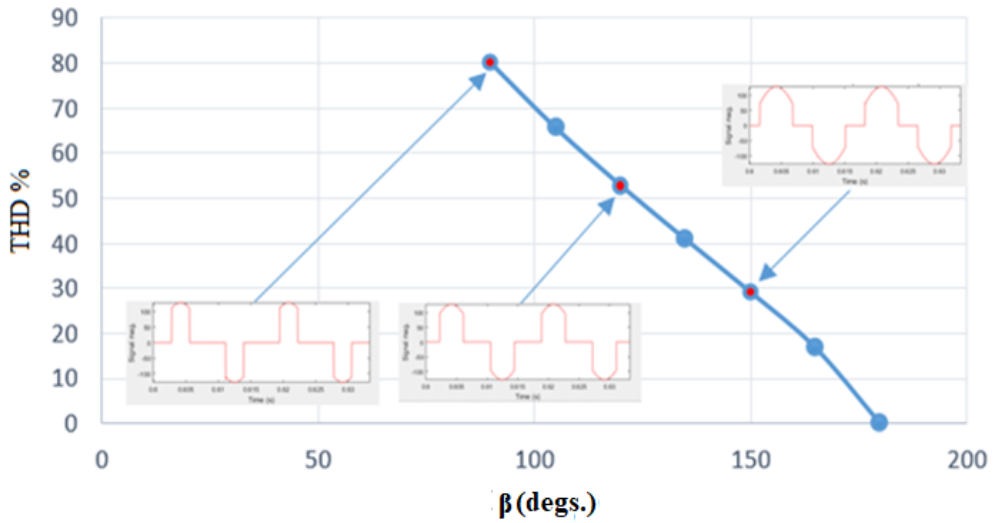


Figure 4.3-10: β versus THD comparison in Symmetric Converter

Fig. 4.3-10 shows the variation of THD in %, varying from a 0 % to 90 % versus the β in degs., varying from 90 deg. to 180 degs.. Fig. 4.3-10 displays that the waveform shape of the output voltage is similar to input current because of the closed loop. These current waveforms are symmetric (i.e. positive cycle has a similar shape as the negative cycle), and quadrant symmetric as well (i.e. start and end points are similar to the positive and negative cycles just like the output voltage). Thus, when the positive and negative cycle are combined and compared with a sinusoidal waveform, it can be noted that the shape of the waveform has an opening and ending gap that is determined by the β angle value (β represents the width range), which can vary from 180 degs. to 90 degs.. Also, as can be noticed, the quadrant asymmetric current shape is similar to V_{output} as can be seen at β = 150, 120 & 90 degs. in Fig 26. This causes the harmonics to increase because of

their asymmetry as compared to a normal sinusoidal waveform. Hence, Fig. 4.3-10 shows that the percentage of THD is increasing from 0% to almost 80% by decreasing the value of β between 180 to 90 degs..

4.4. Comparison & Conclusion

4.4.1. PF comparison between Asymmetric and Symmetric Converters

The PF angle comparison between Asymmetric and Symmetric converters is shown in Fig. 4.4-1:

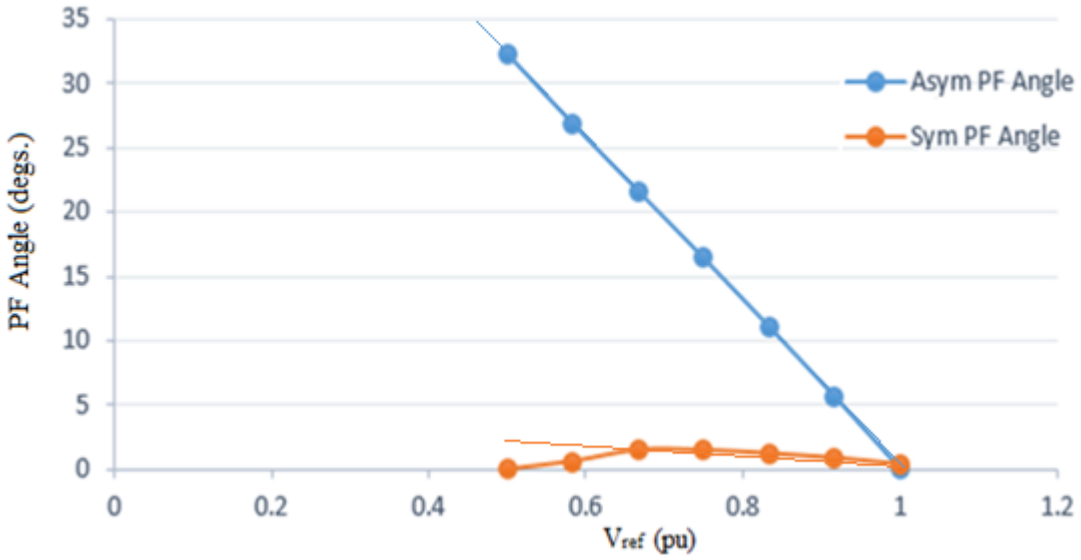


Figure 4.4-1: PF comparison between Asymmetric and Symmetric

Fig. 4.4-1 shows the variation of PF angle in degrees, varying from a 0 deg. to 35 degs. versus V_{ref} in pu, varying from 0.5 pu to 1.0 pu. There are two cases shown in this figure: Asymmetric PF in blue and Symmetric PF in orange. This figure depicts that PF angle of the Symmetric controller is much better than that of the Asymmetric controller over the whole operating range for V_{ref} ranging from 0.5 pu to 1 pu. As expected, in the case of the Symmetric converter the PF angle is always close to zero over the whole operating range. In the case of the Asymmetric converter, the PF angle varies as a

function of the $V_{ref,}$ dropping linearly from a high of about 80 degs. at V_{ref} of 0 pu to 0 degs. at a V_{ref} of 1 pu.

4.4.2. THD comparison between Asymmetric and Symmetric Converters

Fig. 4.4-2 shows the THD comparison between Asymmetric and Symmetric converters over their operating range:

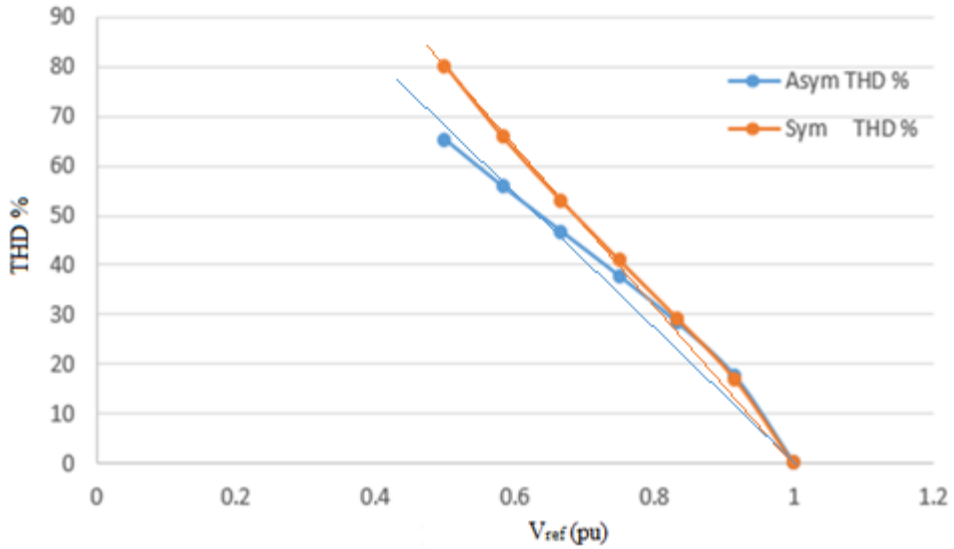


Figure 4.4-2: THD comparison between Asymmetric and Symmetric

Fig. 4.4-2 shows the variation of THD in %, varying from 0% to 80% versus V_{ref} in pu, varying from 0.5 pu to 1.0 pu. There are two cases shown in this figure: Asymmetric THD in blue and Symmetric THD in orange. It is noticeable in this figure that for a certain amount of V_{ref} (pu), the percentage change in THD follows a similar trend in both converters, although the actual magnitude of the THD is higher for the Symmetric converter from operating range 0-0.5 pu V_{ref}. This THD comparison is without the use of AC filters in both converters. However, the individual harmonics in the Symmetric converter are at higher frequencies which may be easier to filter out.

4.4.3. Conclusion

Through the comparison, it can be observed that by changing from an asymmetric to symmetric converter, one of the main goals of obtaining a better PF is achieved. The PF angle in the symmetric converter was close to 0 i.e. PF was much closer to unity, as desired. However, that was not the case for the THD. THD is slightly higher in the symmetric converter as compared to the asymmetric converter. This means that the system requires LPF to filter out individual harmonics so that the desired THD level can be achieved.

Additionally, with the possibility of using PWM techniques with the symmetric converter, the THD could be further reduced.

CHAPTER 5: MODULATION TECHNIQUE AND LPF in 1-PHASE MODEL FOR TESS

5.1. Introduction

As discussed in the chapter 4, THD is still problematic in the proposed design of 1-phase rectifier and its controller for TESS. It is necessary to have THD under 5% in-order for the rectifier to be integrated to a power grid effectively for TESS rated at 2 MW. However, just using LPF can be very costly due to the cost of high values of its inductance and capacitance in conjunction with rated power for TESS. Therefore, the aim is to reduce the size of LPF to a practical size by modifying the switching pattern and the converter's controller. To achieve such goal, PWM based switching pattern is to be implemented and investigated for the introduced TESS. In this chapter, PWM is applied and the results are verified showing the effect on the THD, and the LPF sizing.

5.2. Pulse Width Modulation (PWM)

5.2.1. Introduction to PWM

PWM waveform is defined by two main components: duty cycle (D) and switching frequency (f_s). A duty cycle is defined by the time at which the pulse is ON divided by the period (T_s) of the signal. The inverse of the switching frequency defines the period. In PWM control, the V_{output} is controlled by varying D [46].

In this instance, a 1-phase, half-controlled symmetric rectifier with VOC is being used, as can be seen in Chapter 4. By applying PWM on this converter, it is expected to have a controlled output voltage with a non-linear load, as the resistance of the load is expected to change with temperature. PWM can accomplish this with the help of IGBTs

by determining the frequency waveform of V_{output}. The average voltage V_{avg} can be described as:

$$V_{avg} = \left(\frac{1}{Ts}\right)\int_{t}^{t+Ts} V_{output}(t)dt \quad (5\text{-}1)$$

T_s here is the time period of the switching frequency (carrier frequency) while $V_{output}(t)$ represents the instantaneous voltage across a single-phase of a load. The requirement for a better and smoother control is to have a fixed switching frequency (f_s), higher than the fundamental frequency; however, it must be kept in mind that the switching losses of the converter's semiconductor devices determine the upper switching frequency.

Hence, the average value of voltage or current fed to the load is controlled by switching the active lower switches ON and OFF based on the switching frequency. Thus, the switching frequency should be higher than the line frequency [52].

5.2.2. Output with PWM

The task is to figure out a reasonable chopping (switching) frequency (N times the line frequency) to smoothen out the output. The choice of N determines the shift of the generated harmonics towards a higher order which may be easier to filter out.

The frequency that displays optimal results is 1020 Hz or N = 17 times fundamental (line) frequency (60 Hz) for switching. The results are shown below at β = 150, 120 and 90 degs. (β is defined in section 4.3.2) from Fig. 5.2-1 to Fig 5.2-3:

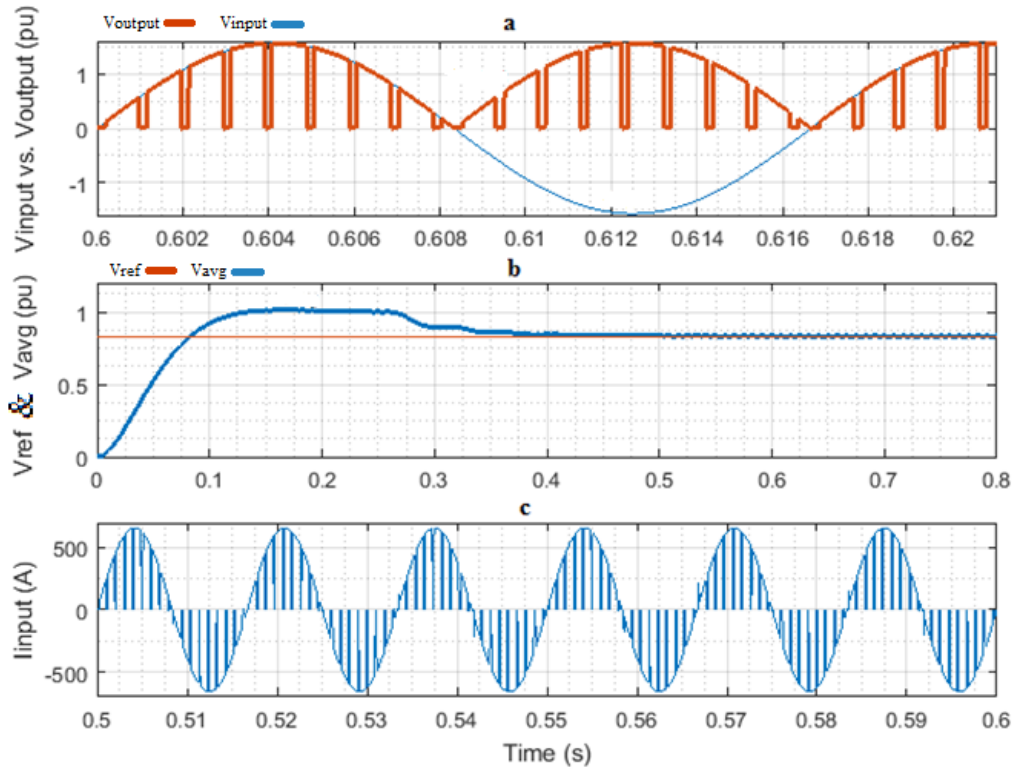


Figure 5.2-1: Sampled PWM Waveforms at V_{ref} = 0.833 pu (or β = 150 degs.)

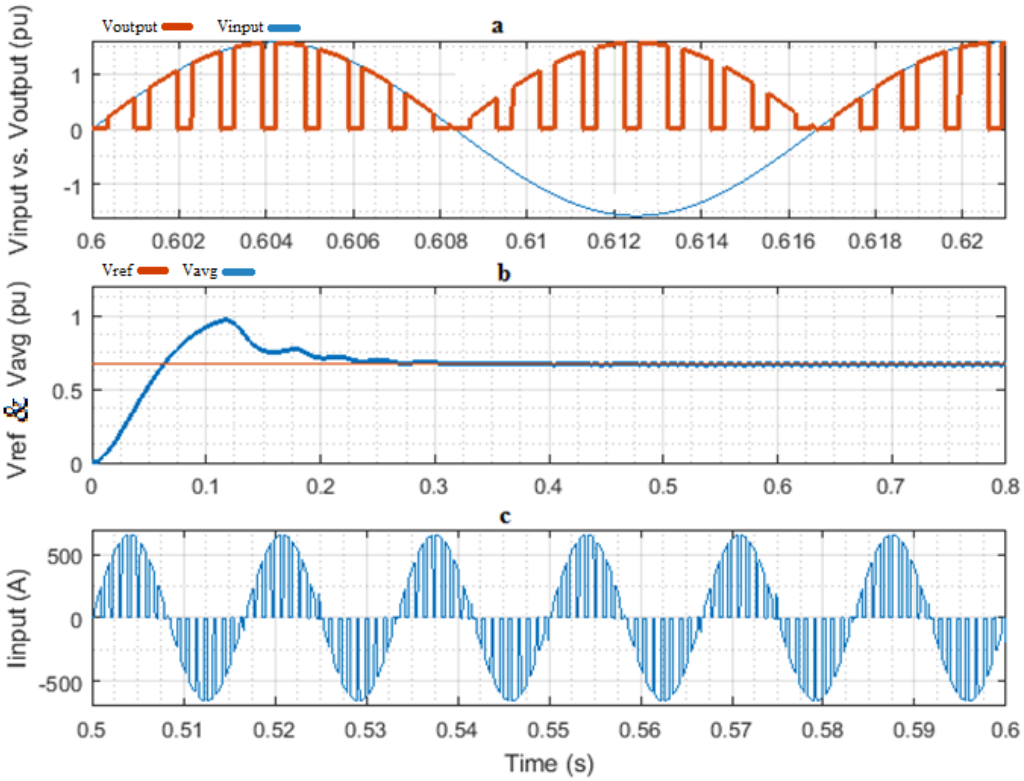


Figure 5.2-2: Sampled PWM Waves at V_{ref} = 0.667 pu (or β = 120 degs.)

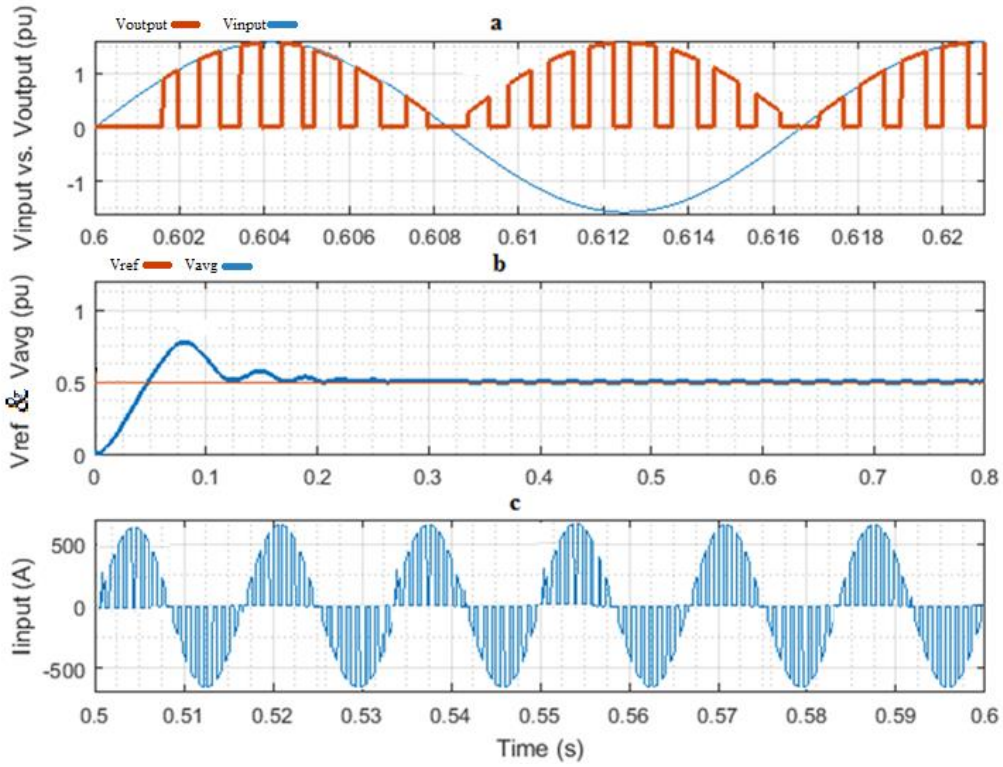


Figure 5.2-3: Sampled PWM Waves at V_{ref} = 0.5 pu (or β = 90 degs.)

Fig. 5.2-1a to 5.2-3a show the variation of V_{input} (in blue) vs. V_{output} (in orange), varying from a -1.5 pu to 1.5 pu time in seconds, varying from 0.6s to 0.62s. Sampling time chosen for Fig. 5.2-1a to Fig. 5.2-3a depict one complete cycle, which shows the behavior of V_{output} as compared to V_{input}; V_{output} and V_{input} shape look identical due to the chops in V_{output}, hence, displaying the effectiveness of the PWM.

Furthermore, Fig. 5.2-1b to 5.2-3b display the variation of V_{ref} (in orange) and V_{avg} (in blue) in pu, varying from a 0.0 pu to 1.0 pu versus time in seconds, varying from 0.0s to 0.8s. These figures verify the test response of the output of the controller with 0.8 seconds runtime. V_{avg} in this case needs to change according to V_{ref} in order to verify the dynamic performance of this converter. Since V_{avg} is accurately tracking V_{ref} in all three cases, it verifies the system's capability.

Lastly, Fig. 5.2-1c to 5.2-3c depicts the variation of I_{input} in Ampere, varying from a -550 A to 550 A versus time in seconds, varying from 0.5s to 0.6s. The input current waveform in these cases have a similar shape to sinusoidal waveform and they also looks similar to V_{output} for all three cases of β. This displays the connection of V_{output} and I_{input} in a close loop system, and further verifies the effectiveness of PWM.

5.2.3. Effects on Harmonics

Fig. 5.2-4 shows the shift of harmonics towards a higher order using PWM for three different conduction orders Beta = 150, 120 and 90 degs.; the main harmonics present after the fundamental harmonic (order 1) are mainly of order 13 (780 Hz) or above. Since the main harmonic frequencies are high, this allows the usage of a smaller LC filter, thereby making the system relatively cheaper than before.

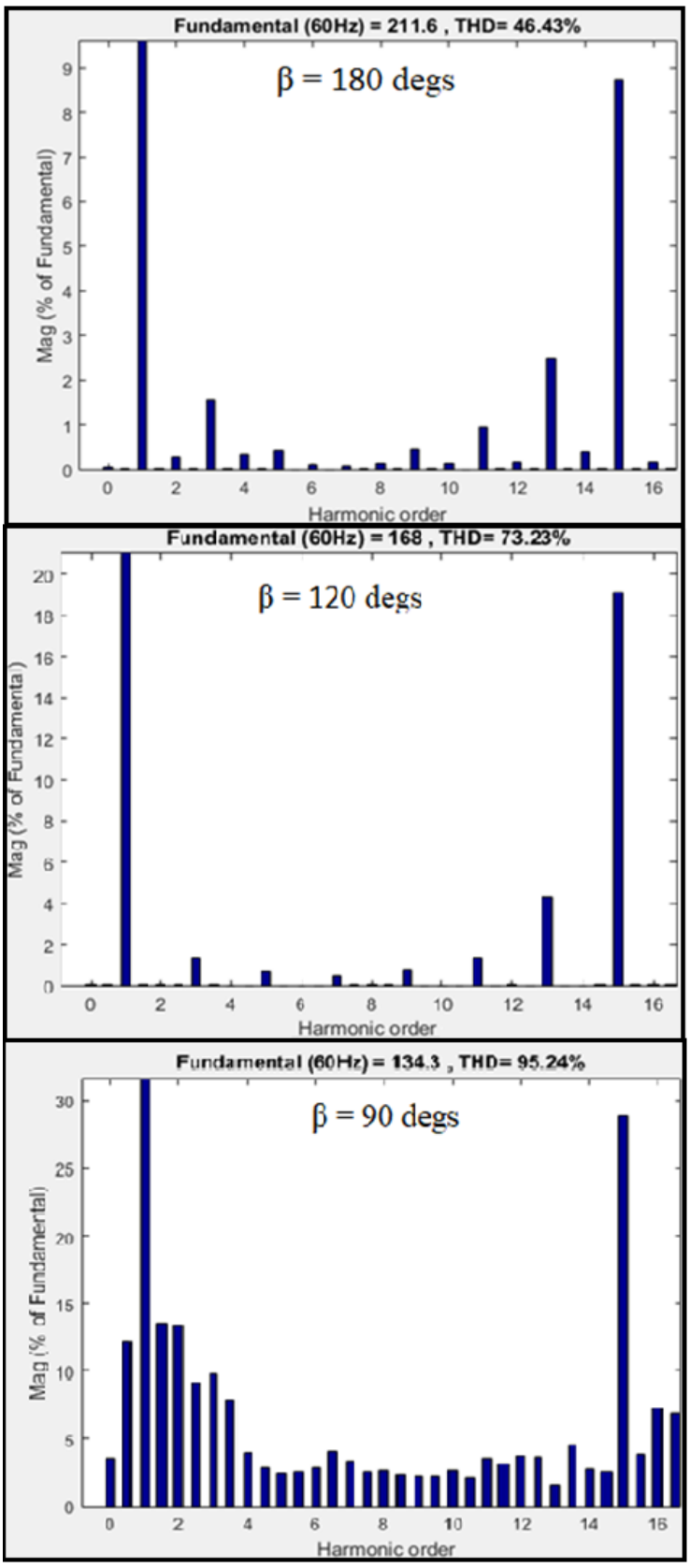


Figure 5.2-4: THD with PWM at β = 150, 120, 90 degs.

5.2.4. Conclusion

An analysis of these results shows that the PWM technique on the half-controlled 1-phase rectifier is still useful in shifting the harmonics towards a higher order. This is highly beneficial, despite the THD being higher, as it reduces the cost of the whole system, ultimately allowing the use of a smaller LC filter. However, the high magnitude of the THD is a negative for this type of converter.

5.3. Adding LPF with PWM in 1-Phase model

Fig. 5.3-1a shows diagrams of the 1-phase rectifier using IGBTs and voltage oriented controller with PWM in Fig. 5.3-1b.

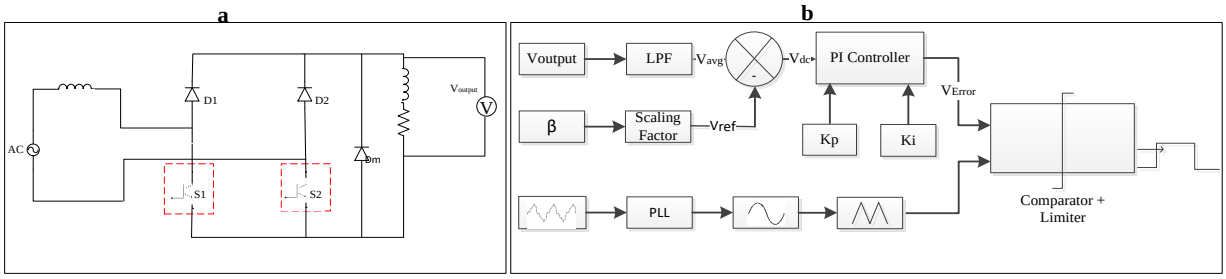


Figure 5.3-1: 1-Phase Rectifier and controller design with PWM

As discussed in section 5.2., implementing PWM into the controller for 1-phase rectifier shifts the harmonics to a higher frequency allowing the usage of a smaller LPF. A LPF can be utilized to remove harmonics, but it is important to ensure that the PF remains close to unity as the LPF can introduce a phase shift in the current leading to a reduction in the PF. Since it is a simple LPF (Fig. 5.3-2), it is much easier to design. The filter design is discussed next.

The value of the filter capacitor C is given by:

$$C = \frac{P}{(V^2)(2\pi f)}$$

(5-2)

Where,

P = Real Power (2 MW)
V = Voltage (1075V)
f = Fundamental Frequency (60 Hz)

To obtain the inductor value, the following formula is used:

$$L = \frac{1}{\left(2\pi f_{cutoff}\right)^2 C}$$

(5-3)

Where, f_{cutoff} = Cut-off Frequency (780Hz) as the harmonics shift to order 13 and above using PWM.

The transfer function for this filter is as follows:

$$G(s) = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} = \frac{(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2}$$

(5-4)

Where R is assumed to be the resistance of the wires, for which the value is set at 0.1 Ω. Another important factor that affects the designs of LPF is quality factor (Q) and damping ratio (ζ). Q represents the ratio stored in the oscillating resonator to energy dissipated per cycle by the damping process, as shown in equation (5-5). ζ shows whether the oscillating system is overdamped (i.e. ζ>1), underdamped (i.e. ζ<1) or critically damped (i.e. ζ=1). The relationship between Q and ζ is shown in equation (5-6):

$$Q = 2\pi f \frac{energy\ stored}{power\ loss}$$

(5-5)

Where,

$$Q = \frac{1}{2\zeta}$$

(5-6)

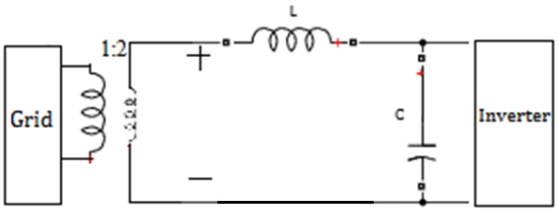


Figure 5.3-2: LC-LPF Design

The initial calculated values of LPF using the equation (5-2) and equation (5-3) are shown in Table 1, which represent the case of an overdamped system. Table 1 further shows the calculated values for L and C for other cases as well including underdamped and critical damped. Moreover, step response for each case is displayed in Fig. 5.3-3.

Table 1: L & C comparison with damping

Damping	**Q**	**ζ**	**L (µH)**	**C (µF)**	**R (Ω)**
Overdamped	0.44	1.12	9.07	4590	0.1
Critically damped	0.5	1	9.07	3620	0.1
Underdamped	0.77	0.33	40	1000	0.1

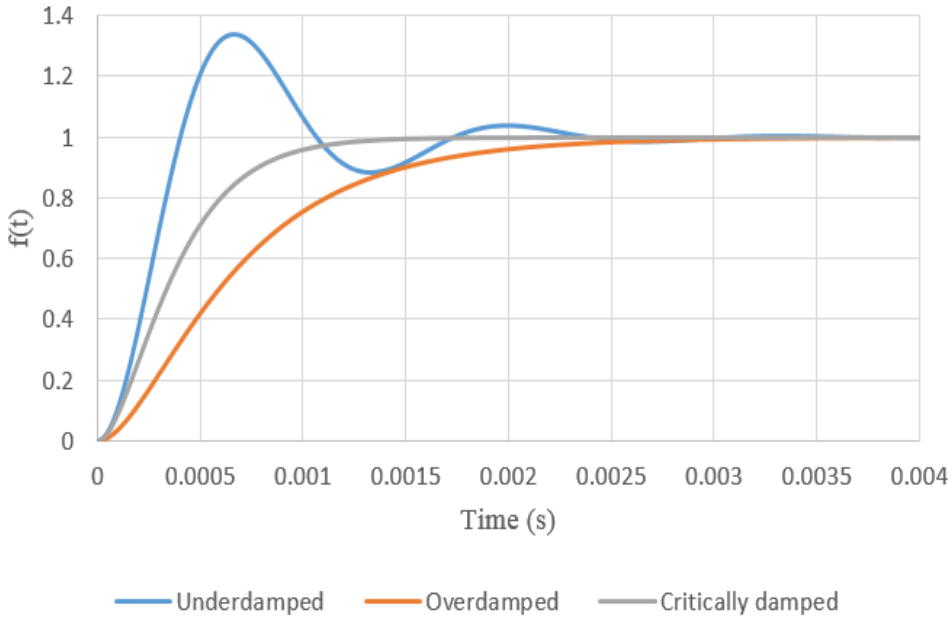


Figure 5.3-3: Transient Analysis

By observing the results in Fig. 5.3-3, it can be seen that the best response is the critically damped response. Therefore, to obtain a stable LPF result, the value for C = 3620 µF and L = 9.07 µH should be used which can be obtained by changing ζ at 1 and Q at 0.5. With this fine-tuning, the system does not oscillate and provides a rapid response.

5.3.1. Input THD and PF

By applying the adjusted filter, the changes in THD for three different β values at 150, 120 and 90 degs. can be seen in Fig. 5.3-4. The changes in THD vs. β are marginal.

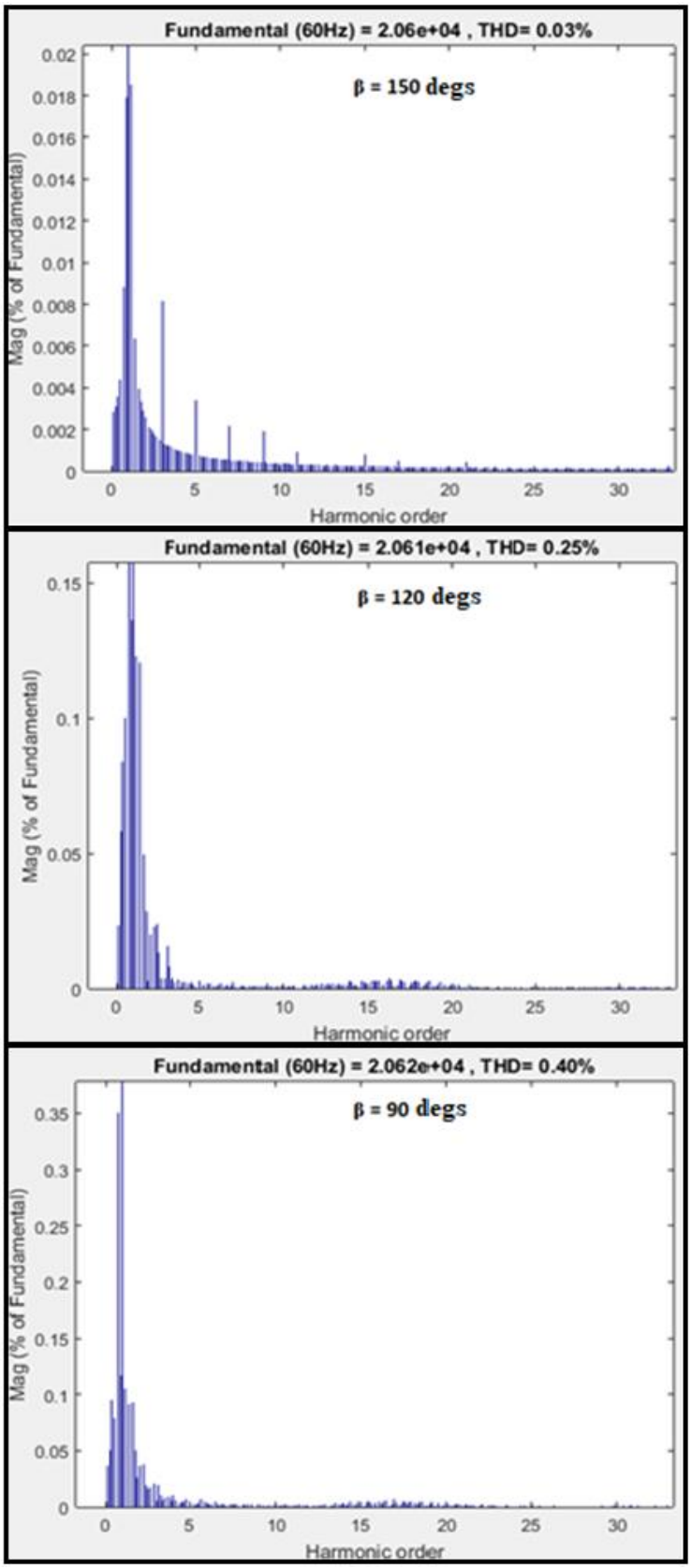


Figure 5.3-4: Harmonics with PWM and LPF at β = 150, 120 and 90 degs.

Fig. 5.3-4 shows that the THD for critically damped LPF at β values 150, 120 and 90 degs. works reasonably well with an increase in THD from 0.03% to 0.40%, with decreasing values of β from 150 degs. to 90 degs. respectively.

The changes for the PF vs. β can be seen in Fig. 5.3-5. It can be seen that there is almost a linear relationship between PF and β.

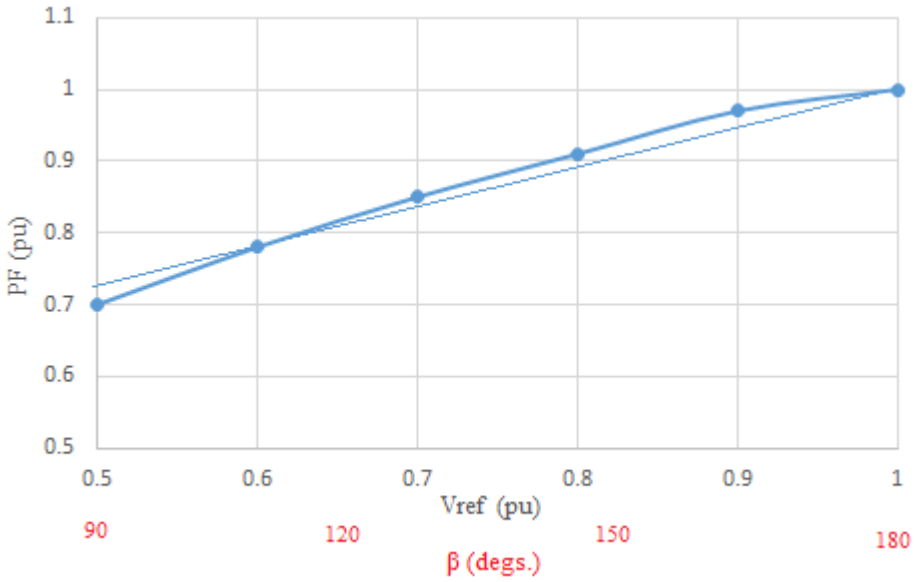


Figure 5.3-5: PF with LPF and PWM

Fig. 5.3-5 shows the variation of PF in pu, varying from a 0.55 pu to 1.00 pu versus β in degs., varying from 90 degs. to 180 degs.. The PF original characteristic shows that PF varies linearly with β from point [0.66, 90°] to point [1, 180°], with a positive slope of [0.00367 pu/deg.], however, this slope can be improved further with some adjustments in the LPF.

Furthermore, values for L and C can be further reduced as well for LPF to be more cost-effective while keeping LPF critically damped. Therefore, critically damped LC-LPF is not yet the most optimal filter and can be tuned further.

The aim for LPF design is that it needs to provide THD under 5% and PF close to unity, while keeping the ζ at 1 and Q at 0.5 (critically damped) and altering L and C values. Therefore, after many repetitions the most optimal L and C values found to be 4.5 µH and 450 µF. THD for the chosen LPF at three different β values 150, 120 and 90 degs. is shown by Fig. 5.3-6 followed by the PF in Fig. 5.3-7.

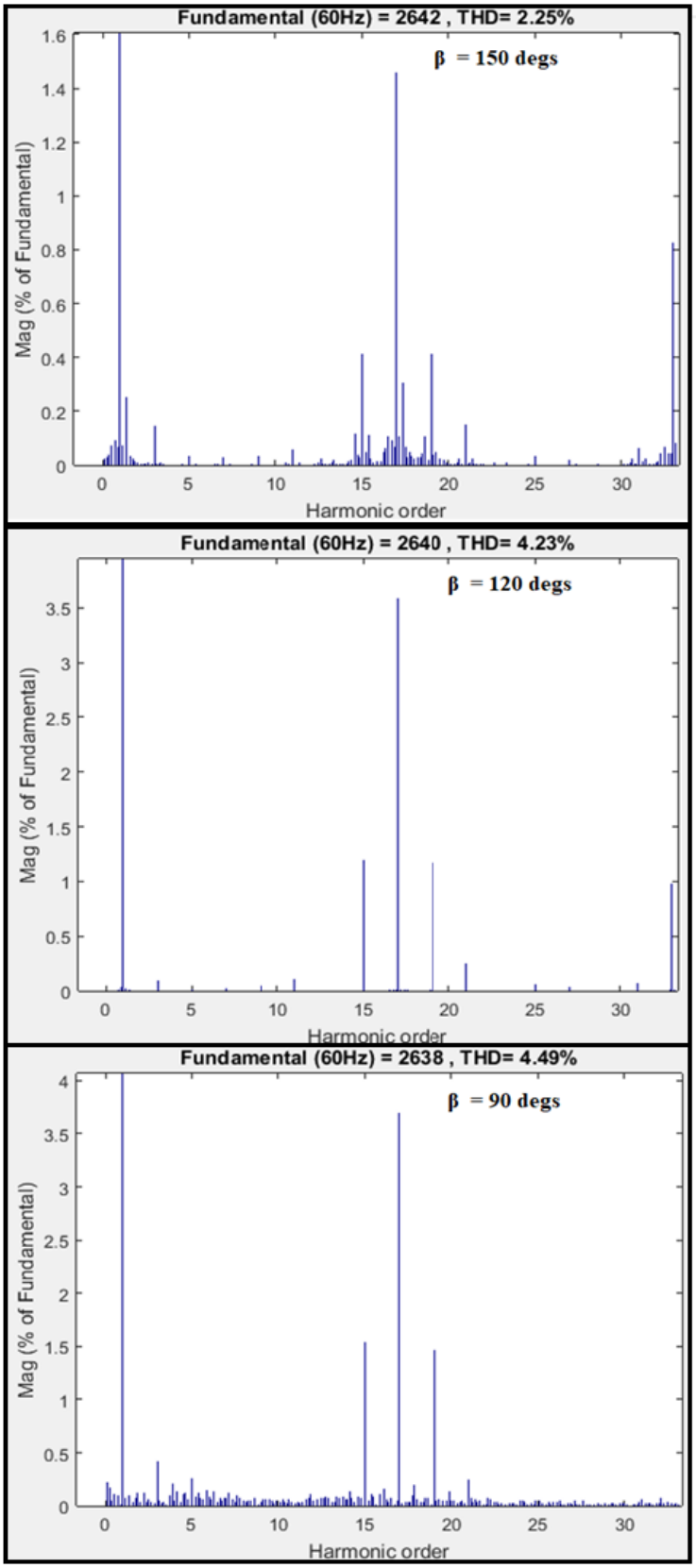


Figure 5.3-6: Harmonics with PWM and LPF at β = 150, 120 and 90 degs.

Fig. 5.3-6 displays that THD has increased for all three cases (β = 150, 120 and 90 degs.), but still meets the THD requirements (i.e. THD < 5%). Therefore, this is an acceptable result.

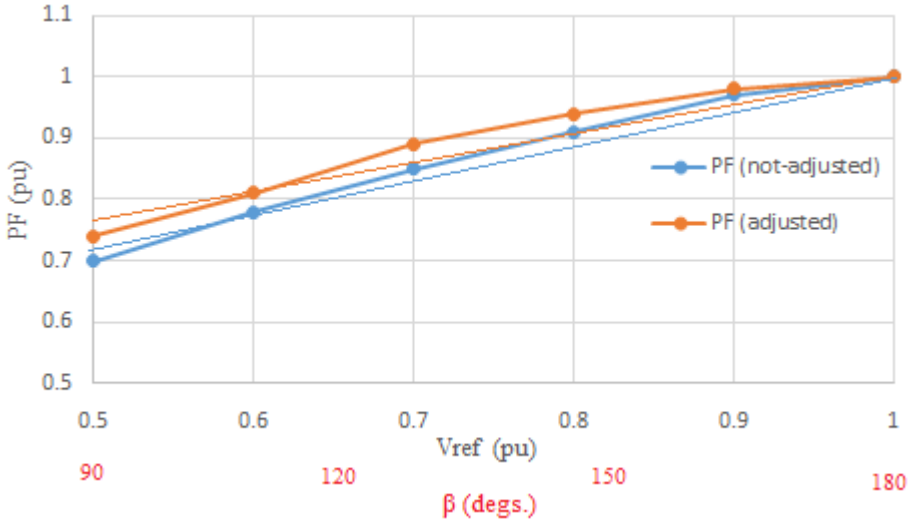


Figure 5.3-7: PF with LPF and PWM

Fig. 5.3-7 displays the variation of PF in pu, varying from a 0.55 pu to 1.00 pu versus β in degs., varying from 90 degs. to 180 degs.. There are two cases shown in this figure: PF (Critically Damped (not adjusted) in blue and PF (Critically Damped (optimally adjusted)) in orange. Fig. 5.3-7 verifies that the PF in optimally adjusted LPF has improved as compared to before (not adjusted LPF) with a steeper slope of [0.00375 pu/deg.] and a higher starting point 0.725 pu at β = 90 degs.. This helps in reducing L and C value in LPF (L is reduced by 2 times and C is reduced by 8 times). Therefore, this solution is more optimal and cost-effective.

5.3.2. Conclusion

As can be observed, the THD has improved by applying LPF and meets the requirement for being under 5% for β from 180 degs. to 90 degs.. However, it can be noticed that LC-LPF also affects the PF as predicted previously. Even though PF is being

affected, it is within the feasible range for most of the β values and can handle the change within the load or the voltage. Thus, this system is stable, not complex and a cost-effective solution. It can be utilized and maintained easily for heating purposes for 1-phase rectifier in proposed TESS design.

CHAPTER 6: 3-PHASE RECTIFIER AND CONTROLLING TECHNIQUES

6.1. Introduction to 3-Phase Converter

In this chapter, the design of a 3-phase rectifier for TESS using the PWM modulation technique is compared with a 3-phase converter using the popular VICC controller.

6.2. Symmetric Half-Bridge Controlled 3-Phase Rectifier

Following the 1-phase symmetric model described earlier (section 5.3), a 3-phase version (Fig. 6.2-1) is designed. Fig. 6.2-1 depicts the half-bridge IGBT-based, force-commutated symmetric converter rated at 2 MW. Using a 2.15 kV PCC bus voltage, this converter is fed from 1.07 kV source with the help of a transformer and feeding a resistive load of 2.3 Ω per phase (total = 6.9 Ω per converter). The converter is composed of three diodes D1, D2, and D3 as well as three controlled IGBT switches S1, S2 and S3, in addition to a freewheeling diode, D_m, connected across the load to cope with the inductive load.

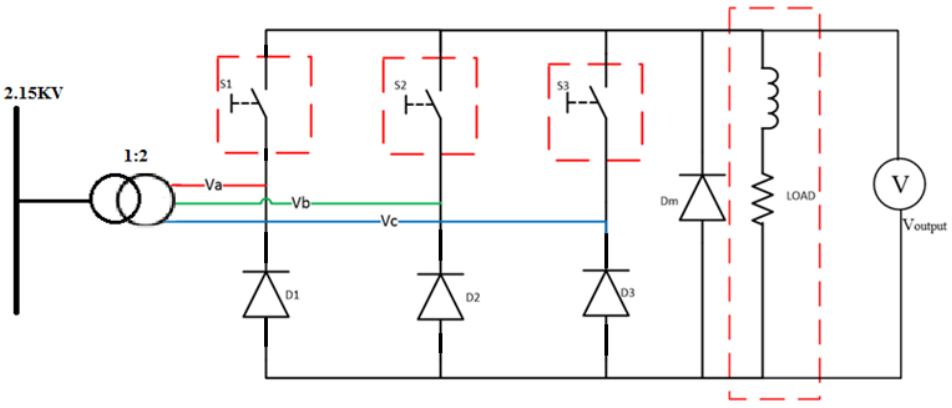


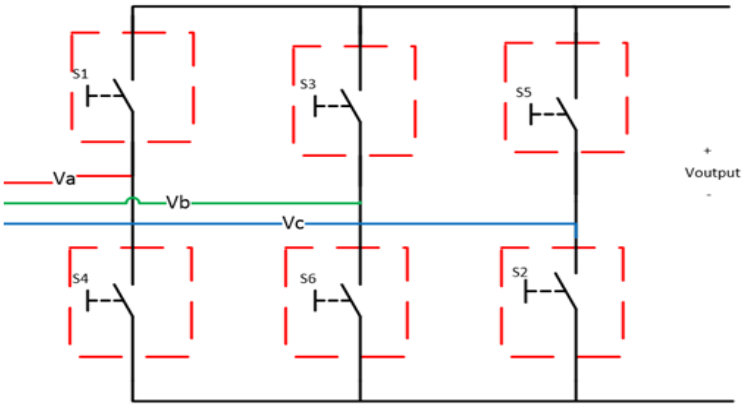
Figure 6.2-1: Half Bridge Controlled 3-Phase Rectifier

6.2.1. Half-Bridge Controlled 3-Phase Symmetric Converter

The challenge with the half-bridge controlled 3-phase symmetric converter, controlled by 3 switches, is that each switch must be controlled to a specified conduction angle value. This poses a challenge because each switch has a limited conduction angle operating range to ensure an effective performance.

A fully-controlled, 3-phase converter is comprised of all six IGBT switches, as opposed to 3 diodes and 3 IGBT switches for a half-bridge-controlled converter. The switching sequence for the fully controlled converter is shown in Fig. 6.2-2, which shows that one pair of switches work in unison at different angles, i.e. S1& S2, S3 & S4 or S5 & S6. However, it is also noted that switches S1 & S4, S3 & S6 or S5 & S2 cannot be ON simultaneously, otherwise a short circuit will occur.

In a half-bridge controlled 3-phase converter (Fig. 6.2-1), the conducting states of the three diodes can only be determined by voltage differences in each phase. Hence, only a limited controlling range is available. To further understand this, the first step is to analyze the general 3-phase input waveform in Fig. 6.2-3.



Switch no.	Switching Angles (deg)
1	0-120
2	60-180
3	120 -240
4	180-300
5	240-360
6	300-0-60

Figure 6.2-2: Full control 3-Phase Rectifier with switching angles

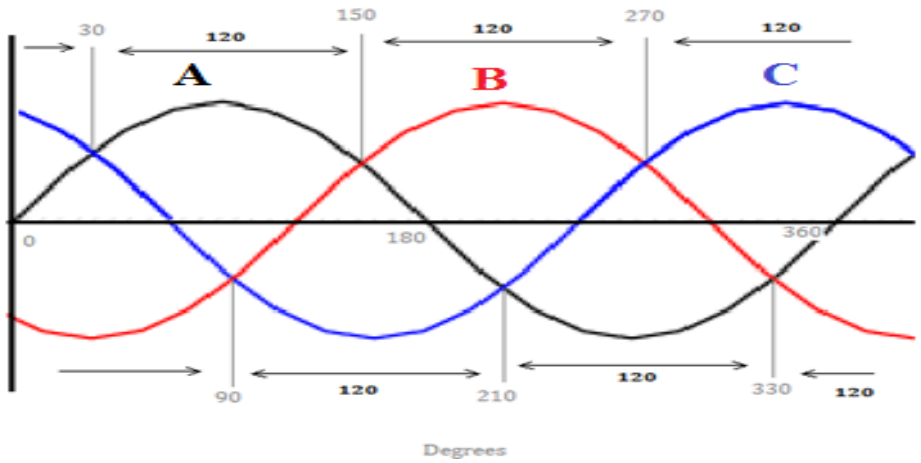


Figure 6.2-3:3-Phase Input Waveform

Since the IGBTs are only on the top side of the bridge, only the positive side of each waveform can be controlled. As seen in Fig.6.2-3, between each of the 3-phases there is a 120 degs. delay before each phase crosses another phase. For Phase A, for example, the operating range starts from angle 30 degs. to 150 degs.. And because of the symmetry of the sinewave form, this period is centered at 90 degs. making it possible to divide the period in to 60 degs. before and 60 degs. after the center line. Similarly, the same period in Phases B and C starts from 150 degs. to 270 degs. and 270 to 30 degs. respectively. Hence, Switch S1 can be coupled with Phase A waveform, switch S2 can be coupled with Phase B waveform and similarly Phase C waveform can be coupled with switch S3. To ensure that each switch deals only with the assigned phase, each phase waveform the operating range is limited to the defined ranges above.

During this duration, a square pulse is created for each phase and then chopped up to 17 times in-order to increase the switching frequency to 1020 Hz. Each of these chops are then converted to triangles, so that when compared with a constant reference, they can produce controllable switching pulses for each phase. Fig. 6.2-4 shows a controller for this rectifier.

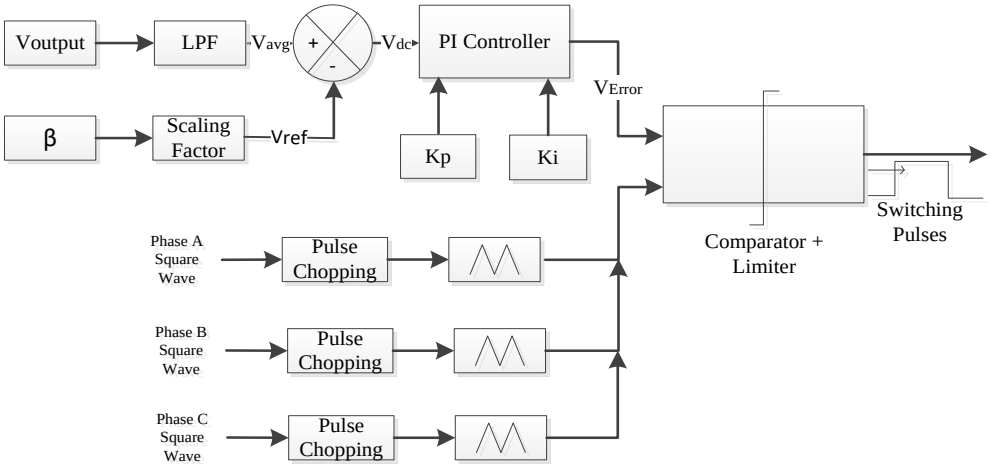


Figure 6.2-4: 3 - Phase Symmetric Conduction Angle Controller

As shown in Fig. *6.2-4*, the inputs are V_{output} which is sensed from the load, and β is the reference conduction angle which is set manually. V_{ref} is produced using conduction angle β by multiplying with a scaling factor. Likewise, a second order filter LPF is applied to the measured V_{output} to obtain its average value, V_{avg}. *Then,* V_{ref} is compared with V_{avg}, and the difference is then fed through a PI controller (with proportional gain K_p = 5 and integral gain K_i = 100). This step serves to minimize the error over repetitive cycles (V_{Error}). The synchronized triangular waveform, V_{tri}, is generated from the calculated chopped pulses and is then compared with V_{Error} to generate switching pulses for each switch.

For the filter, the most optimum L and C values were found to be 2 mH and 2000 μF, resulting in a critically damped circuit. This filter LPF is too costly due to the large capacitance value as compared to some other solutions available.

6.2.2. Results

Fig. 6.2-5 shows the test response of the output of the controller V_{avg} to a step change in the V_{ref} (V_{ref} = 1 pu to V_{ref} = 0.5 pu) implemented at 0.7 seconds. This test

verifies the dynamic performance of the 3-phase half-bridge converter. The simulation duration is 1.2 seconds.

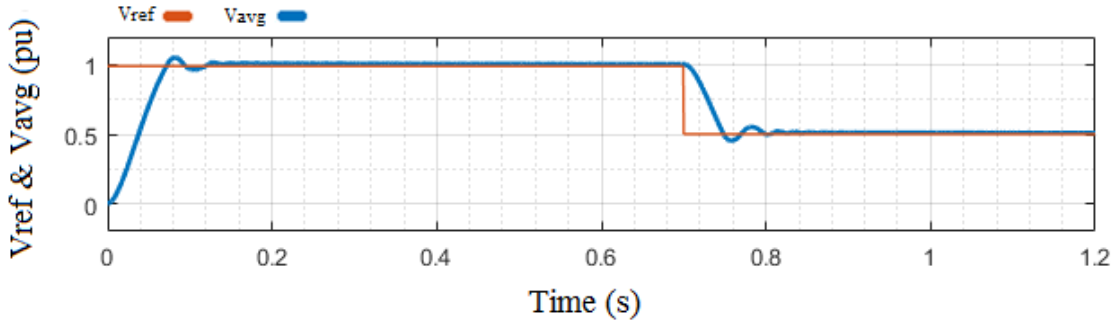


Figure 6.2-5: Step Change in V_{ref} from 1 pu to 0.5 pu

Fig. 6.2-5 shows the comparative variation of V_{ref} and V_{avg} in pu, varying from a 0.0 pu to 1.0 pu versus time in seconds, varying from 0.0s to 1.2s. This figure shows V_{ref} in orange and V_{avg} in blue. The initialisation is controlled and the V_{avg} reaches the steady state value within 0.1s. A step change is applied at 0.7s to reduce V_{ref} from 1.0 pu to 0.5 pu. Fig. 6.2-5 verifies that the controllers follow the step change closely and in a stable manner. Therefore, this confirms the 3-phase half-bridge converter's dynamic performance.

To further verify that the converter is performing as expected, some other results of the 3-phase half-bridge converter are examined in Fig. 6.2-6 to Fig. 6.2-8 for three different values of the reference voltage V_{ref} = 0.833, 0.633 and 0.5 pu (which are also equivalent to conduction angles β = 150, 120 and 90 degs. respectively) (Relationship between V_{ref} and β is defined in section 4.3.2)).

Initially, the V_{output}, is displayed by Fig. 6.2-6a to Fig. 6.2-8a for which a shorter sampling time is taken to observe its shape properly. Following that, Fig. 6.2-6b to Fig.

6.2-8b shows the response of the output of the controller V_{ref} and V_{avg} for 0 – 0.4 s seconds of simulated time for each β case. Finally, Fig. 6.2-6c to Fig. 6.2-8c shows the Phase A input voltage (V_a) and current (I_a) to verify their shape and phase change.

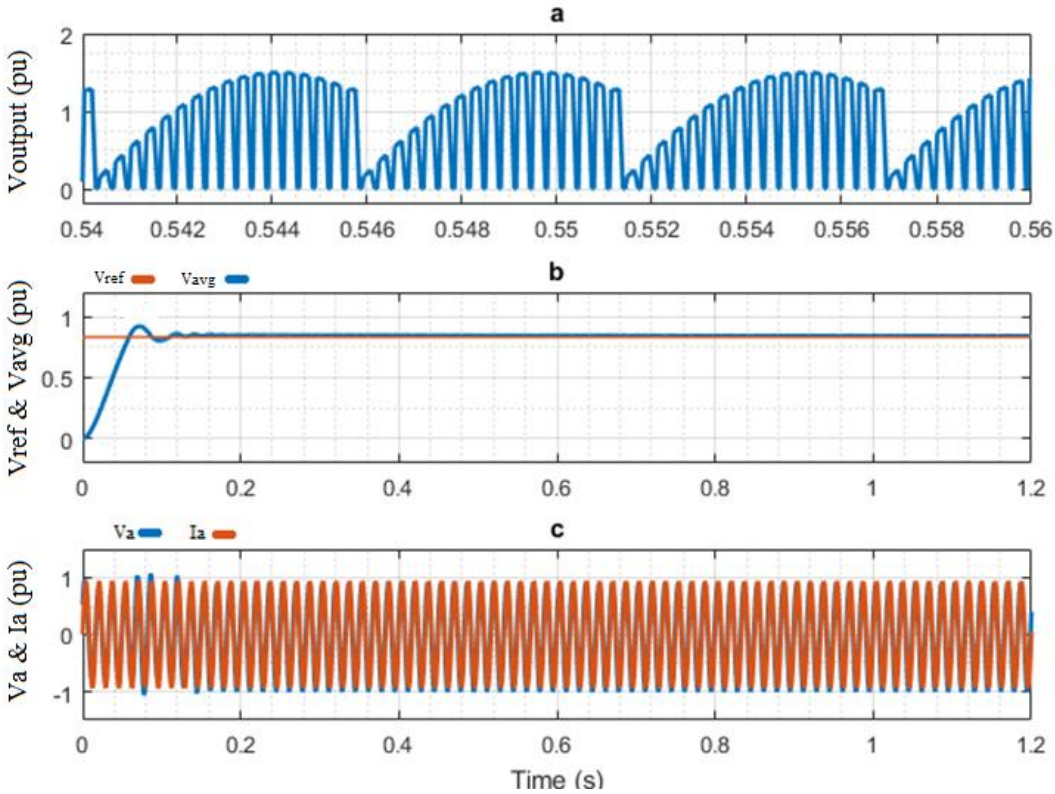


Figure 6.2-6: Half-Bridge Converter Input and Output at V_{ref} = 0.833 pu (or β = 150 degs.)

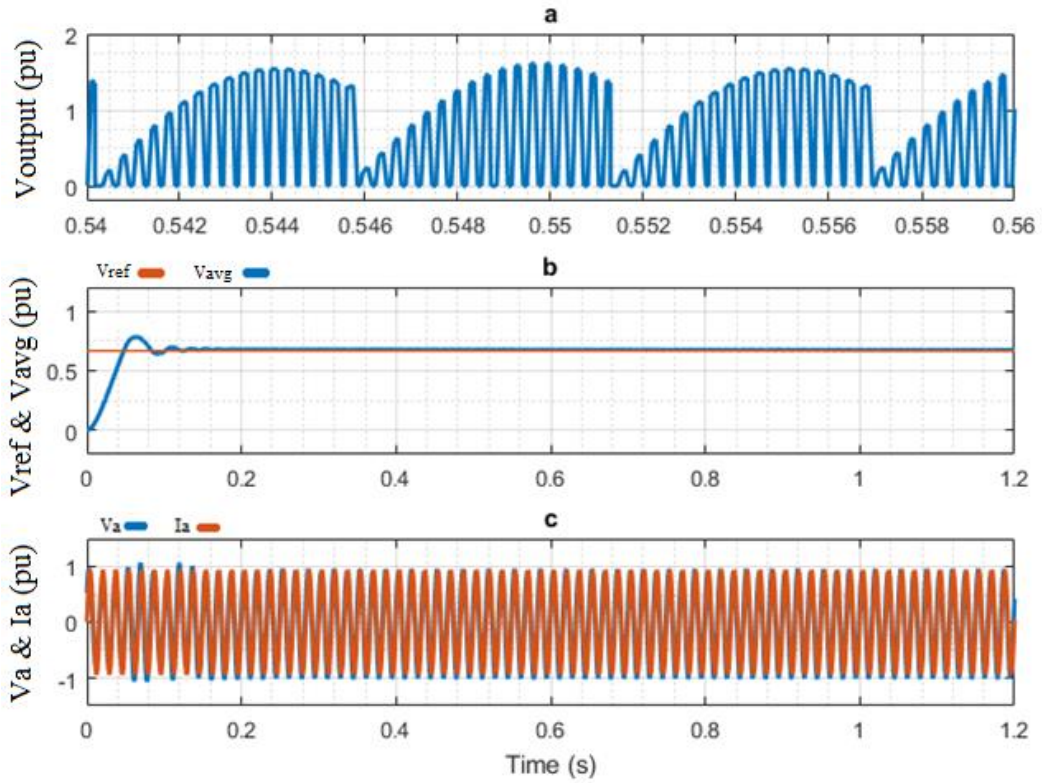


Figure 6.2-7: Half-Bridge Converter Input and Output at V_{ref} = 0.667 pu (or β = 120 degs.)

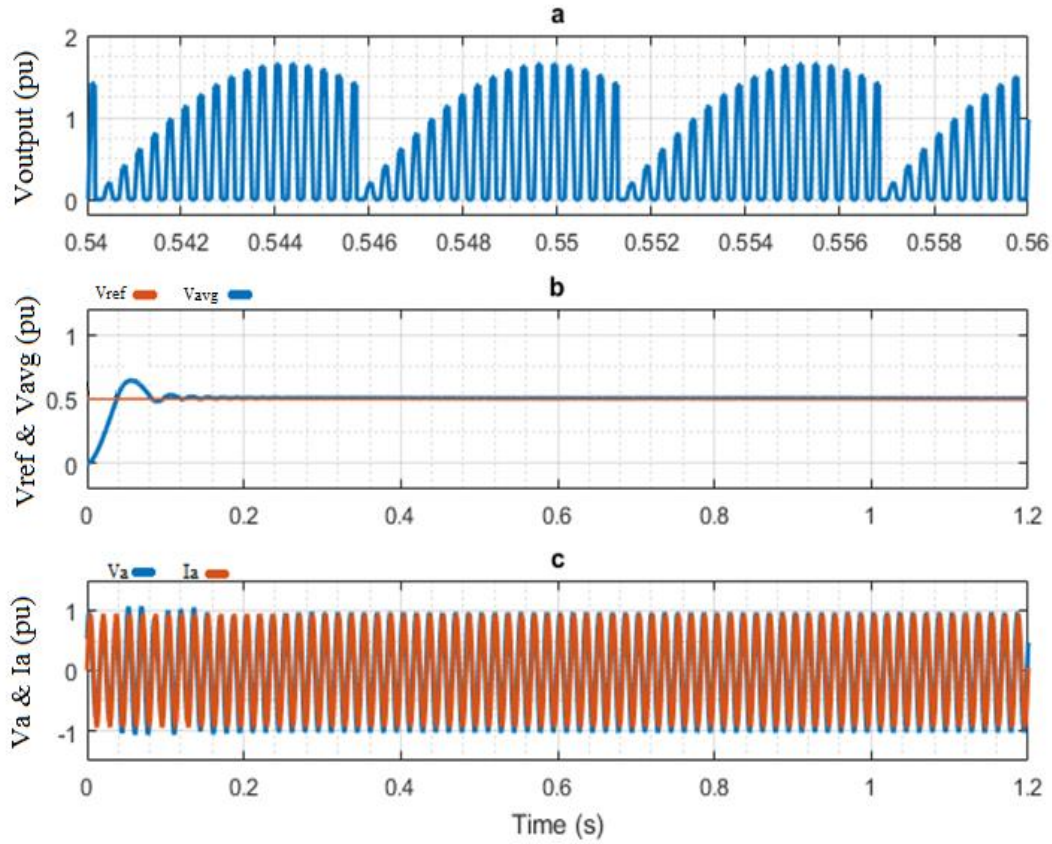


Figure 6.2-8: Half-Bridge Converter Input and Output at V_{ref} = 0.5 pu (or β = 90 degs.)

Fig. 6.2-6a to 6.2-8a depict the variation of V_{output} in pu, varying from a 0.0 pu to 2.0 pu versus time in seconds, varying from 0.54s to 0.56s. The behavior of V_{output}, in this case appears to be asymmetric with symmetric chops. The V_{output} shown in this figure is designed based on line to neutral voltage, where switching operational range is 120 degs. per switch. Each switch handles one phase, thereby limiting the duration of a phase since a full cycle per phase is 180 degs.. Therefore, the shown V_{output} behavior confirms that it is working as expected.

The V_{output} shape could be corrected to a symmetric shape by shifting the switching square waves by 30 degs.; however, this causes a shift in input current and voltage of the designed model, thereby affecting negatively the PF (displayed in Fig. 6.2-10). Therefore, shape was left as asymmetric.

Fig. 6.2-6b to 6.2-8b show the variation of V_{ref} (in orange) and V_{avg} (in blue) in pu, varying from a 0.0 pu to 1.0 pu versus time in seconds, varying from 0.0s to 1.2s. These figures verify the test response of the output of the controller in which V_{avg} needs to change according to the V_{ref} in order to verify the dynamic performance of the 3-phase half-bridge converter. Since V_{avg} is accurately tracking V_{ref} in all three cases, it verifies the system's capability. This was also shown earlier in Fig. 6.2-5. However, now the values of the V_{ref} have been changed to 0.833, 0.667 and 0.5 pu respectively. The three tests indicate that the dynamic response varies with the V_{ref} settings, meaning that the controller gains are not optimal at all values of the V_{ref}.

Fig. 6.2-6c to 6.2-8c display the variation of V_a (in blue) & I_a (in orange) in pu, varying from a -1.0 pu to 1.0 pu versus time in seconds, varying from 0.0s to 1.2s. The input voltage (V_a) and current (I_a) waveforms appear to be sinusoidal for all three cases of

V_{ref} (or β). Furthermore, V_a and I_a do not have a significant phase shift in between them as can be seen in these figures which implies that the designed LPF is working properly. Therefore, LPF can be used to lower the THD, which needs to be kept under 5% as per the standard requirement of the power grid. Additionally, it also displays that despite the V_{output} being asymmetric in a close loop system, its LPF is rigid enough to correct input current shape as desired.

Fig. 6.2-9 show the THD requirement for the power grid is below 5% for β at 150, 120 and 90 degs: i.e. THD = 4.31%, 3.46% and 2.61% respectively.

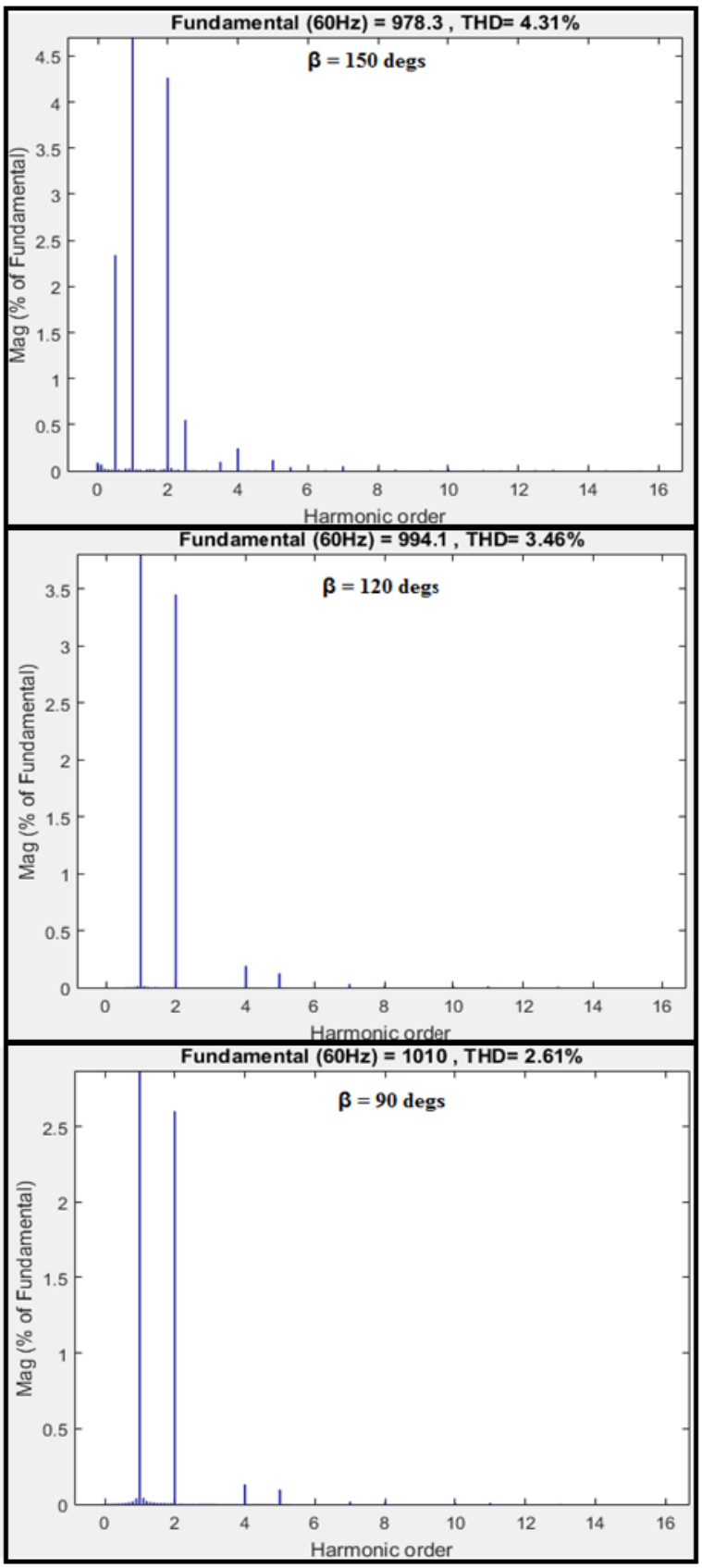


Figure 6.2-9: THD (β = 150, 120, 90 degs.) of Half-Bridge Controlled Rectifier

In Fig. 6.2-10, the variation of PF as a function of β for two conditions is shown: PF (Original) which is based on current controller design for half-bridge rectifier and PF (After Phase Shift), where a shift of 30 degs. was attempted for switching, in-order to make V_{output} shape symmetric.

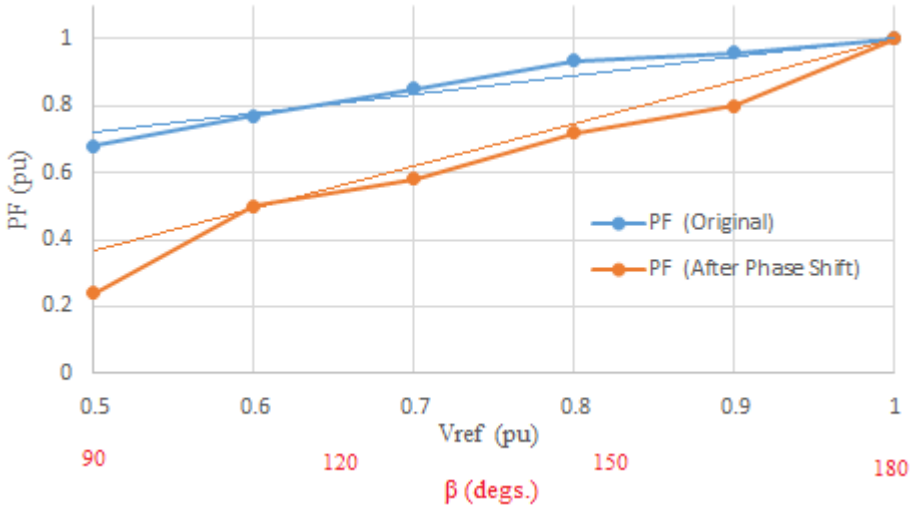


Figure 6.2-10: PF of Half-Bridge Controlled Rectifier with and without phase shift

Fig. 6.2-10 shows the variation of PF in pu, varying from a 0.0 pu to 1.0 pu versus β in degs., varying from 90 degs. to 180 degs.. There are two cases shown in this figure: PF (Original) in blue and PF (After Phase Shift) in orange.

Fig. 6.2-10 verifies that for the PF (Original), the PF increases with a slope of 0.0051pu/deg. from β = 90 degs. to β = 150 degs. The result in Fig. 6.2-10 displays the PF increase from 0.67 pu at β = 90 degs. to 0.95 pu at β = 150 degs. Ranging from β = 150 degs. to β = 180 degs. PF is nearly ideal (PF > 0.95). As a result, it can be said that PF is adequate for most of the β range.

As for the case PF (After Phase Shift), it exhibits the same behavior as PF (Original), however it can be clearly seen that PF in this case is much inferior with a

starting point at 0.27 pu at β = 90 degs. which increases at the rate of 0.0087 pu/deg.. As a result, shift in switching square waves were not applied for V_{output} shape correction.

6.2.3. Conclusion

A half-bridge controlled 3-phase rectifier is an acceptable solution for the power supply since the output THD and PF are acceptable. As compared to the conventional 3-phase converter, this power supply seems to be more cost effective. One of the most popular schemes is called voltage and current cascaded control (VICC) scheme for fully controlled 3-phase converter. In the following section, the VICC system is explained along with its results and then compared with 3-phase half-bridge power supply system.

6.3. Introduction to Fully Controlled Symmetric Rectifier using VICC:

Fig. 6.3-1 displays a fully-controlled, IGBT-based, force-commutated symmetric converter composed of six controlled IGBT switches: S1, S3, S5, S4, S6, and S2. Additionally, it has a capacitor - which acts as a load side filter - that is connected across the RL load. The VICC for this rectifier can be utilized to independently control the active power P and reactive power Q. This rectifier is capable of absorbing sinusoidal current input with a near unity PF. Furthermore, it can work in both the rectifying and inverting modes, as well as control the DC voltage. Potentially, this rectifier can be an ideal solution for TESS [38].

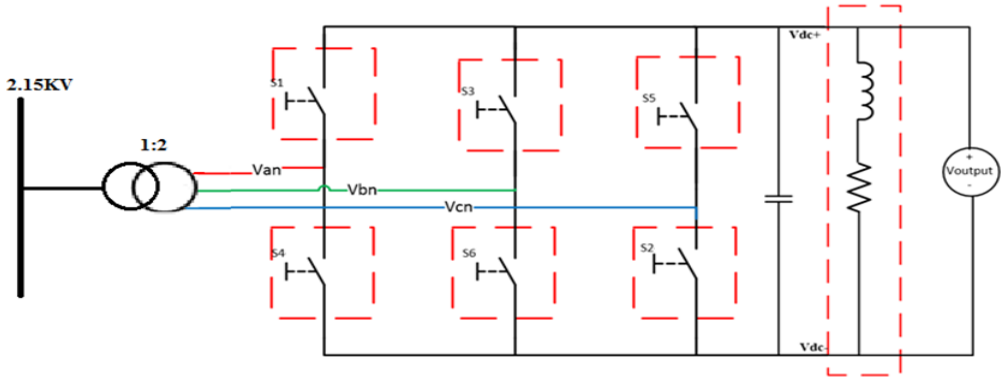


Figure 6.3-1: Fully Controlled 3-Phase Rectifier

Furthermore, in previous sections (sections 5.3 & 6.2), successful attempts were made to remove the harmonics using an external LPF-LC filter; however, there were still challenges mainly due to the filter having a negative impact on PF. Therefore, a full control scheme such as VICC should be able to reduce the LPF, which will make the system not only more cost-effective, but simple as well.

6.3.1. VICC Rectifier Model:

Generally, switched boost rectifiers are considered to be one of the better choices that have a nearly sinusoidal input current, while being controlled by sinusoidal PWM. Thus, they have lower THD, while being controlled by VICC [38]. Thus, employing a simple L-filter on the AC side of the rectifier (Fig. 6.3-2) is used to deal with the current harmonics. Switching functions of this rectifier are defined using a switching space vector for an active rectifier $p_j\,(t) = (j = a, b, c)$:

$$\bar{p}(t) = \left(\frac{2}{3}\right)\left(p_a(t) + \alpha * p_b(t) + \alpha^2 * p_c(t)\right) \tag{6-1}$$

Assuming an L on the AC side, the mathematical model becomes [38],

$$\frac{d\bar{\imath}(t)}{dt} = \frac{1}{L}\left[-R\bar{\imath}(t) + \bar{e}(t) - \frac{1}{2}\bar{p}(t)v_{0output}(t)\right] \tag{6-2}$$

$$\frac{dv_{0output}(t)}{dt} = \frac{1}{C}\{\frac{3}{4}Re\left[\bar{p}(t)\bar{\bar{\imath}}(t)\right] - i_L(t)\} \tag{6-3}$$

$\bar{p}(t)$, $\bar{\imath}(t), and\ \bar{e}(t)$ are the space vectors of the rectifier input power, current and grid voltage (Fig. 6.3-3). $\bar{\bar{\imath}}(t)$ represents the complex conjugate of $\bar{\imath}(t)$. Equation (6-2)-(6-3) show that the system is non-linear and its behavior is dependent on $\bar{p}(t)$.

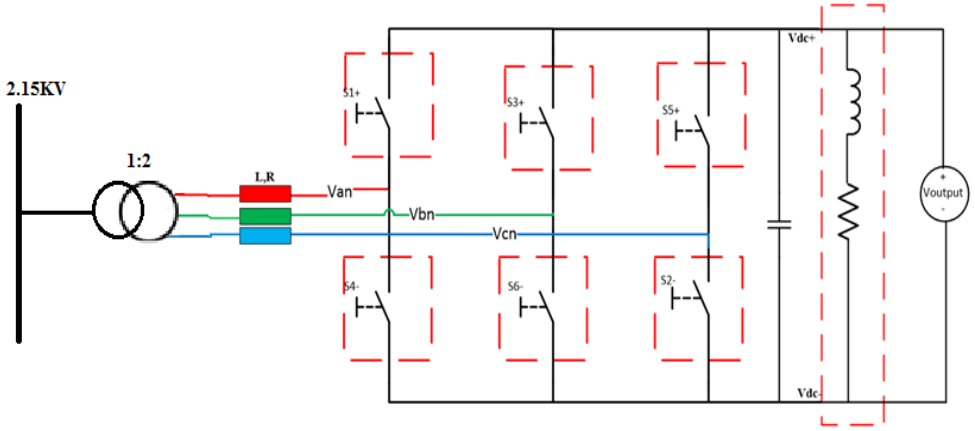


Figure 6.3-2: Full Controlled 3-Phase Rectifier with L at AC side

6.3.2. Rectifier Control:

The rectifier voltage control is *dq* frame oriented (Fig. 6.3-3), where i_d (input current *d*-component) is used to control the DC voltage and similarly, i_q (input current *q*-component) control is used to control the reactive power and to achieve a unity PF. Since *dq*-frame is being used, which rotates at angular speed ω (ω = 2πf), where f is fundamental frequency, equation (6-2) becomes:

$$\frac{di_d(t)}{dt} - \omega i_q = \frac{1}{L}\left[-Ri_d(t) + e_d(t) - \frac{1}{2}p_d(t)v_{0utput}(t)\right]$$

$$\frac{di_q(t)}{dt} + \omega i_d = \frac{1}{L}\left[-Ri_q(t) + e_q(t) - \frac{1}{2}p_q(t)v_{0utput}(t)\right]$$

(6-4)

Equation (6-4) illustrates that because of cross coupling terms $\omega i_d(t)$ and $\omega i_q(t)$, the *d* and *q* differential equations for the current are inter-dependent.

$$\frac{dv_{output}(t)}{dt} = \frac{1}{C}\left\{\frac{3}{4}\left[p_d(t)i_d(t) + p_q(t)i_q(t)\right] - i_L(t)\right\}$$

(6-5)

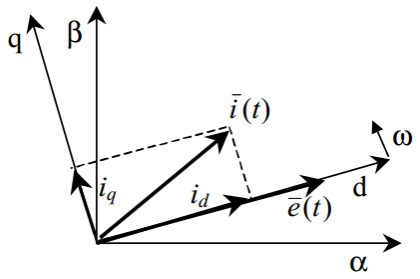


Figure 6.3-3: Active Rectifier's Voltage Control in the dq frame [38]

Equation (6-5) can be linearized considering $V_{output}(t) = V_{output}$, (where V_{output} is a constant), hence, making it possible for continous switching vector to be replaced with average converter voltage [38].

Compared to the single loop voltage control, the cascaded two loops control scheme is formed by the current loop, which is the inner loop for fast dynamics; the voltage loop is the outer loop for slower dynamics, which helps with the overall stability of the system. That being said, in terms of control systems, the outer loop must be ten or more times slower than the inner loop to decouple both dynamics. By satisfying this condition, the reference value of the inner loop (which is the output signal of the outer

controller i_{dref}) can be considered relatively constant. Therefore, the choice of the inner loop parameters are subjective to this criteria. Load change can produce transients in the voltage loop; however, since the inner current loop is faster, its reference (i_{dref}) is considered fairly constant allowing it to compensate for the change very quickly [38].

In the control block diagram that is shown in Fig. 6.3-4, the output voltage control is performed by updating the i_{dref} which adjusts the value of the input current. In order to minimize the ripples from output voltage, ωL from the difference of V_{output} and V_{ref} gets subtracted from $V_{q,}$ which is expected to be 0 or very close to it. Similarly, ωL from i_{qref} (contstant 0) is added to V_d.

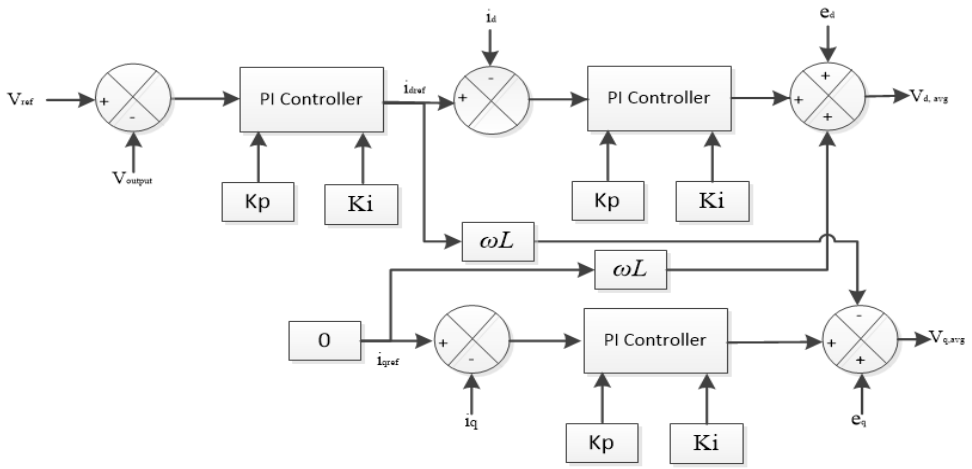


Figure 6.3-4: Basic Controller scheme for Active Rectifier

In Fig. 6.3-5, V_{ref} is compared with V_{output} (average value, due to capacitor in parallel with the load (Fig. 6.3-2)) through PI controller (K_p = 0.2, K_i = 1/0.002) returning a constant i_{dref}. This constant decreases in each cycle until error reaches zero between V_{ref} and V_{output}. Moving to the inner loop, i_{dref}, is then compared with i_d which is obtained through input current I_{abc}, using abc to DQ0 transformation. This transformation separates the real and complex components i_d and i_q of I_{abc}. These are the rotating vectors

which remain constant during the steady state condition. In-order to obtain matching crossover frequency between voltage and current (inner and outer loop), a PLL is used, where, V_{abc} is the input for PLL and output is used as a reference during the transformation of I_{abc} *to* i_d and i_q. This also helps greatly in PI tuning to achieve optimum symmetry.

As mentioned earlier, the time constant for the PI controller for inner loop is at-least 10 times greater than the time constant of the PI controller used for outer loop, which leads to more optimal results. PI controller (K_p = 0.02, K_i = 1/0.0017) is used in between i_d and voltage constant, i_{dref}, in order to obtain the value of $V_{d,avg.}$ It is also used between constant 0 and i_q as the zero-complex component of current would provide the finest results. This is because there would be no torque for rotation and a constant value can be achieved instead of oscillation because of rotation. Through this, i_q is reduced within a few cycles providing a constant zero or close to zero $V_{q,avg}$. Once both constants $V_{d,avg}$ and $V_{q,avg}$ are found, they are transformed back to V_{abc} using the DQ0 to abc transformation and similarly as before, the same PLL output is used during this transformation as a reference.

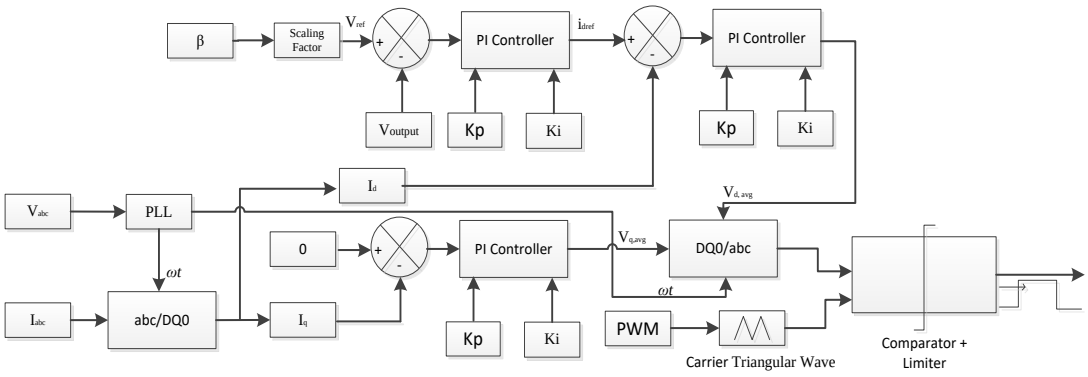


Figure 6.3-5: Basic scheme for VICC

Nonetheless, as low order harmonics are close to the fundamental frequency, they are more difficult to filter out. Thus, they can cause more pronounced ripples at the output voltage, which in fact, will not affect the load as much since it is for heating application. Such an effect does not affect the controller performance as significantly at a high output voltage. However, as the output voltage decreases, lower harmonics becomes more prominent and affect the controller's output and overall stability of the system. Nonetheless, this issue can be overcome by implementing a symmetrical PWM switching strategy.

It is clear that symmetrical PWM can solve this problem as it increases the carrier frequency which shifts the harmonics towards higher order ones, making it easier for the external LPF to filter them out. This reduces their effect on the control loops, despite being existed at the output voltage, which, as mentioned, does not affect the load requirements. The triangular carrier frequency used in symmetrical PWM is at 10 kHz which is then compared against the reference signal, providing the proper switching pattern for each gate [53], as shown in table 2 below:

Table 2: Switching Pattern

Switching Pulse	***Switch***
V_a	*S1*
V_a *(NOT)*	*S4*
V_b	*S3*
V_b *(NOT)*	*S6*
V_c	*S5*
V_c *(NOT)*	*S2*

6.3.3. Results:

Fig. 6.3-6 shows the test response of the output of the controller V_{output} to a step change in the V_{ref} (V_{ref} = 1 pu to V_{ref} = 0.5 pu) implemented at 0.1 second. This test verifies the dynamic performance of the 3-phase VICC converter. The simulation duration is 0.2 second. However, the post disturbance period shows a remarkably unstable performance with sustained oscillations at 5th harmonic.

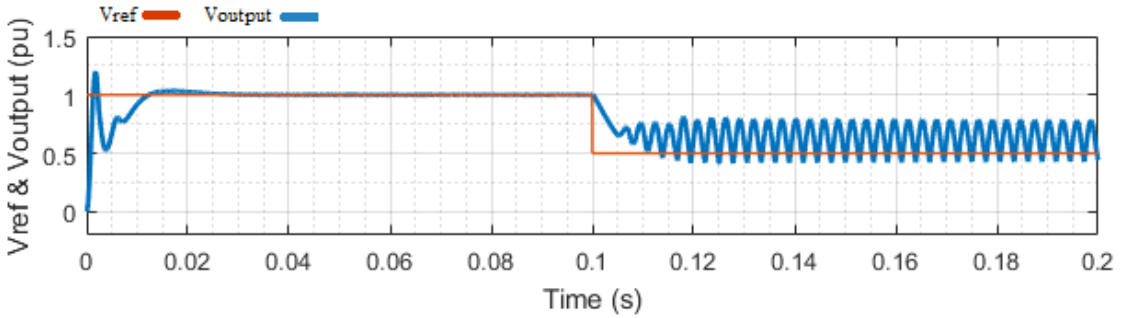


Figure 6.3-6: Step Change in V_{ref} from 1 pu to 0.5 pu

Fig. 6.3-6 shows the comparative variation of V_{ref} and V_{output} in pu, varying from a 0.0 pu to 1.0 pu versus time in seconds, varying from 0s to 0.2s. This figure shows V_{ref} in orange and V_{avg} in blue. Fig. 6.3-6 verifies that unlike half-bridge rectifier, VICC rectifier fails to follow the step change closely and in a stable manner. Therefore, this confirms the VICC converter's dynamic performance has limitations.

To find out those limitations; VICC rectifier needs to be examined more. As a result, Fig. 6.3-7 to Fig. 6.3-9 VICC is examined for three different values of the reference voltage V_{ref} = 0.833, 0.633 and 0.5 pu (which are also equivalent to conduction angles β = 150, 120 and 90 degs. (Relationship between V_{ref} and β is defined in section 4.3.2)).

Initially, V_a & I_a, is displayed by Fig. 6.3-7a to Fig. 6.3-9a to observe their shape and ripples in input. Following that, Fig. 6.3-7b to Fig. 6.3-9b shows the response of the output of the controller V_{ref} and V_{output} for each β case. Similarly, Fig. 6.3-7c to Fig. 6.3-9c shows the output current (I_{output}) to observe the response for each β case. The runtime is 0.2 second.

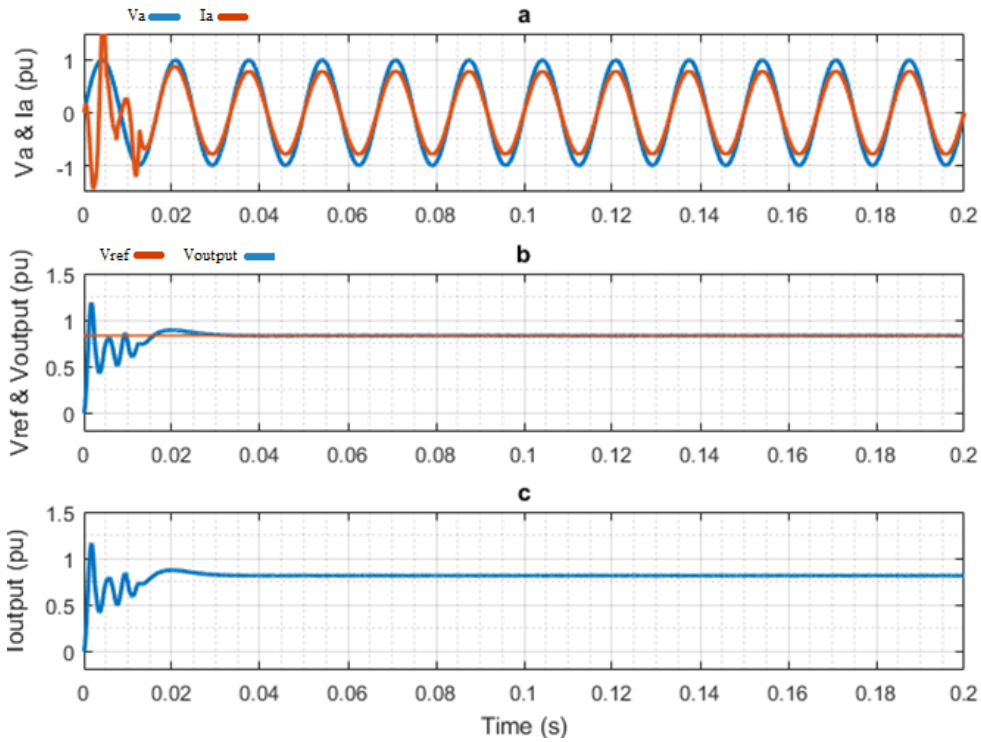


Figure 6.3-7: VICC Input and Output at V_{ref} = 0.833 pu (or β = 150 degs.)

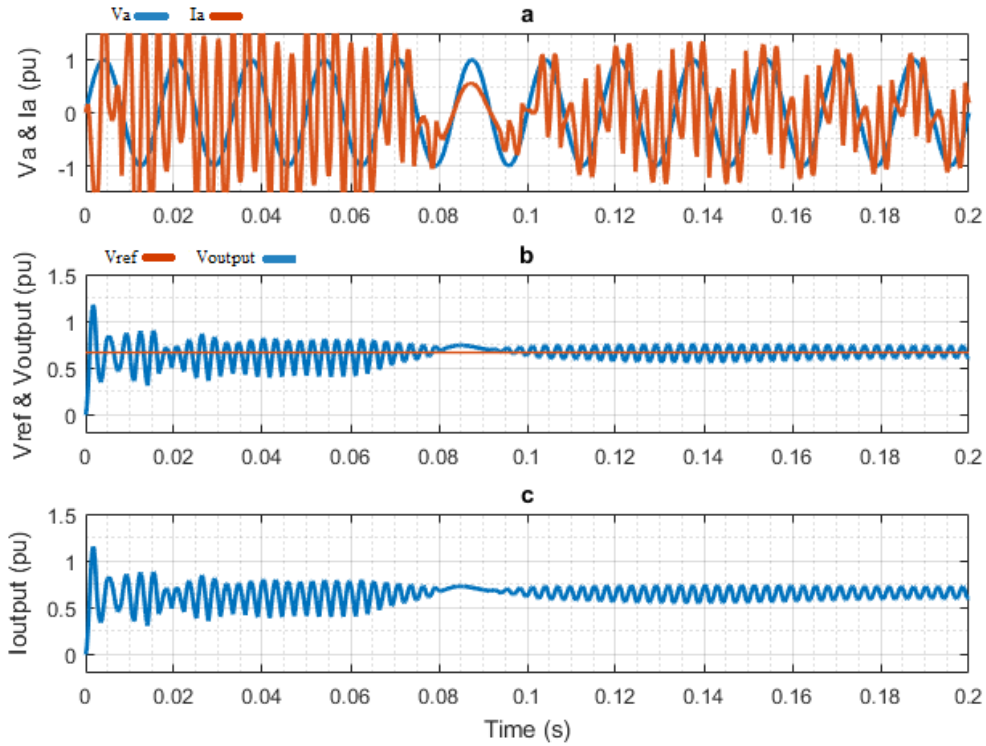


Figure 6.3-8: VICC Input and Output at V_{ref} = 0.667 pu (or β = 120 degs.)

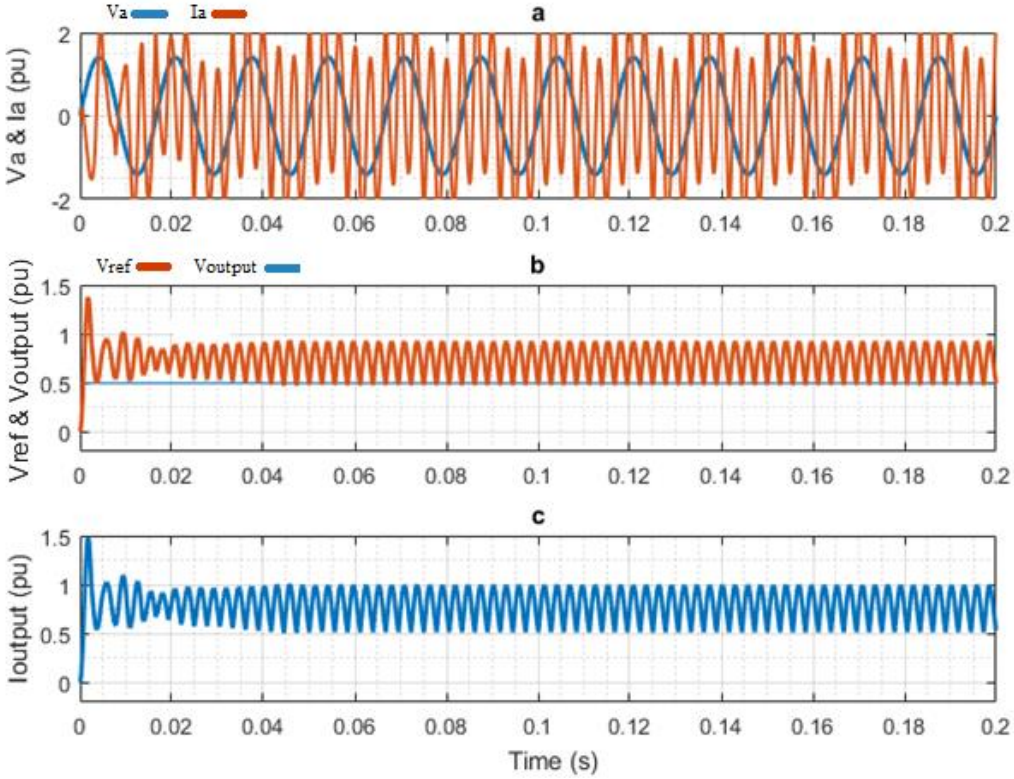


Figure 6.3-9: VICC Input and Output at V_{ref} = 0.500 pu (or β = 90 degs.)

Fig. 6.3-7a to 6.3-9a show the variation of V_a (in blue) & I_a (in orange) in pu, varying from a -1.5 pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. In comparison, Fig. 6.3-7b to 6.3-9b display the variation of V_{ref} (in blue) vs. V_{output} (in orange) in pu, varying from a 0.0 pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. Additionally, Figs. 6.3-7c to 6.3-9c depict the variation of I_{output} in pu, varying from a 0.0pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. In Fig. 6.3-7 both the voltage (V_a) and current (I_a) outputs are nearly a pure sinusoidal (i.e. low THD) waveform, which are in phase (i.e. unity PF) at β = 150 degs.. However, as compared to Fig. 6.3-7, the voltage and current output seen in Fig. 6.3-8 and 6.3-9 have a high ripple content (5^{th} harmonic oscillation) causing the system to operate poorly. Therefore, there exists a breaking point in between β = 150 degs. to β = 120 degs. which make sense, as V_{ref} needs to be equal or higher than voltage going into a boost rectifier. Boost rectifier is unable to handle an output voltage that is lower than its input voltage and for that buck-boost rectifier is needed. The input voltage in this case (with boost rectifier) is 2633V which is equal to V_{ref} = 0.71 pu (or β = 128 degs.). Hence, Fig. 6.3-10 shows the test response of the output of the controller V_{output} to a step change in the V_{ref} (V_{ref} = 0.72 pu to V_{ref} = 0.69 pu) implemented at 0.1 second to verify the performance and to find out the breaking point of the 3-phase VICC converter. The simulation duration is 0.2 second.

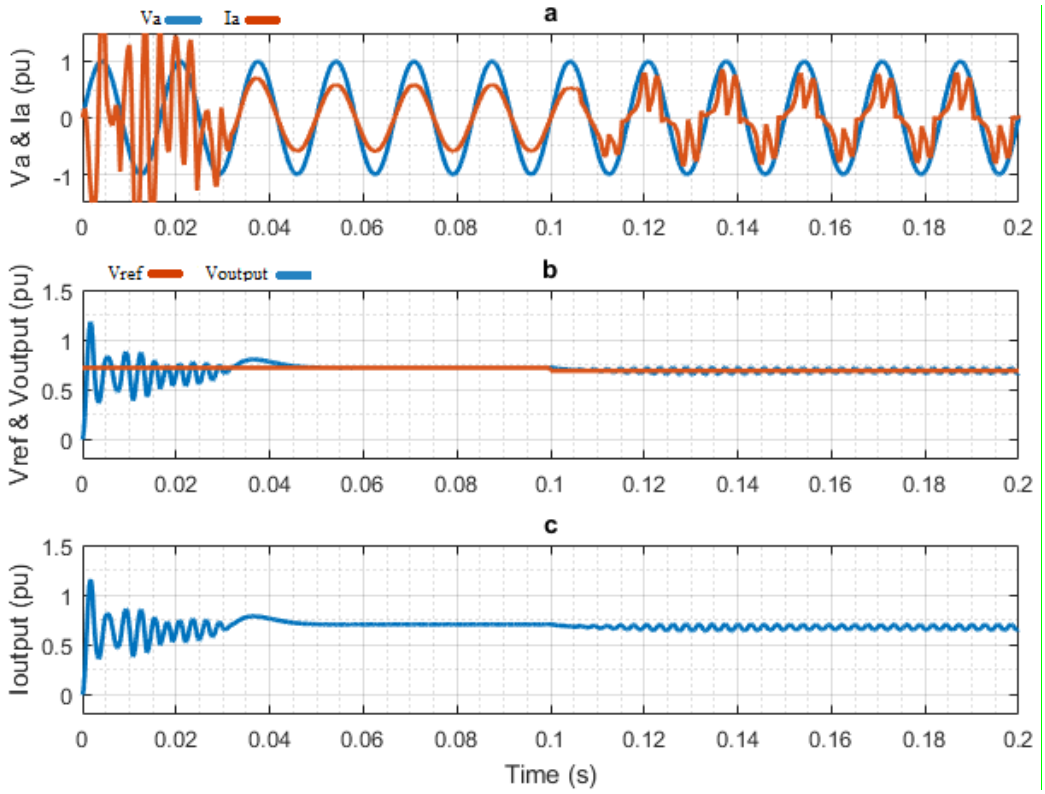


Figure 6.3-10: Step Change in V_{ref} from 0.72 pu to 0.69 pu (or β from 130 degs. to 124 degs.)

Fig. 6.3-10a shows the variation of V_a (in blue) & I_a (in orange) in pu, varying from a -1.5 pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. In Fig. 59a both the voltage (V_a) and current (I_a) outputs are nearly a pure sinusoidal waveform before the step change at 0.1 second and then ripples can be seen in I_a.

In comparison, Fig. 6.3-10b displays the variation of V_{ref} (in blue) vs. V_{output} (in orange) in pu, varying from a 0.0 pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. Similar behavior as Fig. 6.3-10a can be seen in Fig. 6.3-10b, V_{output} takes 0.045s reaching the steady state, however, after the step change at 0.1s there appears to be ripples in V_{output} and does not seem to be stable.

Finally, Figs. 6.3-10c depicts the variation of I_{output} in pu, varying from a 0.0 pu to 1.5 pu versus time in seconds, varying from 0.0s to 0.2s. Once more, similar behavior can

be seen in I_{output} which takes 0.045s reaching the steady state, however, after the step change at 0.1s there appears to be ripples in V_{output} and does not seem to be stable. Therefore, it can be concluded that the operational range for VICC scheme with boost rectifier is from 1 pu to 0.71 pu (or $\beta = 180$ degs. to $\beta = 128$ degs.).

Since it is a close loop system, the output of the system has a severe impact on the input of this system (i.e. voltage and the current). Therefore, beyond the operational range VICC rectifier, the uncharacteristic output of voltage and current is causing THD to increase exponentially and PF to drift away from unity.

Fig. 6.3-11 displays the THD for VICC rectifier over the range from $\beta = 150$, 128, and 120 degs.:

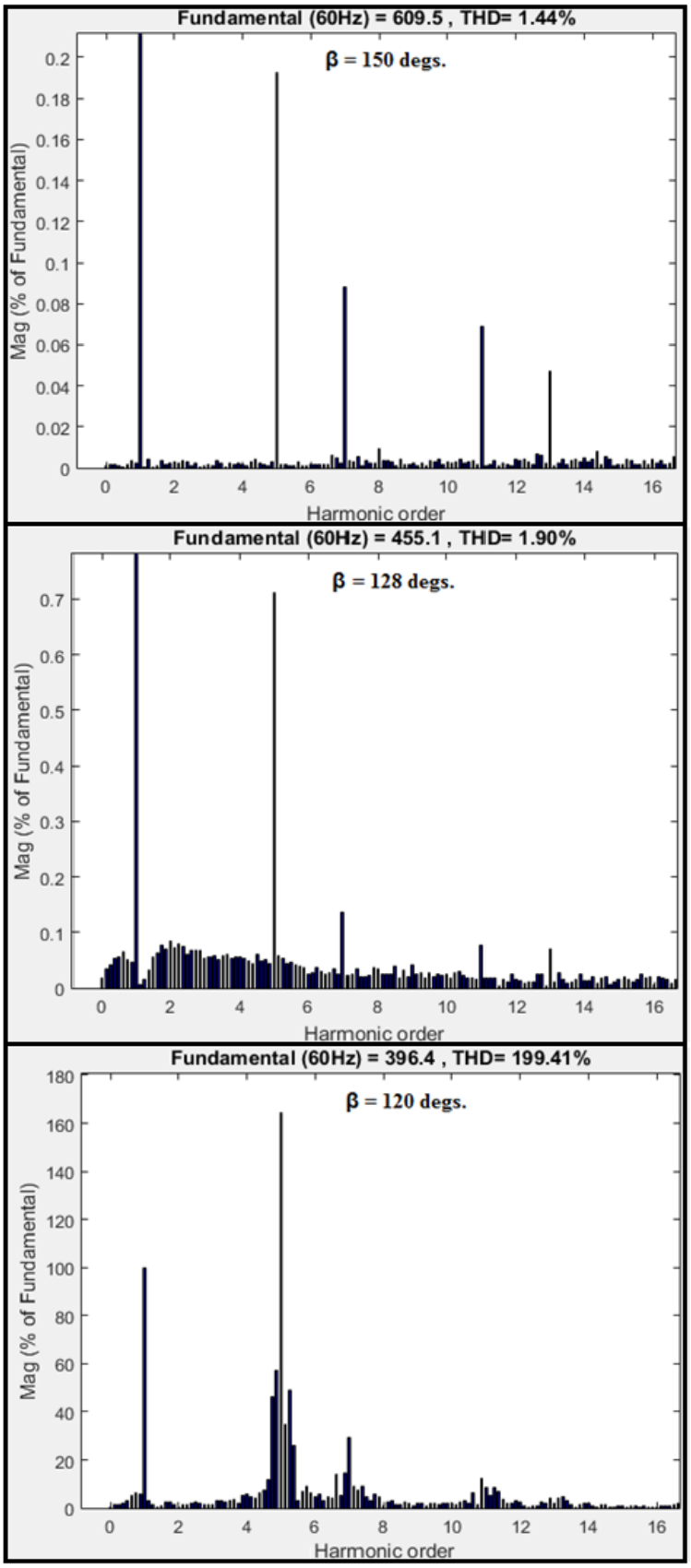


Figure 6.3-11: THD (β = 150, 128, and 120 degs.) with VICC Scheme

The results shown in Fig. 6.3-10 illustrates the effect on THD based on different conduction angles (β). It can be observed that THD is under 2% for up to β = 128 degs., which is under the required rate of 5%. However, after that range THD increases exponentially up to 199.41% as can be seen for β = 120 degs..

Fig. 6.3-12 displays the PF over the range of β = 180 degs. to β = 90 degs.:

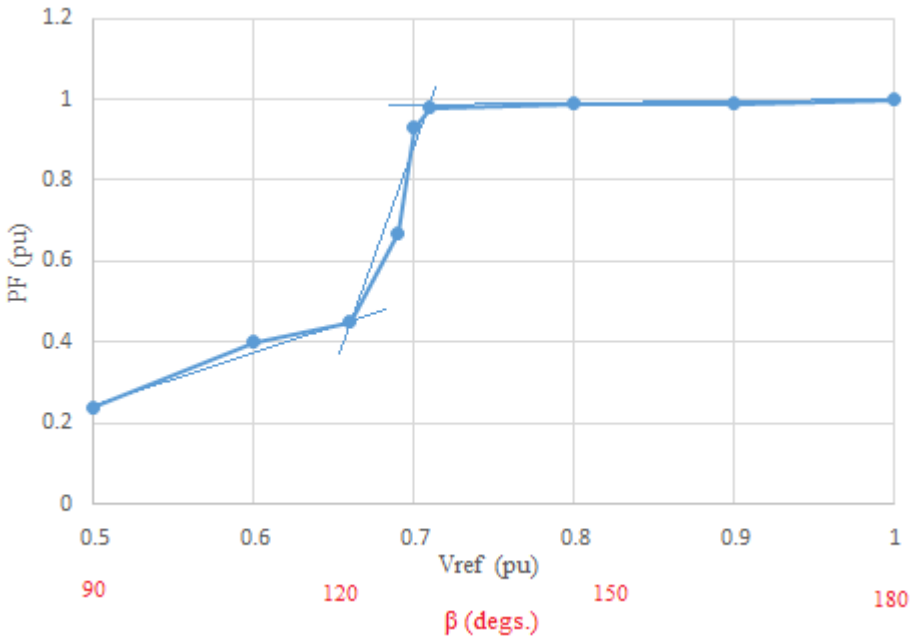


Figure 6.3-12: PF with VICC Scheme

Fig. 6.3-12 depicts the variation of PF in pu, varying from a 0.0 pu to 1.0 pu) versus the β in degs., varying from 90 degs. to 180 degs.. It can be seen that PF is nearly ideal (PF = 0.995) for the β ranging between 180 to 128 degs.. Conversely, PF drops rapidly to PF = 0.45 as β decreases form 128 to 120 degs. and then changes gradually from 0.45 to 0.27 for β ranging from 120 to 90 degs., as it can be seen in the figure above.

6.3.4. Conclusion:

Results in the previous section demonstrate that the full symmetric 3-phase VICC rectifier can be utilized for TESS heating application. Conversely, the system is capable of operating within certain limits of β values (β = 180 to β = 128 degs.). Within the specified range, the system performs ideally with THD less than 2% and PF at 0.995. However, outside that operational range, the THD increases exponentially, and PF falls down rapidly. Nevertheless, the system is more cost efficient due to the fact that it only uses one boost inductor (200μH) per phase for harmonic filtering. Hence, it can be said that the system with VICC converter can be implemented for TESS heating application, but with certain limitations of control.

6.4. Comparison between Half-Bridge Control and VICC Converter Results

This section will compare the THD and PF between the half-bridge converter and full VICC converter. Followed by that it will look at the solutions from the perspective of cost and TESS.

6.4.1. THD Comparison

Fig. 6.4-1 compares the THD of 3-phase half-bridge rectifier and VICC rectifier.

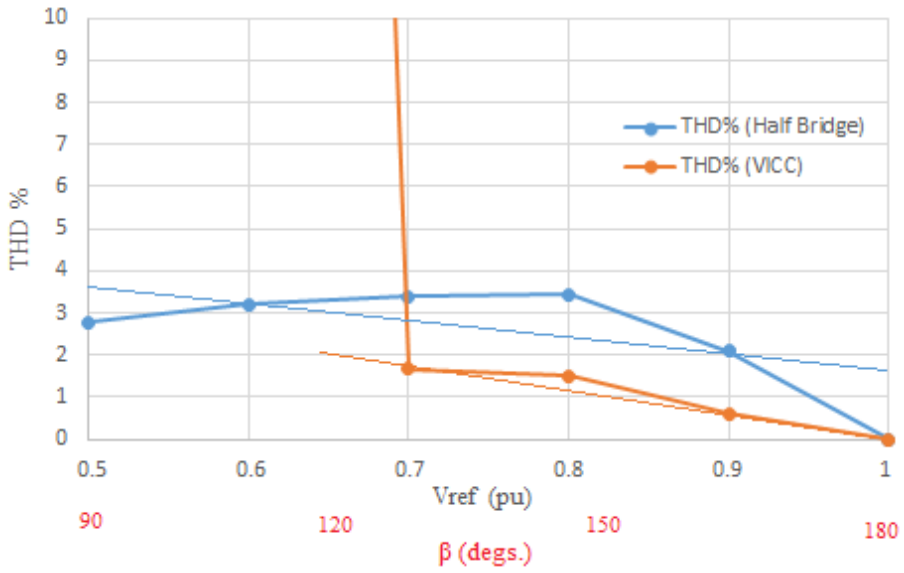


Figure 6.4-1: THD Comparison between Half-Bridge Rectifier and VICC Rectifier

Fig. 6.4-1 shows the variation of THD in %, varying from a 0% to 10% versus β in degs., varying from 90 degs. to 180 degs.. There are two cases shown in this figure: PF (Half-Bridge) in blue and PF (VICC) in orange.

For half-bridge rectifier, the THD is below that of the VICC rectifier throughout β values from 180 degs. to 90 degs., whereas, VICC rectifier has only operational range from 180 degs. to 128 degs. and after that range the THD overshoots dramatically the requirement of 5%threshold. Therefore, it can be said that if a rectifier is required to work under only certain voltage range, both rectifiers are going to effective. However, for a wider range of operation, the half-bridge rectifier seems to be the more effective solution.

6.4.2. PF Comparison

Fig. 6.4-2 compares the PF of 3-phase half-bridge-controlled rectifier and VICC rectifier.

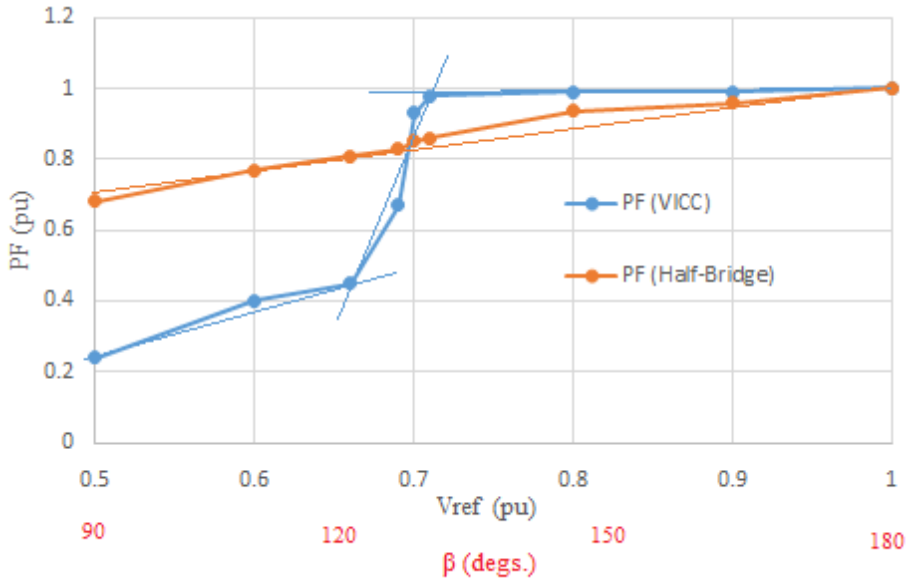


Figure 6.4-2: PF Comparison between Half-Bridge Rectifier and VICC Rectifier

Fig. 6.4-2 shows the variation PF in pu, varying from a 0.0 pu to 1.0 pu versus β in degs., varying from 90 degs. to 180 degs.. There are two cases shown in this figure: PF (Half-Bridge) in orange and PF (VICC) in blue.

For half-bridge-controlled rectifier, the PF rises from 0.65 linearly with the β values at 90 degs. to unity at 180 degs. with the slope of 0.00359 pu/deg.. However, for VICC rectifier, the PF is fairly low at 0.27 at β = 90 degs , and it jumps to almost unity at β = 128 degs.. Therefore, it can be concluded that to handle a smaller range of β in the VICC controller is a better solution, but for wider range the half-bridge-controlled rectifier seems to be more effective.

6.4.3. Cost and Requirements Analysis

The biggest factor, in terms of the cost, is the requirement for an external LPF. For half-bridge-controlled rectifier LC-LPF is used where L is 2 mH and C is 2000 μF as compared to VICC rectifier where only L (boost inductor) is used with the value of 0.2

mH making it a much cheaper solution in terms of LPF. Furthermore, VICC rectifier also uses a capacitor in parallel to load with value of 900 μF to obtain average V_{output} whereas, in half-bridge-controlled rectifier a 2nd order LPF is used in controller (much cheaper) to find average after the V_{output} is obtained. Lastly, the half-bridge rectifier has 3 IGBTs (controllable switches) and 3 diodes as compared to VICC rectifier which has 6 IGBTs increasing its cost slightly. Overall when looked at VICC controller seems to be the cheaper solution among the two.

In TESS, graphite is expected to change its resistance with the temperature which will cause change in load, and ultimately effecting the voltage. Resistance is proportional to voltage and change in resistance can be almost as much as two-third of its original value or a little more. Therefore, expected voltage change with respect to heat can be same. From that perspective, for TESS 3-phase half-bridge rectifier seems to be more feasible solution as compared to 3-phase VICC rectifier.

CHAPTER 7: CONCLUSION

Meeting the projected energy demand with integration of reneweable energy sources with the modern electrical grid faces a challenge; it requires an improvement in its efficiency and operating capabilities. The energy storage system will play a vital role to assist with these challenges, as well as ensure a high flexibility and reliability of the system. Consequently, improving energy storage technology appears to be the next problem that needs to be addressed as electricity, as of yet, cannot be stored easily or efficiently at significant power levels (i.e. greater than a few MW). Therefore, this thesis proposes that TESS technology be utilised to store energy during low-cost off-peak times when the demand for electricity is low. The stored energy can then be utilised during peak times when electricity demand is high. This ensures peak shaving to be achieved for a more efficient electricity utilisation.

TESS is a new technology that offers a few advtantages compared to BESS, such as TESS is capable of storing energy for longer time periods, and at a lower cost while TESS capacity limits can exceed most other known storage technologies. Furthermore, TESS has less energy wastage in the long run. The electrical energy is converted to thermal energy in order to be stored in a TESS. Hence, this procedure requires an optimal heating element for the TESS. Graphite is used for this purpose and designed according to the desired resistance requirements. However, it is known that Graphite's resistance varies with temperature making it non-linear. Consequently, a fast acting voltage controlled power rectifier is used to supply the electrical power to the heating element at high efficiency while maintaining the harmonic distortion of the gird current at a minimum.

Such a power supply presents some challenges. Choosing the proper control and switching technique is the key factor that affects the system's overall performance and efficiency. Keeping the cost of operation in mind, a 1- phase rectifier with the half-controlled symmetric converter is more appropriate. It is observed that by changing from an asymmetric to a symmetric converter, higher PF closer to unity is achieved. However, distortion in the input current in terms of THD remains at unacceptable levels compared to the grid regulation codes. Therefore, PWM modulation technique with LPF designs are investigated and implemented in this work.

Implementing PWM shifts the generated harmonics to a higher frequency order, which makes the LPF compact and cost effective. An LC-LPF is utilized as an external LPF in-order to bring THD down to 5% or below for V_{ref} changing from 1 pu to 0.5 pu. However, it is noticed that LC-LPF also affects the PF but it remains within the feasible range for most of the V_{ref} . Thus, the system is stable and a cost-effective solution for heating purposes with a 1-phase rectifier in proposed TESS design.

A similar scheme to the 1-phase rectifier is applied to a half-bridge controlled 3-phase rectifier and is found to be an acceptable solution for the power supply. It offers the output THD to be under 5% similar to 1-phase rectifier and PF is also acceptable. Furthermore, it seems to be cost effective and provides a reasonable operational range (conduction angles from $\beta = 180$ to 90 degs.).

A comparison between the fully controlled 3-phase converter with VICC scheme and the half-bridge controlled converter is also conducted. For VICC scheme, it is found that VICC with full symmetric 3-phase rectifier works for TESS as well, however, only within the range from $\beta = 180$ to $\beta = 150$ degs. with less than a 3% THD and PF almost at

unity (0.995). However, after that range THD increased exponentially and PF falls down to almost 0.2 from 0.99. Nonetheless, in terms of filtration, it only uses an inductor (for boosting) per phase; conversely, with the half-bridge rectifier, LC-LPF is required. Thus, the overall system is more cost efficient as compared to half-bridge rectifier.

Thus, it can be said that the converter with VICC scheme can be implemented in TESS for less cost, but it provides only a limited range of operation. As a result, in general for TESS, a 3-phase half-bridge rectifier appears to be a more feasible solution in comparison to a 3-phase VICC rectifier.

As a conclusion for TESS, using graphite for heating, a half-bridge voltage-oriented controller (in 1-phase or 3-Phase rectifier) can be implemented as power supplies. As compared to VICC, half-bridge controller provides a wider range of operation within the reasonable cost while meeting the THD and PF requirements. In the future, there is potential to overcome these limitations using VICC control design, thereby offering an even cheaper design solution. The offered VICC rectifier design acts as boost converter, which makes the range of operation limited based on the desired voltage reference. If the rectifier design can be changed into buck-boost converter while using the same VICC controller, it would provide a wider range of operation, while optimally meeting the THD and PF requirements. Additionally, conducting further studies on improving the heating material (i.e. graphite) and heated material (i.e. molten salt) will assist in improving efficiency and cost of the system. Moreover, studies in insulation method also will impact in improvement in efficiency and capacity for TESS.

APPENDIX

8.1. Model of Half-Controlled Symmetric Converter

This section gives more information about 1-phase half-controlled rectifier design (Chapter 5). Fig. 8.1-1 shows a block diagram of a half-controlled rectifier system. Each block is then explained in depth to verify the stability of the system.

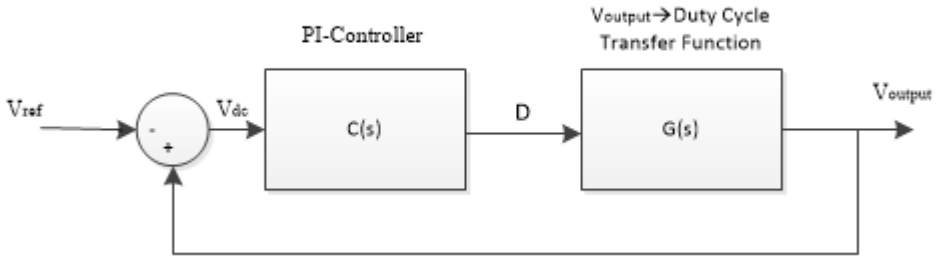


Figure 8.1-1: 1-Phase Half-Controlled Rectifier Block Diagram

8.1.1. System Transfer Function (G(s))

Symmetric 1-phase reciter in output voltage control mode is depicted in Fig. 8.1-2. During the on state of either switches S1 or S2, the input ac voltage V_{in} is connected to the load R_L through the input LC filter as shown in the equivalent circuit in Fig. 8.1-3 (a). However, during the off state of either of them, the load is completely disconnected form the input voltage and the LC, as shown in the equivalent circuit shown in Fig. 8.1-3 (b). Moreover, due to the lack of capacitor filter (DC link capacitor) at the load side, the system can be reduced to an equivalent input voltage source V_g (input grid voltage and input LC filter) and a switching circuit that connects the load and disconnects it within one complete ac cycle.

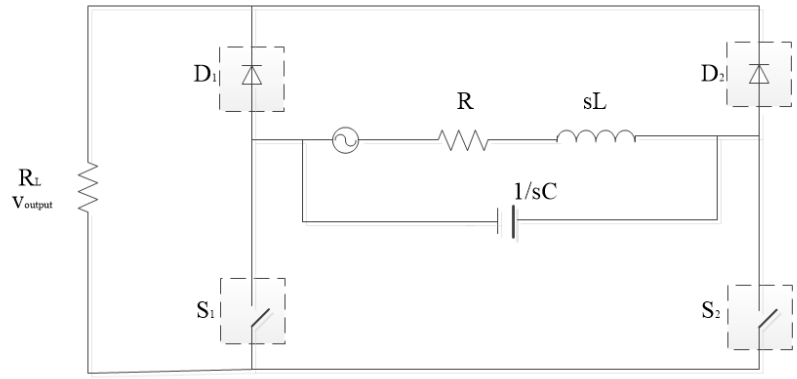


Figure 8.1-2: Symmetric 1-phase Rectfier in Output Voltage Control Mode

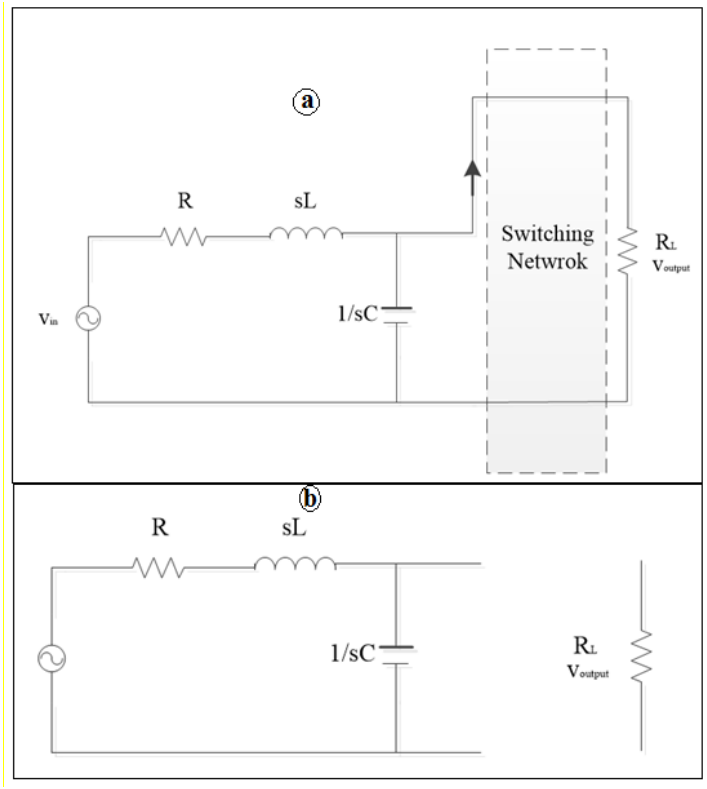
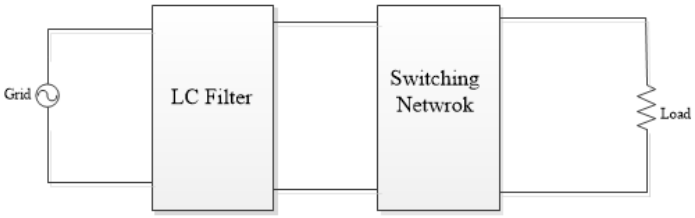


Figure 8.1-3: States of Switching

Therefore, the converter transfer function $G(s)$ can be reduced to the impedance transfer function of the LC input filter [54], as shown in Fig. 8.1-4. Where, the input voltage V_{in} is multiplied by the modulation index mi (the duty cycle) and is referred to as

V_g. As the system is design for output voltage control mode, the transfer function between the output voltage and input modulation index can be deduced as follow:



NETWORK

Figure 8.1-4: 1 Stage Block Diagram

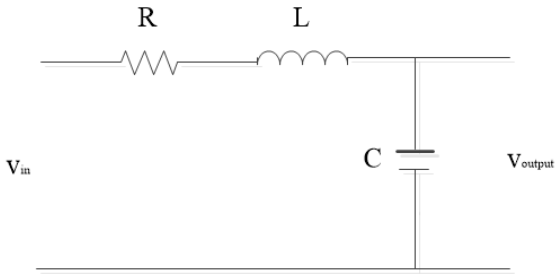


Figure 8.1-5: Impedance Transfer Function of the LC Input Filter

$$V_g = V_{in} * mi \tag{8-1}$$

where, mi is the duty cycle,

As both load impedance and capacitive impedance are in parallel, thus:

$$(\frac{1}{Cs}||R) = \frac{\frac{R_L}{Cs}}{R_L + \frac{1}{Cs}} = \frac{R_L}{CR_Ls + 1} \tag{8-2}$$

Where, R_L is the load impedance and sC is the input filter capacitor in frequency domain (Laplace domain).

Thus, the relation between the output voltage and input modulation index (duty cycle) can be derived as follow:

$$v_{output} = \frac{\frac{R_L}{RCs+1}}{R + Ls + \frac{R_L}{RCs+1}} * v_g \tag{8-3}$$

where, L is the inductor value and R is its wiring resistance.

$$= \frac{R_L}{sRR_LC + RLCs^2 + (R_L + R) + Ls} * v_g$$

$$= \frac{R_L}{RLCs^2 + [RR_LCs + L]s + R_L + R} * v_{in} * mi \tag{8-4}$$

$$G(s) = \frac{V_{output}}{mi} = \frac{R_L}{RLCs^2 + [RR_LCs + L]s + R_L + R} * v_{in} \tag{8-5}$$

Therefore, $G(s)$ provides the transfer function between the system output voltage and mi. The system bode plot, root locus and time step response are shown in Fig. 8.1-6, Fig. 8.1-7 and Fig. 8.1-8. to show the system open loop dynamics.

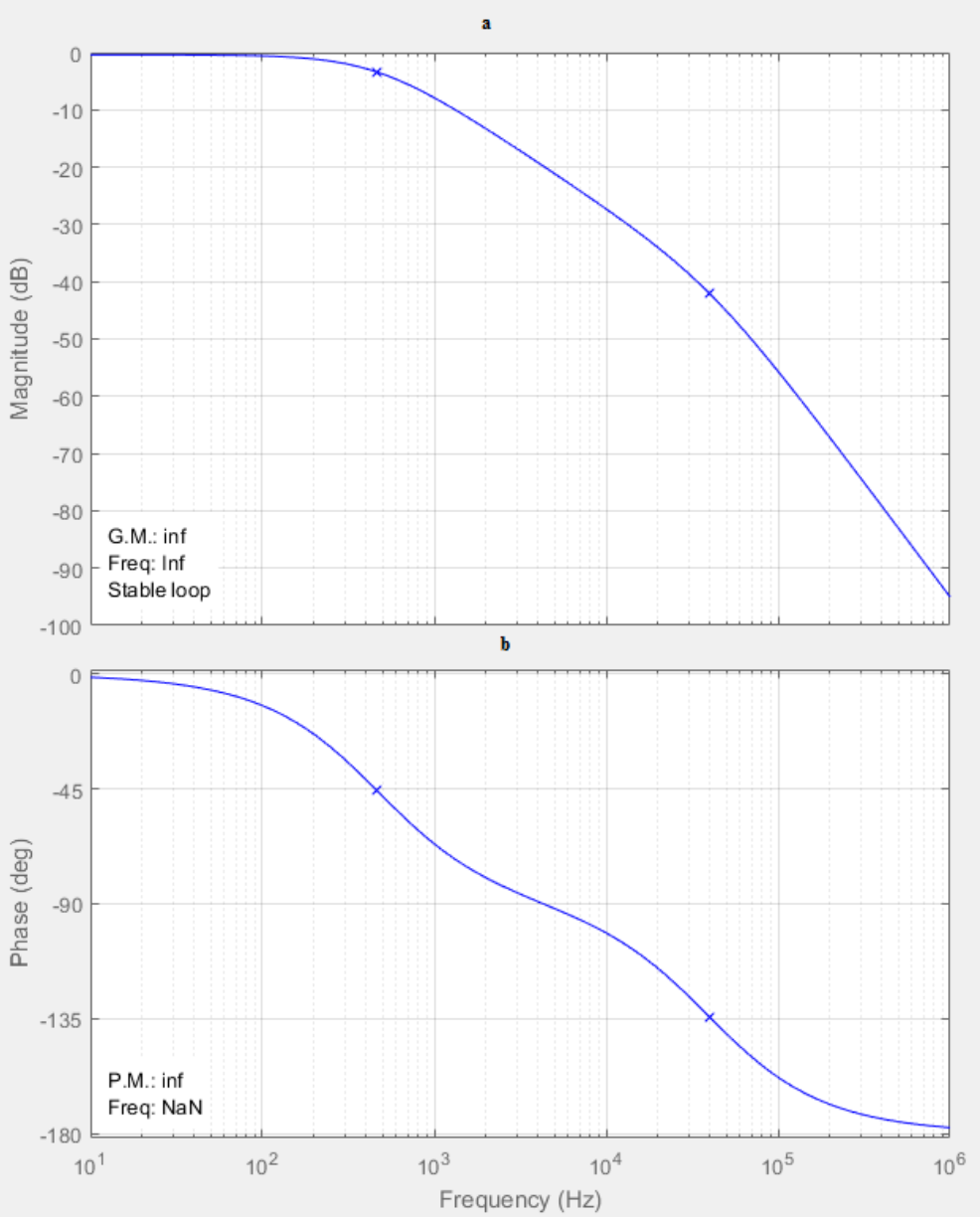


Figure 8.1-6: Magnitude and Phase Diagram

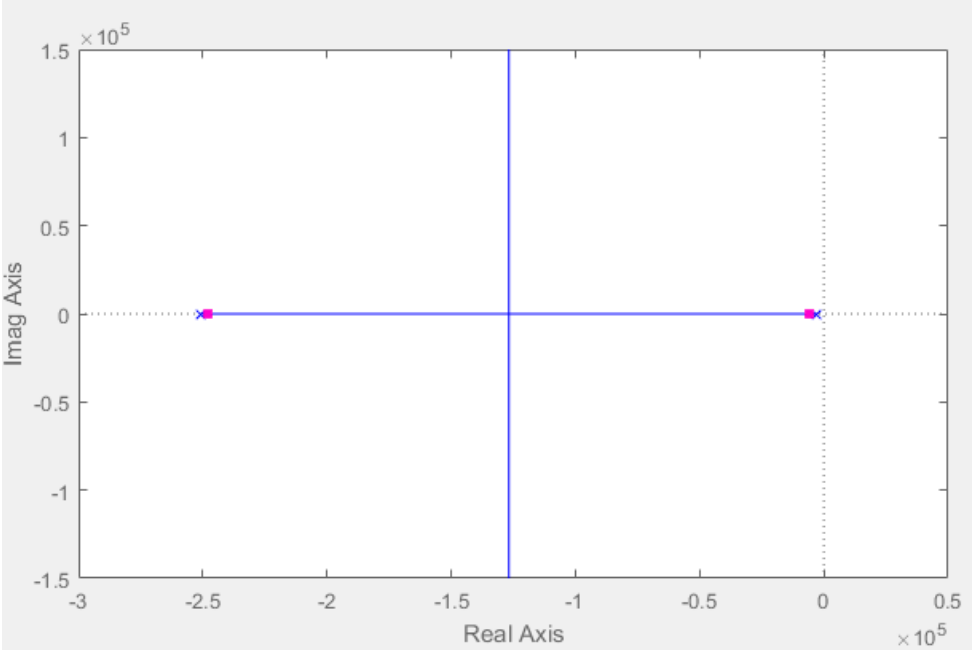


Figure 8.1-7: Root Locus Plot

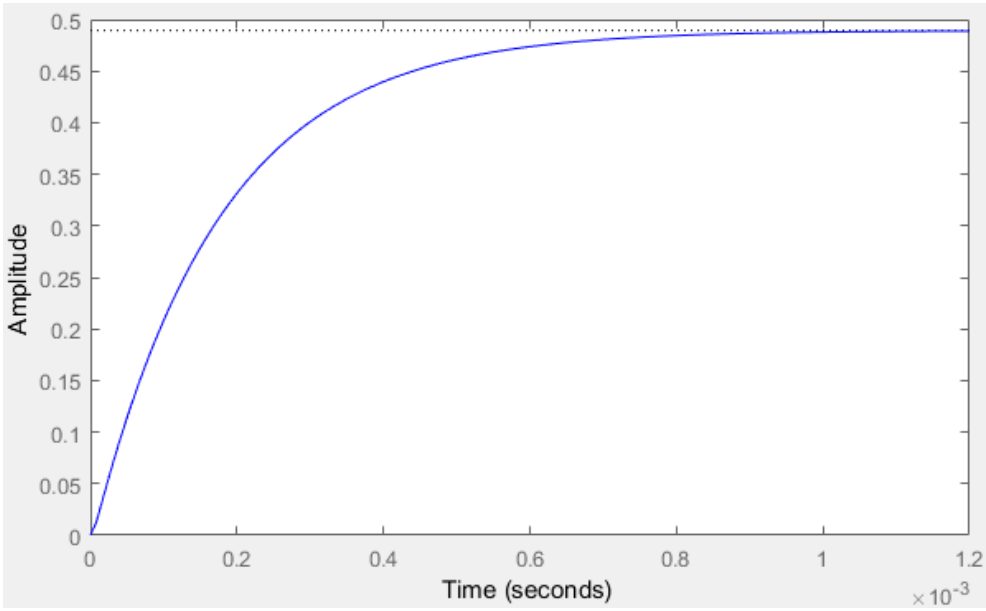


Figure 8.1-8: Time-Step Response

8.1.2. Discretization of the PI Controller (C(s))

The controller transfer function is given by [54]:

$$PI(s) = K_i * \frac{\left(1 + s * \left(\frac{K_p}{K_i}\right)\right)}{s}$$

(8-6)

Euler integration method is being applied for controller discretization. Using Backward Euler method when substitute the *s* variable with the Z-form [54]:

$$s = \frac{(z-1)}{z * T_s}$$

(8-7)

Function PI(s) becomes:

$$PI(z) = K_i * \left(\left(\frac{\left(1 + \frac{z-1}{z * T_s} * \frac{K_p}{K_i}\right)}{\frac{z-1}{z * T_s}}\right)\right) = \frac{\left(K_p + K_i * T_s\right) * z - K_p}{z-1}$$

$$= K_p + K_i * T_s * \frac{z}{z-1}$$

(8-8)

A new rational transfer function is obtained that can be simplified to give discreet time implementation of PI Controller which can be seen in block diagram below [54]:

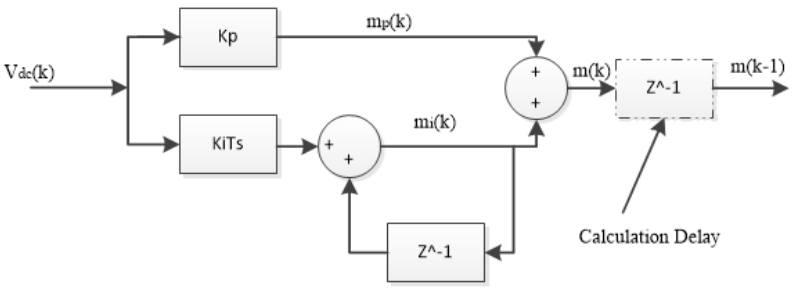


Figure 8.1-9: Block diagram representation of the digital PI controller

This figure (8.1-9) represents the parallel realization of the discreet time regulator, followed by a possible model of calculation delay. Using Z-Transform properties; the control algorithm may be used to implement the PI regulator in this microcontroller which is as follows [54]:

$$m_{i(k)} = K_i * Ts * V_{dc}(k) + mi(k-1)$$
$$m(k) = m_{p(k)} + m_{i(k)} = K_p * V_{dc(k)} + m_{i(k)} \quad (8\text{-}9)$$

Equation (8-8) is very similar to equation (8-9); only the integral part that is not based on a single current error value, but rather on the moving average of the two most recent current error samples which is liable for the lower frequency response distortion of the Tustin transform. Additionally, it can be seen that the proportional and integral gains for the two different versions of the discretized PI controller are exactly the same and also the application of preparing does not change much the values of the controller gains; especially when a relatively high ratio between the sampling frequency and the desired crossover frequency is possible [54].

In summary, we have seen that, given a suitably designed analog PI regulator, the application of any of the considered discretization strategies simply requires the computation of the digital PI gains, as in the following [54]:

$$Ki_{dig} - K_i * T_s$$
$$K_{p_{dig}} = K_p \tag{8-10}$$

Last but not least, the added delay block to the controller block makes it possible to calculate the effect of the delay on the control performance and closed loop system stability using any kind of system modeling or simulation software. This case shows the worst case scenario which is calculation delay almost equal to sampling period. More important, the design of the original analog PI controller was performed *neglecting* the calculation delay, so inclusion in digital controller model might affect the dynamic performance of the system [54].

For single phase asymmetric rectifier, the PI parameters are tuned using the auto tuning function provided by Matlab SISO tool. Nonetheless, the same values can be obtained by pole placement methodology [55] [56]. It can be seen the system is stable with a bandwidth of 841 Hz and gain 60 degrees phase margin. Fig.8.1-10, Fig. 8.1-11 and Fig. 8.1-12 shows the system bode plot, root locus and time step response respectively of the system's open loop gain.

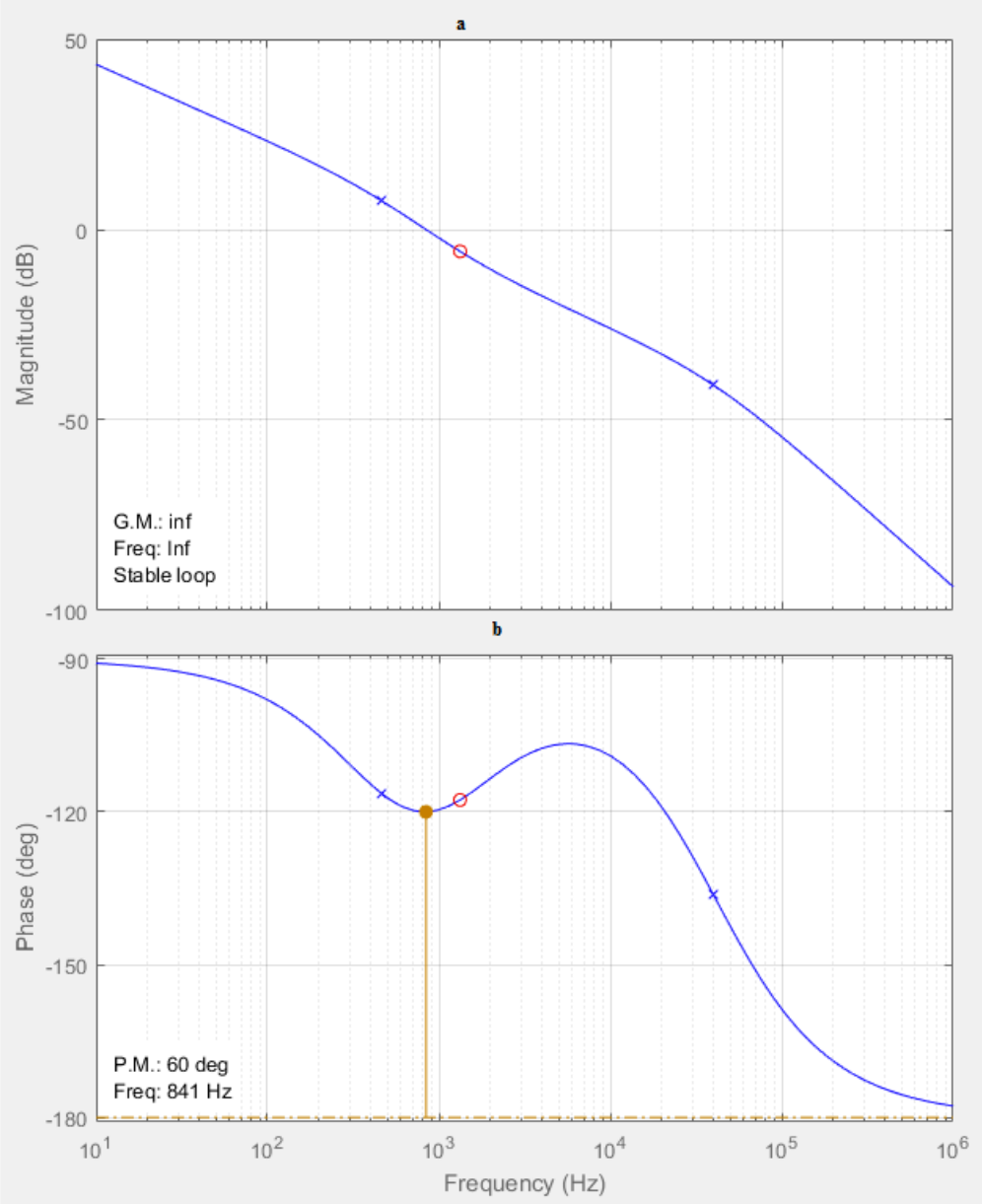


Figure 8.1-10: Magnitude and Phase Diagram

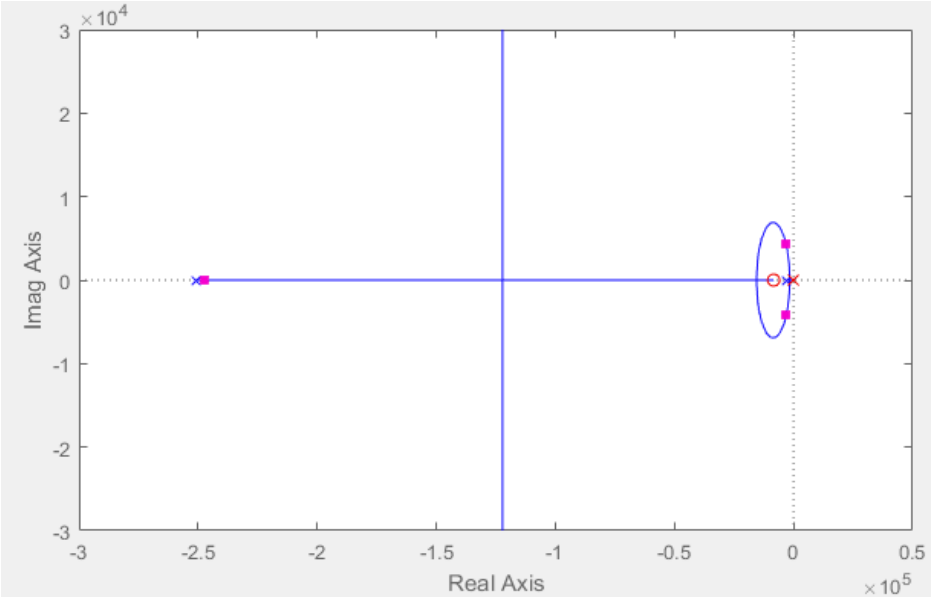


Figure 8.1-11: Root Locus Plot

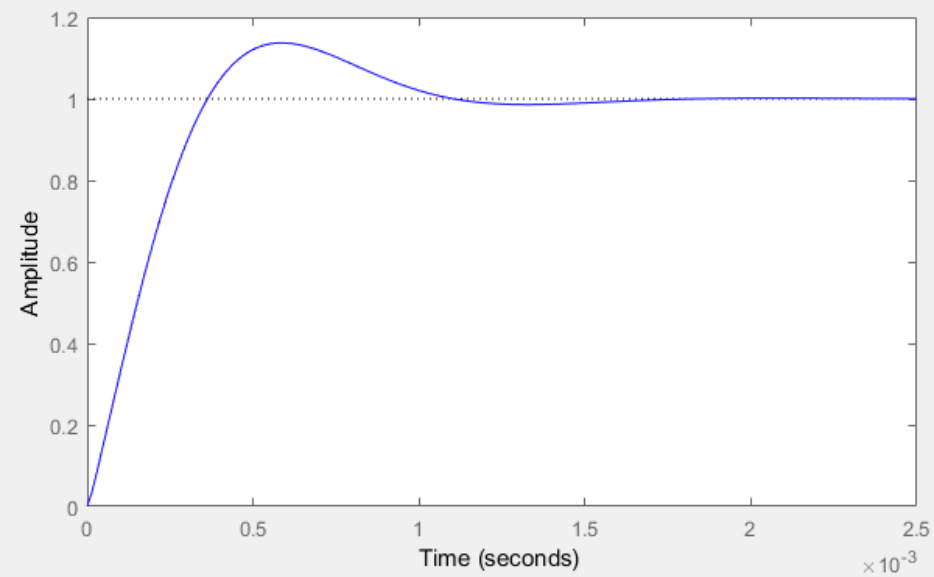


Figure 8.1-12: Time-Step Response

8.2. Model of Active Rectifier (VICC)

This section provides additional information of the VICC controller (Section 6.3). Using Fig. 6.3-4 it can be noted that for the continuous switching vector, which components are the duty cycle of each converter leg $-1 \leq s_{j(t)} \leq 1$ $(j = a, b, c)$ is defined as [38]:

$$s'(t) = (\frac{2}{3})(s_a(t) + \alpha * S_{b(t)} + \alpha^2 * s_{c(t)})$$

(8-11)

Additionally, equation (6-4) can be linearized considering $v_{output}(t) = V_{output}$ with V_{output} being a constant, hence, instead of continuous switching vector V_{avg} is used and equation (6-5) can be written as equation (8-12):

$$\frac{di_d(t)}{dt} - \omega i_q = \frac{1}{L}\left[-Ri_d(t) + e_d(t) - \frac{1}{2}p_d(t)v_{0output}(t)\right]$$
$$\frac{di_q(t)}{dt} + \omega i_d = \frac{1}{L}\left[-Ri_q(t) + e_q(t) - \frac{1}{2}p_q(t)v_{0output}(t)\right] \quad (6\text{-}4)$$

$$\frac{dv_{output}(t)}{dt} = \frac{1}{C}\left\{\frac{3}{4}\left[p_d(t)i_d(t) + p_q(t)i_q(t)\right] - i_L(t)\right\} \quad (6\text{-}5)$$

$$\left(\frac{d}{dt}\right)\begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} = \begin{vmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{vmatrix}\begin{matrix} i_d(t) \\ i_q(t) \end{matrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \end{bmatrix}\begin{bmatrix} v_{d,av}(t) \\ v_{q,av}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} e_d(t) \\ e_q(t) \end{bmatrix}$$

(8-12)

Equation (8-12) is linear. Both control loops of active and reactive power can be seen in Fig. 8.2-1. This figure displays disturbance (account all the neglected phenomena) as *w*. Zero Order Hold (ZOH) is suitable model of analogue to digital conversion as it introduces half a sampling period delay (value considered into account of the modulator influence). ZOH is represented by *G(z).* Furthermore, for technical optimum the PI integrator time constant T_I needs to be equal to plant time constant *T* and constant K_p *where* [38]*:*

$$K_p = \frac{L}{3T_s}$$

(8-13)

Accordingly, the current loop bandwidth f_{bi} is:

$$f_{bi} = \frac{1}{6\pi T_s} \approx \frac{1}{20T_s}$$

(8-14)

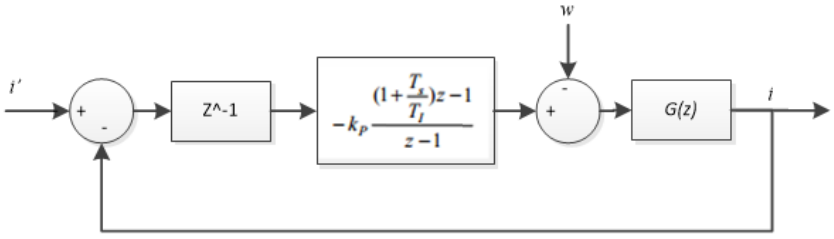


Figure 8.2-1: Current control loop in Z-domain

The DC voltage is obtained through the control of power exchanged by the converter. The change is DC power voltage is taking more or less power from the grid in comparison to what is required by the load, which therefore, changes the reference value for AC current loops. The voltage loop is an outer loop and current loop is an inner loop (Fig. 6.3-5). The outer loop can be designed to be somewhat slower (5-20 times) as compared to inner loop as its main job is to handle stability and optimum regulation. This allows loops to be decoupled making the current components to be equal to their reference when designing the outer DC controller. Hence based on equation (6-5) and considering current is equal to its reference value $i_{d(t)} = i'_d(t),\ i_q(t) = i'_q(t) = 0\ and\ s_d(t) = S_d,\ s_q(t) = S_q$ [38]:

$$\frac{dv_{output}(t)}{dt} = \frac{1}{C}\left\{\frac{3}{4}[S_d i'_d(t)] - i_L(t)\right\}$$

(8-15)

DC voltage control is performed through the selection of $i'_d(t)$ using a cascaded controller. Fig. 8.2-2 shows the voltage control loop in S-domain. This includes the current loop transfer function and a PI controller which helps with optimum symmetrical.

Crossover frequency is represented by ω_c of the open loop and phase margin is represented by ψ. ω_c can be determined by [38]:

$$\omega_c = \frac{1}{3aT_s} \tag{8-16}$$

where,

$$a = \frac{1 + cos\psi}{sin\psi} \tag{8-17}$$

where, a parameter is responsible for both the crossover frequency and the phase margin. Therefore, the controller parameters are as follows:

$$K_p = \frac{4C}{9aS_dT_s}$$
$$T_I = 3a^2T_s \tag{8-18}$$

To have two complex conjugate poles at the closed loop transfer function critically damped (*a =2.4):*

$$k_p = 0.19\frac{C}{S_dT_s}$$
$$T_I = 17T_s \tag{8-19}$$

Accordingly, the voltage loop bandwidth is:

$$f_{bw} = \frac{\omega_c}{2\pi} = \frac{1}{6\pi aT_s} \approx \frac{1}{50T_s} \tag{8-20}$$

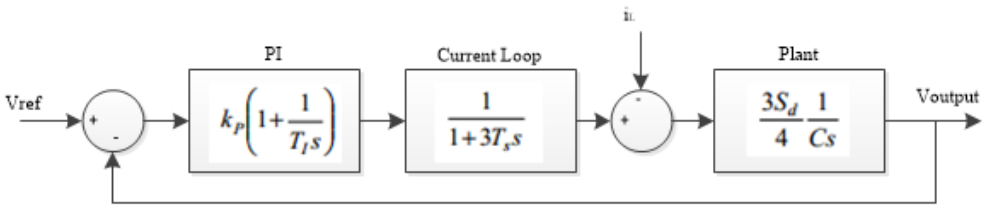


Figure 8.2-2: Voltage control loop in S-domain

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