Controlling the Vienna Rectifier Using a Simplified Space Vector Pulse Width Modulation Technique

by

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

ABSTRACT

In this thesis, a simplified Space-Vector Pulse-Width-Modulation (SVPWM) technique for the Vienna rectifier is introduced to reduce the computational burden, the switching losses and the Total-Harmonic-Distortion (THD). Furthermore, the robustness of this modulation technique is tested under various faults through a 70 kW MATLAB/Simulink model and the results are validated through 1.2 kW prototype. The results reveal that the simplified SVPWM provides a low THD, unity Power-Factor (PF) and effective capacitor voltage balancing even after extreme faults.

This study introduces a multilevel Power-Factor-Correction (PFC) converter in a 2-stage configuration. The first stage is the Vienna rectifier which has a high boosting ratio. To overcome this issue, a high efficiency 4-switch converter is cascaded with the Vienna rectifier. This converter employs storage-less passive components and provides a Zero-Current-Switching (ZCS) for all of its switches. A description of the converter is first introduced followed by the simulation results.

Keywords: PFC; Multi-level rectifier; Vienna rectifier; soft switching; space vector modulation

AUTHOR'S DECLARATION

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STATEMENT OF CONTRIBUTIONS

The main contribution in this thesis is implementing the simplified Space Vector Pulse Width Modulation (SVPWM) for the Vienna rectifier and verifying the robustness of this method under extreme faults. In addition, the functionality of the SVPWM method is verified by experimental results. This contribution is explained in Chapters 5, 6 and 8 and has been published in:

- **A. Sunbul** and V. K. Sood, "Simplified SVPWM Method for the Vienna Rectifier," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-8.

Furthermore, a submission is in the process to:

- **A. Sunbul**, A. Sheir, V. K. Sood, “Study of The Robustness of Vienna Rectifier Under Fault Conditions Using Simplified Space Vector”, in Canadian Journal of Electrical and Computer Engineering, spring 2020, (In progress).

The other contribution in this thesis is to overcome the issue of Vienna rectifier’s high boosting ratio by cascading a highly efficient second stage to it. The second stage employs a soft-switching technique and storage less passive components which keeps the system highly efficient and small in size. This contribution is described in Chapter 7 and has been published in:

- **A. Sunbul**, A. Sheir, V. K. Sood," High Performance Multilevel Power Factor Correction Boost-Buck Converter," 2019 IEEE Electrical Power & Energy Conference (EPEC), Montreal, QC, 2019, pp. 1-6.

Furthermore, a submission is in the process to:

- **A. Sunbul**, A. Sheir, V. K. Sood, "High Performance Multilevel Power Factor Correction Boost-Buck Converter," in Canadian Journal of Electrical and Computer Engineering, spring 2020 (Submitted).

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LIST OF ABBREVIATIONS AND SYMBOLS

A	Ampere
AC	Alternative Current
ADC	Analog-to-Digital Converter
DC	Direct Current
div	Division
EMI	Electromagnetic Interference
EV	Electrical Vehicle
F	Farad
FET	Field-Effect Transistor
H	Henry
Hz	Hertz
k	Kilo
m	milli
MCU	Microcontroller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation
R	Resister
s	Second
SD	Secure Digital
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
u	micro
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
V	Volt
W	Watt
ZCS	Zero Current Switching
Ω	Ohms

Chapter 1. Introduction

1.1. Motivation

Most countries must find a source of renewable energy that can cover the demand increment and reduce the dependency on fossil fuel so that greenhouse gases may be reduced. The production of electricity is one of the main sources of carbon emissions which leads to global warming. To overcome this issue, the power efficiency of distribution systems must be improved. By increasing the efficiency of most commonly used Alternative Current (AC) to Direct Current (DC) rectifiers, higher power quality in distribution systems will be achieved, less energy will be consumed and less pollution will be generated at the electrical distribution systems. Electrical distribution systems supply an Alternative Current (AC) to consumers. However, increasingly a majority of the consumers' loads require a Direct Current (DC) to function; hence, AC to DC rectifiers are needed to make the utility's electricity usable for DC loads. In the last decade, much research has been done on AC to DC rectifiers but there is more to be done in this field. AC to DC rectifiers use diode-bridges to rectify the AC voltage to constant DC voltage. However, the diode-bridge draws a non-sinusoidal current with a low Power Factor (PF) which is not effective for high power applications as it reduces the efficiency and power quality. Therefore, rectifier topologies that draw high quality sinusoidal current should be used. Generally, AC to DC power rectifiers can have two, three, or more voltage levels, depending on the topology, but the complexity increases as the voltage levels increase. In addition, rectifiers can have 1-phase or 3-phase topologies. For high power application, 3-phase topologies are preferred to reduce the components stress and size.

1.2. Objectives

The aim of this research is to develop a Power Factor Correction (PFC) rectifier for both low and high power applications. However, it can also be applied in the first stage of a wind turbine energy system. The wind turbine generates an unusable AC voltage with a variable frequency. This AC voltage is then converted to DC voltage by the developed AC to DC rectifier. A DC to AC inverter is used to convert the voltage to a usable AC voltage with a fixed frequency. The specified objectives of this thesis are listed as follows:

- To develop a high efficient AC to DC conversion with regulated output voltage, low Total Harmonic Distortion (THD) and unity PF by using fewer active switches.
- To reduce the stress and losses of the switches that are employed in the rectifiers.
- To study the functionality of 2-level and 3-level Space Vector Pulse Width Modulation (SVPWM) method in 3-phase rectifiers.
- To reduce the complexity and computational effort of the SVPWM method.
- To analyze the Vienna rectifier using a simplified space vector method.

1.3. Thesis overview

This thesis is comprised of eight chapters. In Chapter 1, an introduction to the thesis is provided, including the motivation and objectives. Chapter 2 covers the background knowledge of PFC rectifiers. It also includes the classification of these rectifiers. This chapter also provides a literature study that investigates the advantages and disadvantages of various rectifier topologies and their modulation techniques. In chapter 3, an introduction to the Vienna

rectifier is provided. The properties and operations of the Vienna rectifier is analyzed in this chapter. Chapter 4 includes a brief introduction to the 2-level SVPWM method. This chapter covers the transformation used in SVPWM methods, the available switching states, space vectors and Dwell time calculation. Chapter 5 provides a detailed space vector analysis for the Vienna rectifier. The space vectors for the Vienna rectifier is derived mathematically. Also, a detailed explanation of the simplified space vector method is illustrated. Finally, the control circuit for the Vienna rectifier is explained in this chapter. Chapter 6 illustrates MATLAB/Simulink simulation results of the Vienna rectifier using the simplified SVPWM technique. The simulation results of the system under extreme fault conditions is also illustrated in this chapter. Chapter 7 introduces an integration of the Vienna rectifier with a soft-switched buck converter to provide a high efficient system for low output voltage application. The analysis and simulation results for the proposed system are outlined in this chapter. In Chapter 8, the validity of the simplified SVPWM is checked under several fault conditions using a 2.4 kW prototype. In this chapter, the details of hardware implementation are provided. Additionally, the experimental results are illustrated and discussed. Chapter 9 provides a conclusion and discusses the potential for future work.

Chapter 2. Background and Literature Review

2.1. Background

2.1.1. Problem statement

2.1.1.1. PFC Converters:

Several kinds of electronic equipment are interfaced with the supply grid. Passive loads normally draw sinusoidal current from the utility grid and they do not affect the operation of other equipment that are interfaced with the grid. However, the rapid switching of currents in power electronic devices causes harmonic distortion in the mains network. These harmonics may interfere with other electronics devices connected to the same grid. The switching behavior of power electronics devices reduces the power quality and efficiency. It causes the utility companies to supply extra power to the equipment and requires strong coupling to account for the circulating currents [1]. To overcome this issue, PFC topologies are proposed to make these switching behaviours appear as resistive loads (with a unity power factor) to the mains. The mains voltage is usually converted to a DC voltage and then adapted to the voltage needed by the load. A major drawback of the conventional PFC topologies is the inability to regulate the DC output voltage. For this reason, they are usually implemented using two stage conversions. The first stage is the diode bridge followed by a DC-link capacitor. The second stage is a DC to DC converter which takes the DC-link capacitor voltage as its input and provides a regulated DC output voltage as illustrated in Figure 2.1. However, improved PFC topologies, which have the capability to regulate the DC output voltage within one stage, do exist, as illustrated in Figure 2.2. These topologies are known as Single-stage PFC converters.

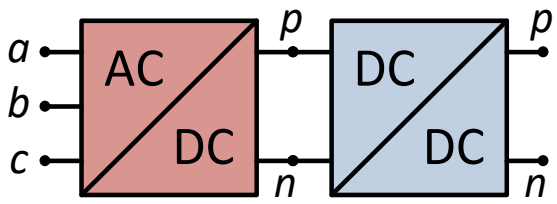

Figure 2.1: Configuration of 2-stage PFC converters

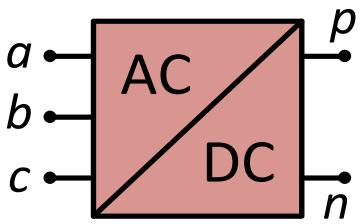

Figure 2.2: Configuration of single-stage PFC converters

The impact of the power electronic converters seen by the mains is partly described by the PF - the angle displacement between the fundamental current to voltage - and, partly by the current THD. The PF equation is derived in this section.

The grid-connected power electronic converters can be represented by the basic circuit in Figure 2.3 and the vector representation of the voltage and current is shown in Figure 2.4.

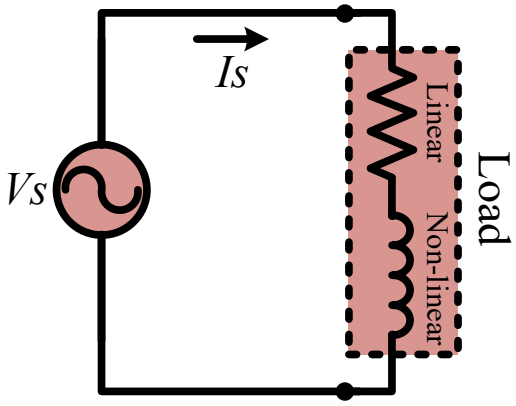

Figure 2.3: Representation of grid-connected power electronic converters

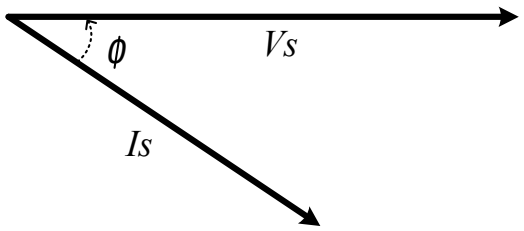

Figure 2.4: Vector representation of the grid's voltage and current

The PF can be calculated as:

$$\text{Power Factor (PF)} = \sin(\Phi) = \frac{\text{Vs}}{\text{Is}} \tag{1}$$

However, in the diode bridge rectifier the current waveform does not have a sinusoidal shape, which causes the PF equation to change as follows [1]:

$$\text{PF} = \frac{\text{DPF}}{\sqrt{1 + \text{THD}^2}} \tag{2}$$

Where DPF is displacement PF.

$$\text{DPF} = \sin(\Phi_1) = \frac{\text{Vs}}{\text{I}_{\text{S1}}} \tag{3}$$

where I_{S1} is fundamental component of the supply current,

$$\text{PF} = \frac{\text{I}_{\text{distortion}}}{\text{I}_{\text{S1}}} \tag{4}$$

Table 2.1: Advantages and disadvantages of PFC rectifier [1]

PFC Rectifiers	
Advantages	**Disadvantages**
Better source efficiency	Introducing greater complexity into the design.
Lower power installation cost	Having more parts adversely affects reliability.
Lower conducted EMI	The generation of EMI and radio frequency interference (RFI) by the active PFC circuits requires extra filtering, making the input filter more complex and more expensive.
Reduced peak current levels	More parts require a more costly power solution.

2.1.2. Classification of Rectifiers:

PF circuits can be classified in two categories [1]:

1- Input PFC

2- Output PFC.

The system is categorized as input PFC when the grid is supplying a nonlinear load and the PFC circuit is placed at the input side. However, when the PFC circuit is placed between the load and the power supply, the system is called output PF. In this thesis, the input PFC system is investigated since it targets a wider range of applications.

The PFC circuits are classified into three categories based on the components as shown in Figure 2.5 and listed as follows:

2.1.2.1 Passive PFC Topologies

Passive PFC circuits use passive components, such as inductors, capacitors, diodes and thyristors, to correct the displacement between the line current and the line voltage. They are purely mains commuted and do not contain any turn-off power semiconductors, which makes it impossible to regulate the output DC voltage. Examples of passive PFC circuits are given in Figure 2.5. Passive circuits are used in industry for high power applications (>100 kW) as higher current harmonics are allowed when supplying from a medium voltage mains [2].

2.1.2.2 Hybrid PFC Topologies

Hybrid PFC circuits mainly consist of passive components with partial integration of active elements such as turn-off power semiconductors. In this system, a diode bridge is connected to the input side while the semiconductors switch is placed at the DC side of the

rectifier. This implies that voltage regulation and sinusoidal input current is possible but they could be limited [2].

2.1.2.3 Active PFC Topologies

Active PFC circuits are fully forced-commuted which use the turn-off power semiconductors in the bridge itself. They are capable of regulating the DC output voltage and shaping the input current. Since active PFC circuits are better than both passive and hybrid PFC circuits in regulating the DC voltage, they are considered in this thesis.

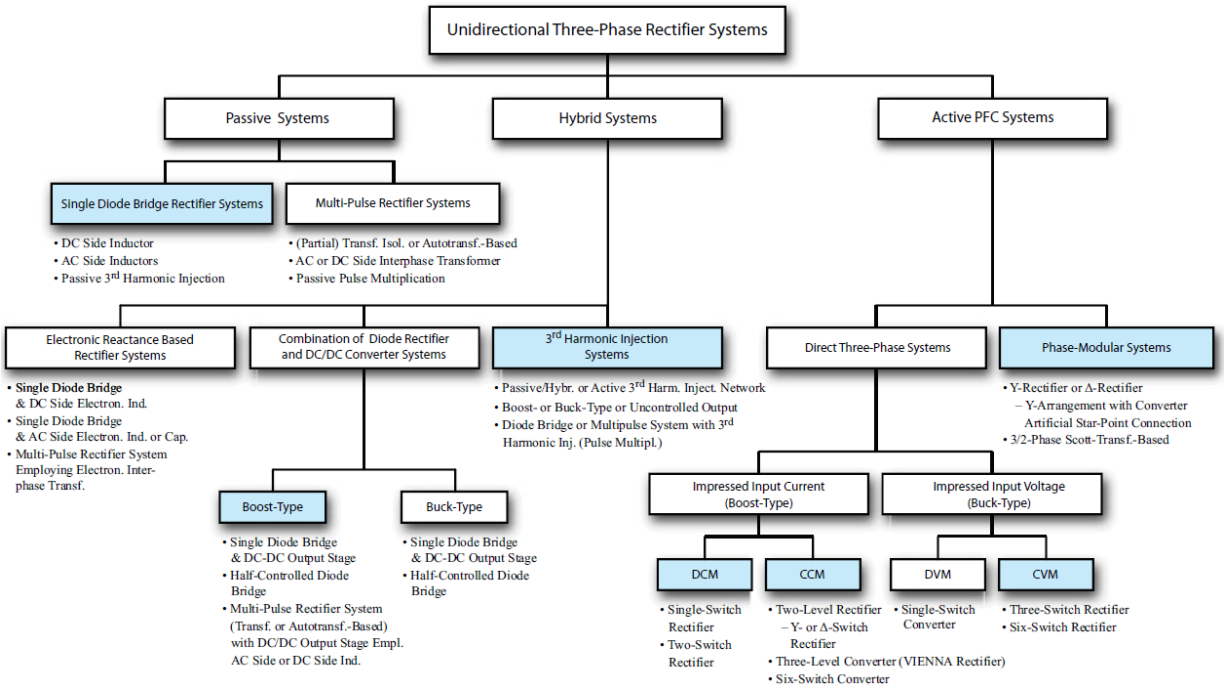

Figure 2.5: Classification of unidirectional 3-phase rectifiers [2]

2.2. Literature Review

2.2.1. Direct 3-phase PFC Rectifiers:

As illustrated in Figure 2.5, direct 3-phase active PFC rectifiers have two different topologies: buck and boost. In this thesis, 3-phase single-stage PFC rectifiers that provide sinusoidal input current, less than 5% THD and controlled output voltage are considered in the

literature review. Several PFC rectifiers under these standards are provided in the literature, [3 – 6]; however, only a few are preferred in the industry, such as 6-switch buck rectifier (Figure 2.6) and SWISS rectifier (buck-type) (Figure 2.7), Vienna rectifier (boost-type), and 6-switch boost rectifier [2]. These rectifiers provide low semiconductors voltage stress, low electromagnetic interference noise, high power density, and efficiency [2]. By comparing both buck-type rectifiers, the Six-switch rectifier is preferred since its total loss is 1.2 times higher than the SWISS rectifier [7]. In addition, another reason why the topology of the SWISS rectifier is preferred is that it requires five active switches while 6-switch rectifier requires six active switches. Generally, the disadvantage of these two Buck-type rectifiers is that the input current is not directly affected by the controller [7]. In addition, the efficiency in both buck-type rectifiers is less than the boost-type rectifiers mentioned above, and they require a higher number of active and passive components. Therefore, Boost-type rectifiers are investigated in this thesis.

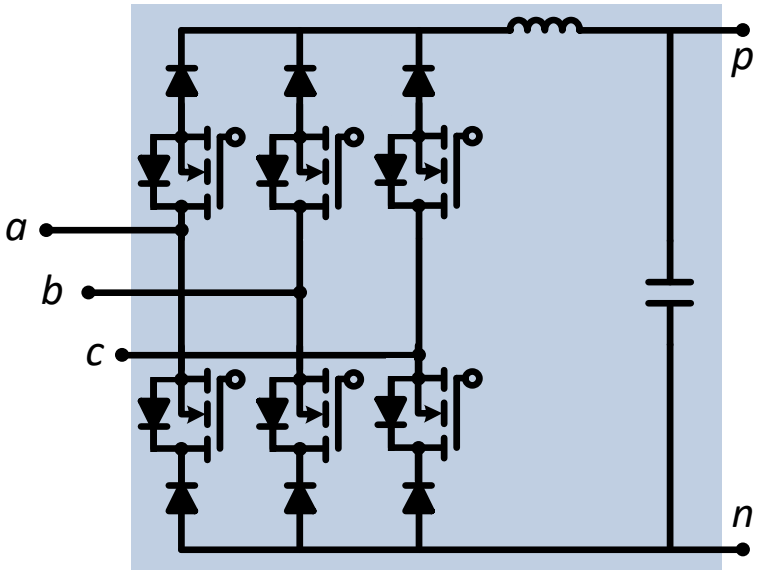

Figure 2.6: Configuration of the 6-switch buck rectifier

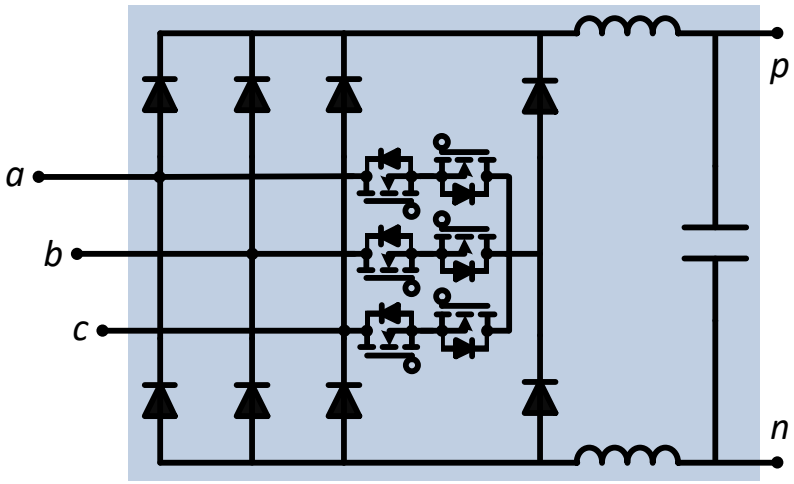

Figure 2.7: Configuration the Swiss rectifier

2.2.2. 3-phase Boost PFC Rectifiers:

In this thesis, 3-phase, PFC, boost topologies are investigated. The idea of 3-phase boost topologies is derived from the conventional hybrid 2-stage, single-phase boost circuit shown in Figure 2.8, where the boost inductor is located at the second stage after the diode bridge and the active switch is located in parallel with the DC-link capacitor.

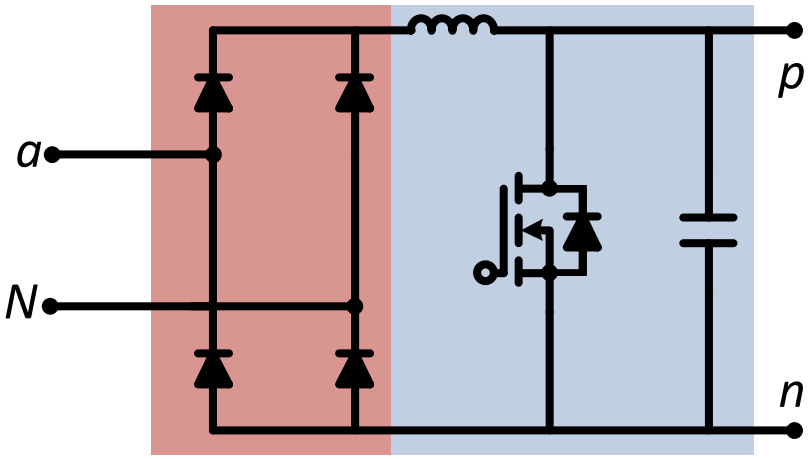

Figure 2.8: Configuration of the conventional hybrid 2-stage single-phase boost rectifier

Similar to Figure 2.8, the topology in Figure 2.9 is extended into 3-phase, which contains a diode bridge that is connected to the rectifier input, followed by the inductor and the active

switch before the DC-link capacitor. This topology provides the ability to regulate the DC output voltage. However, the blockage nature of the diode bridge increases the current distortion (THD = 30%) [8].

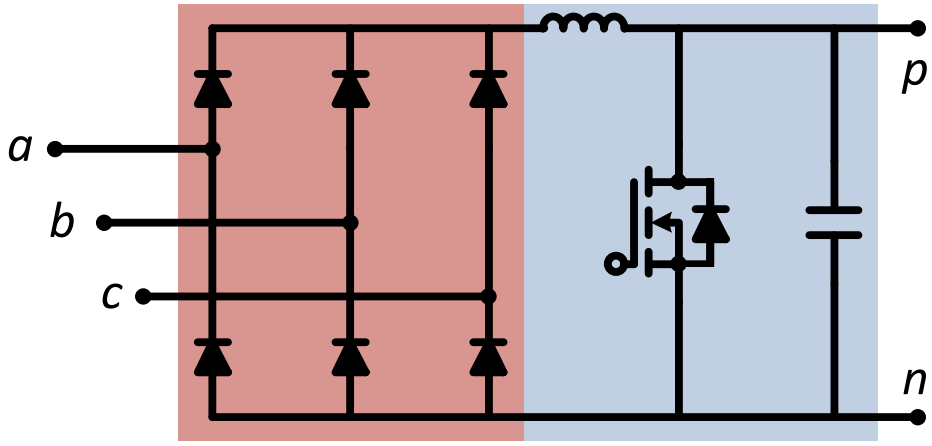

Figure 2.9: Configuration of 3-phase boost PFC rectifier

To improve the THDi in the circuit shown in Figure 2.9, the inductor filter is moved to the input of the rectifier and distributed in the phases as shown in Figure 2.10, and the mode of operation is changed to Discontinues Conduction Mode (DCM). This change leads to a better sinusoidal shape for the input current, however, a low frequency distortion still appears at low voltage transfer ratio [9].

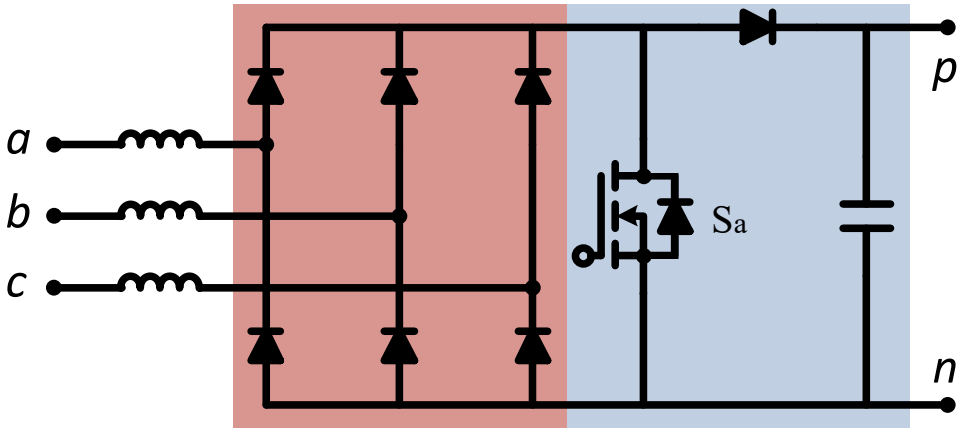

Figure 2.10: Configuration of 3-phase boost PFC rectifier with shifted inductors to the input

A hybrid third harmonic current injection PFC Rectifier, shown in Figure 2.10, is proposed to improve the phase current shape. The improvement is attained by introducing a new switch to control the positive and negative DC bus current. This topology results in a sinusoidal waveform for the input current [10]. In this topology, the current is injected in only one phase at the time, which is decided by the 4-quadrant switches (Sa). This is called a purely passive injection network, which requires large volume and weight. Therefore, other topologies are preferred to improve the efficiency and reduce the component sizing [2].

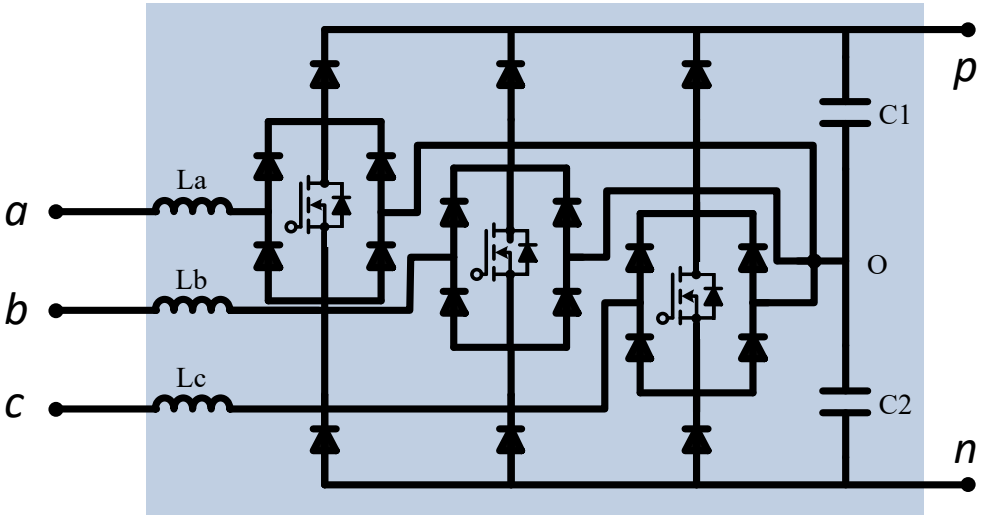

Figure 2.11: Configuration of the Vienna rectifier

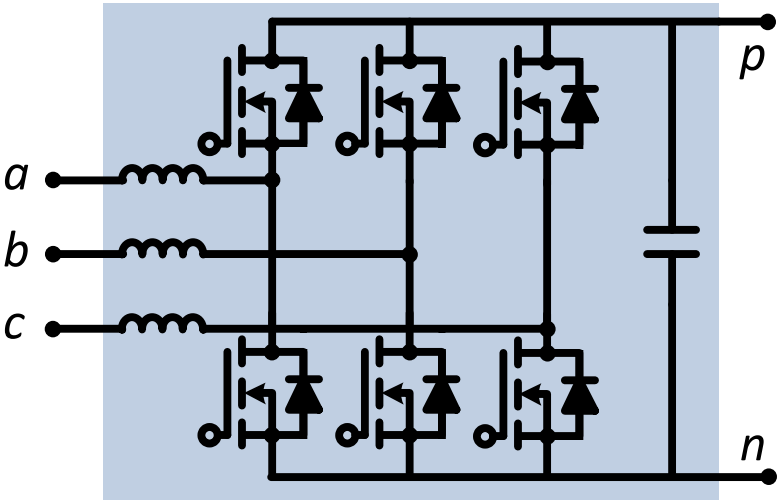

Figure 2.12: Configuration 6-Switch boost rectifier

Figures 2.11 and 2.12 depict both the Vienna and 6-Switch boost rectifiers respectively. Both of these boost-type rectifiers are preferred in the industrial applications because of their high power density. However, the switching losses in the 6-Switch boost rectifier is higher than the Vienna rectifier by a factor of 2.5 and the total efficiency in Vienna rectifier is 20% higher [7]. Moreover, the inductance filter in the Vienna rectifier is half the size of the 6-Switch boost rectifier and its degree of freedom is higher since it has a 3-level characteristic [7]. One of the main advantages of the Vienna rectifier is the reduced voltage stress on the switches due to the 3-level characteristics. In addition, small boost inductors are required while sinusoidal current waveform with low THDi, high efficiency, and power density are gained. Due to these advantages, the Vienna rectifier is chosen for further investigation in this thesis.

2.2.3. Modulation Techniques for the Vienna Rectifier:

The 3-phase, 3-switch, 3-level Vienna rectifier is widely used in several applications, such as for telecommunication supplies and off-board Electric Vehicle (EV) charging etc. [11 - 12]. For applications in the range of several kilowatts, the Vienna rectifier is able to function well above 100 kHz switching frequency depending on electromagnetic compatibility (EMC) requirements [13]. Several researchers have employed sinusoidal Pulse Width Modulation (PWM) and hysteresis modulators to improve the performance of the Vienna rectifier, which is easily built using simple analog circuits [14 - 16]. On the other hand, these types of modulators increase the harmonics since it works in an inconstant switching frequency. To reduce the harmonics, digital controllers based on Field Programmable Gate Arrays (FPGA) and Digital Signal Processors (DSP) are used with constant switching frequency [17 - 21]. Although several modulation techniques have been applied to the Vienna rectifier, the SVPWM method has shown an excellent performance [22]. Another advantage of the SVPWM

is the ability to modify the location and timing of the pulses, which is an important factor for eliminating certain harmonics. Using SVPWM for the Vienna rectifier provides an extra advantage of balancing the DC-link's voltage by changing the time ratio of the two redundant switching states [23 - 27]. Numerous research studies have employed SVPWM for this rectifier; many studies have focused on neutral point balancing [28 - 30], where others proposed methods to improve the zero crossing distortion [31-33]. SPVPWM is also tested under unbalanced load conditions [34 - 36]. However, only limited research studies are focused on improving the main disadvantages of this modulation technique which are the high complexity and the high computational requirement such as [13], [37 - 39]. In this research, a further simplified SVPWM technique, first proposed in [40], is analysed and explained in detail. This method shows a significant reduction in the complexity and computational requirements. However, this simplified technique has not been implemented and its results have not yet been reported in the literature. Moreover, in this thesis, the modulation technique is tested under different extreme faults, such as a sudden load change, unbalanced capacitor voltages, capacitor mismatch and capacitor short-circuit, to check its capability and limitations. MATLAB/Simulink simulation results of the Vienna rectifier using the simplified SVPWM technique are provided.

Chapter 3. The Vienna Rectifier

This chapter provides an introduction to the Vienna rectifier, followed by a detailed explanation of its topology and properties. The bidirectional switches used in this topology are discussed. Finally, the mode of operations and the produced voltage level are explained.

3.1. Introduction to Vienna Rectifier

The Vienna rectifier (shown in Figure 3.1) is a 3-phase, 3-level and 3-switch (controllable) rectifier which was invented by Johann W. Kolar in 1994. It has been commonly used for several high power applications due to its high efficiency, high power density and low THD. The invention of the Vienna rectifier has reduced the number of controllable switches of 3-phase rectifiers into three switches, as opposed to the conventional rectifier, which has six switches. In this rectifier, the required AC filters are relatively small as compared to conventional rectifiers. The switching losses are minimized while the converter boost ratio is increased in this topology.

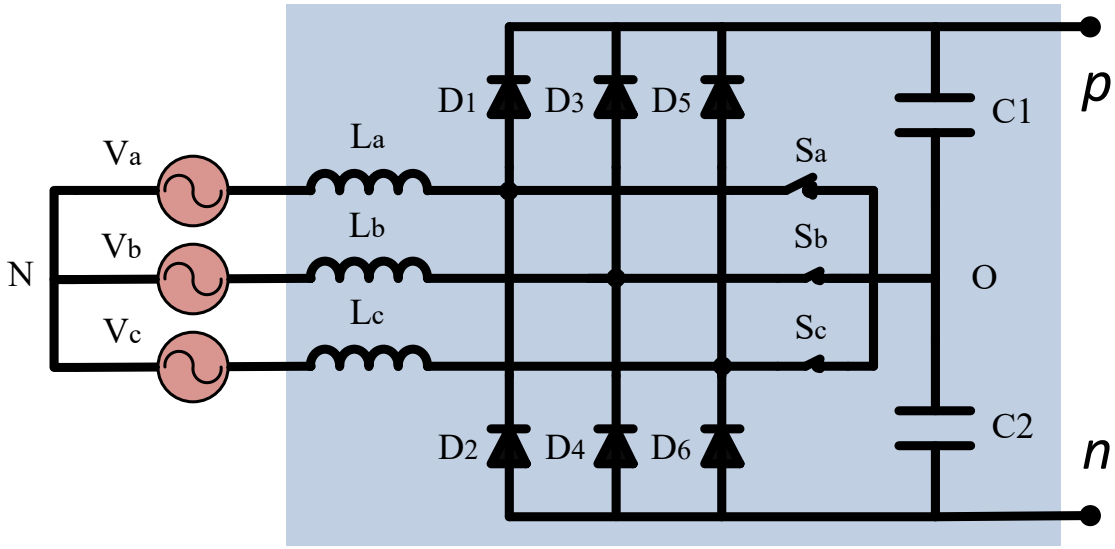

Figure 3.1: Basic topology of the Vienna rectifier

Indeed, it is well known that the main challenges in rectifiers are improving the PF and injecting sinusoidal input current. However, the Vienna rectifier has met these challenges by achieving unity PF and injecting sinusoidal input current from the mains. Moreover, the Vienna rectifier has the capability of performing well under unbalanced circumstances. In the next section, the topology of the Vienna rectifier is discussed.

3.2. Vienna Rectifier Topology:

The Vienna rectifier is similar to the conventional 3-phase diode bridge rectifier, where three inductors are connected to the input of each phase. However, the output is attached to two capacitors, which are connected to a point called “capacitor midpoint (o)”. The inductance filters create a current source while the capacitive filters create a voltage source. The currents produced by the inductors are injected to the capacitor midpoint through three active switches Sa, Sb and Sc. They can also charge or discharge the capacitors mid-point. Bidirectional and bipolar switches are required to fulfill the topology’s requirements. As illustrated in Figure 3.2, each switch contains four diodes and a transistor to create a bidirectional switch. There are four ports in the bidirectional switch. Ports P1 and P4 are connected to the input inductance and capacitor mid-point respectively, whereas ports P2 and P4 are connected to the diodes of the rectifier’s system.

Figures 3.3 to 3.6 illustrate how the current flows in the switch. Four different paths can be taken by the currents. As shown in the Figures 3.2 to 3.6, when the transistor is OFF and the phase current is positive, the current flows from port P1 to port P3 through diode Da1. However, when the transistor is turned ON, the current flows from port P1 to port P4 using diode Da1, transistor S and diode Da4. On the other hand, the current travels from port P3 to port P1 through diode Da3 when the current is negative and the switch is OFF. In contrast, the

current uses diode Da2, transistor S and diode Da3 to travel from port P4 to port P1 when the switch is turned ON.

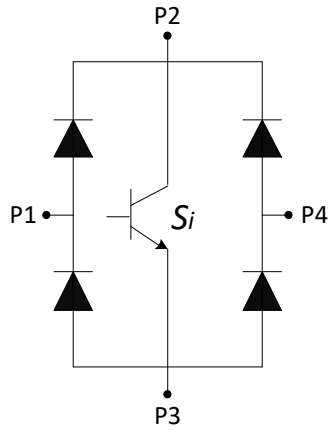

Figure 3.2: Bidirectional bipolar switch

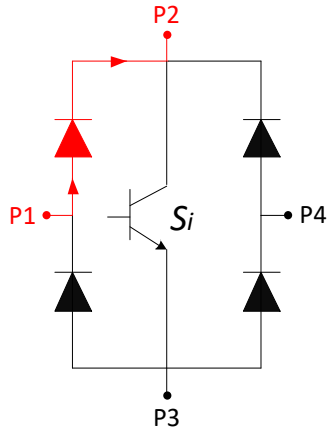

Figure 3.3: Current flow in the switch when the current is positive and the transistor is turned OFF

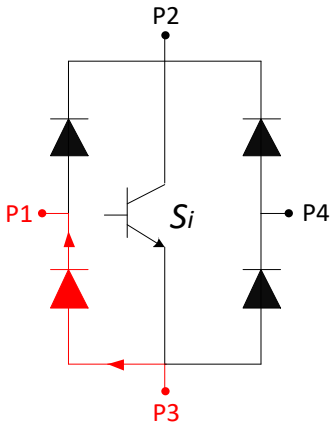

Figure 3.4: Current flow in the switch when the current is negative and the transistor is turned OFF

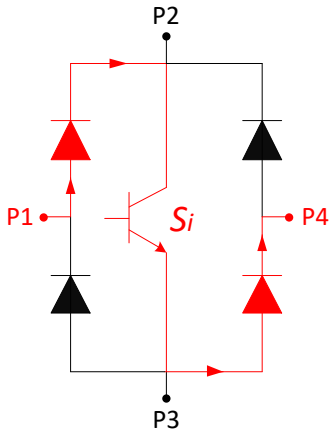

Figure 3.5: Current flow in the switch when the current is positive and the transistor is turned ON

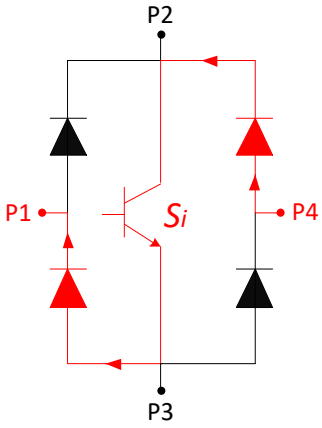

Figure 3.6: Current flow in the switch when the current is negative and the transistor is turned ON

The switches Sa, Sb and Sc (shown in Figure 3.1) are replaced by the bidirectional bipolar switch shown in Figure 3.2. These three bidirectional bipolar switches are integrated into the diode bridge of the rectifier system. As shown in Figure 3.7, each phase in the Vienna rectifier consists of six diodes and a transistor.

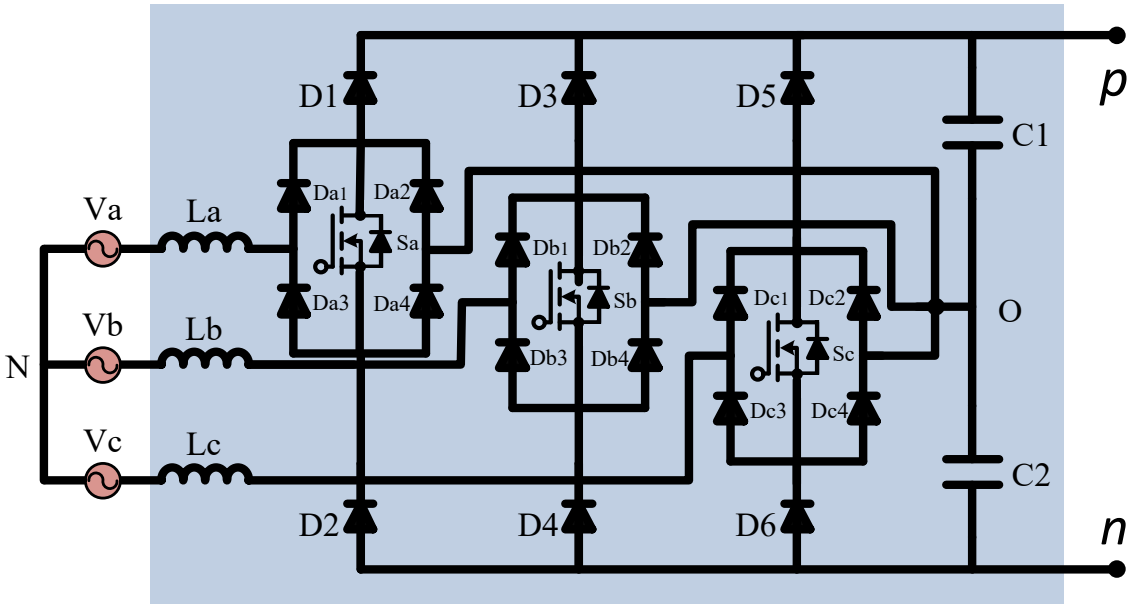

Figure 3.7: Integrating Vienna Rectifier Circuit with the bidirectional bipolar switch

3.3. The Properties of the Vienna Rectifier:

3.3.1. The Degree of Freedom in the Vienna Rectifier

Unlike the conventional 3-phase, 2-level diode bridge rectifier, the Vienna rectifier has a limited degree of freedom as it does not have controllable switches in each phase leg. Instead, it has three switches that connect the rectifier's input to the capacitor mid-point. Moreover, turning the switches ON and OFF is not the only controlling factor in this rectifier since the direction of the phase currents decides which voltage level is applied to the rectifier (positive or negative). In other words, the position of the switches and the current directions are the two controlling factors in the Vienna rectifier.

3.3.2. The Operation of the Vienna Rectifier

Since the Vienna rectifier is a 3-switch rectifier, it has eight possible switching states. However, as a 3-phase system, there are six possible sectors based on the polarity of the grid as follows:

Sector 1: Current in phase A is positive, while in phases B and C, they are negative (+,-,-).

Sector 2: Currents in phase A and B are positive, while in phase C it is negative (+, +, -).

Sector 3: Currents in phases A and C are negative, while in phase B it is positive (-, +, -).

Sector 4: Current in phase A is negative, while in phases B and C they are positive (-,+,+).

Sector 5: Currents in phases A and B are negative, while in phase C it is positive (-, -, +).

Sector 6: Currents in phases A and C are positive, while in phase B it is negative (+, -, +).

Combining the six sectors with the eight switching states produces 48 different modes of operation. However, the modes of operation are reduced to 25 since some of them are repeated in two different sectors. The operation of this topology can be explained as follows: When the active switch Sa in phase A is OFF, the phase current travels through one of the two diodes D1 or D2, depending on its polarity, and charges the two output capacitive filters. In other words, the input current of the rectifier has three paths to travel through, depending on the current direction and the active switches status. The first path is through the upper diode D1, D3 and D5, which is possible only when the phase current is positive. The phase current travels on the second path between the rectifier's inputs to the capacitor midpoint through the active switches, which is possible for both positive and negative input phase currents. The third path is possible when the input phase current is negative, where the current travels from the bottom capacitor C2 towards the input inductor through the lower diode D2, D4 and D6. Both capacitors, C1 and C2, work as two different boost circuits where the upper capacitor boosts the positive voltage while the lower capacitor boosts the negative voltage. On the other hand, the boost inductors are charged when the rectifier input is connected to the capacitor mid-point through one of the bidirectional active switches.

As mentioned earlier, there are three possible paths for the current to travel through in each phase. However, in considering the current directions in each sector, it is evident that only two paths are possible now. For instance, the current in Sector 1 can go through the upper diode (D1) or through the active switch towards the capacitor mid-point, but it cannot pass through the bottom diode (D2). The three controllable switches decide which path the currents will take. As the Vienna rectifier has three controllable switches, eight possible switching states can be applied. The switching states and their effect on the current directions are explained in detail in this chapter. Table 3.1 shows the eight switching states.

Table 3.1: Relation between the switching states and the switches

Switching State	Switch A	Switch B	Switch C
0 0 0	OFF	OFF	OFF
1 0 0	ON	OFF	OFF
0 0 1	OFF	OFF	ON
1 0 1	ON	OFF	ON
0 1 0	OFF	ON	OFF
1 1 0	ON	ON	OFF
0 1 1	OFF	ON	ON
1 1 1	ON	ON	ON

Figures 3.8 to 3.15 show the current paths when the eight switching states are applied to Sector 1 and illustrate that the current passes through the switch whenever the switch is ON. Otherwise, it travels through the upper or lower diodes, depending on the current direction of each phase. It is also observed that the lower diode in phase A and the upper diodes in phases B and C do not function in Sector 1 because phase A is positive while phases B and C are negative.

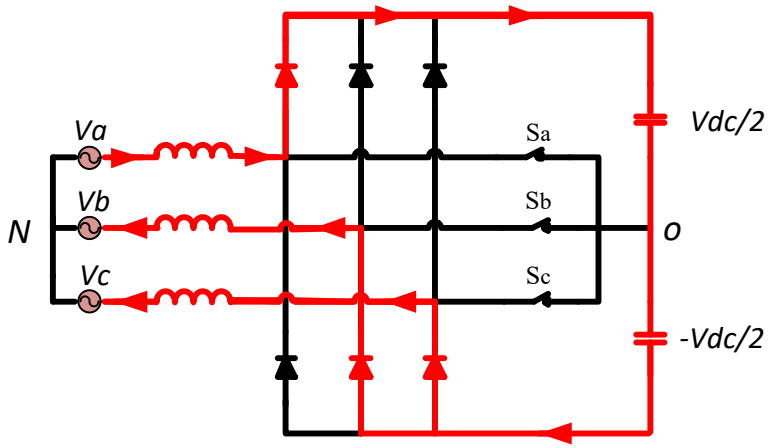

Figure 3.8: Current flow in Vienna rectifier at “000” state for Sector 1

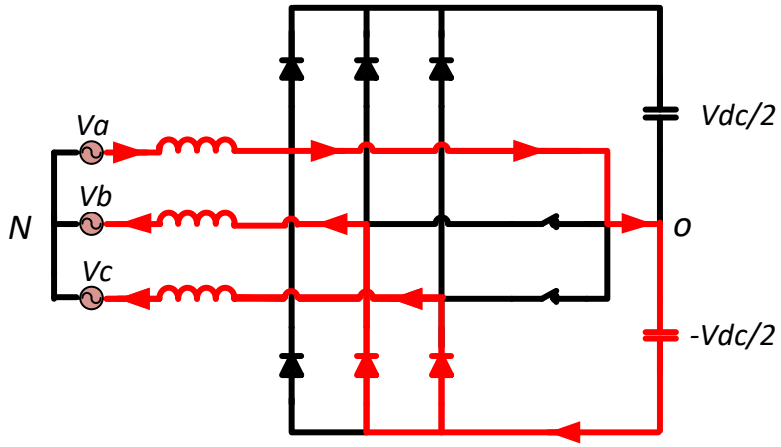

Figure 3.9: Current flow in Vienna rectifier at “100” State for Sector 1

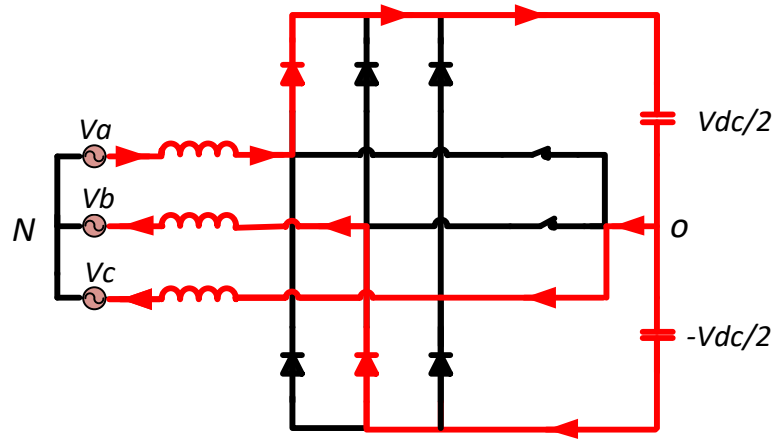

Figure 3.10: Current flow in Vienna rectifier at “001” state for Sector 1

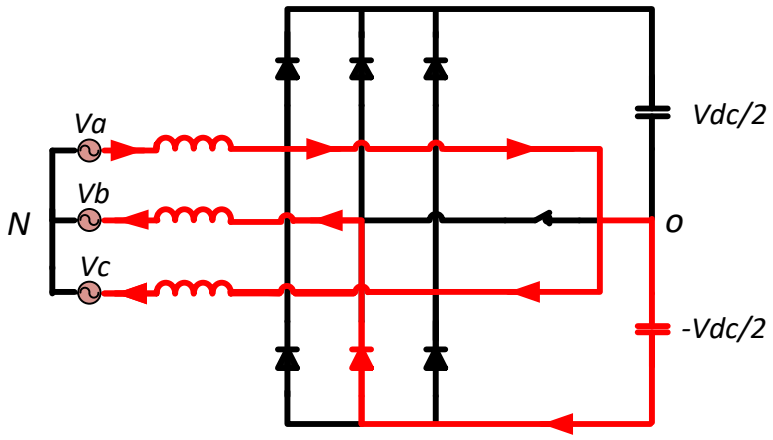

Figure 3.11: Current flow in Vienna rectifier at “101” state for Sector 1

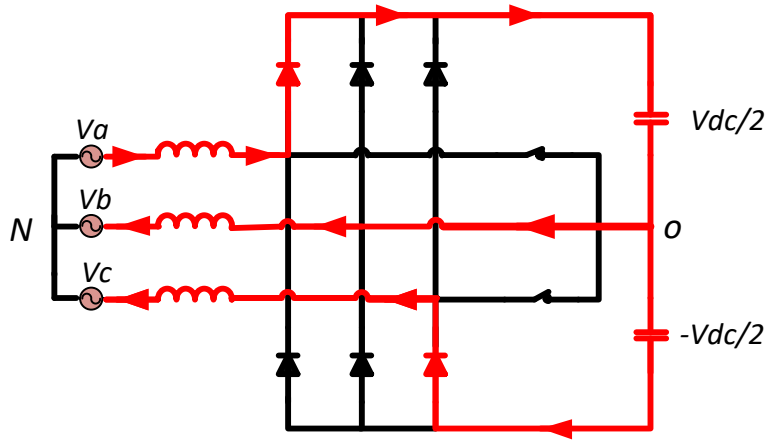

Figure 3.12: Current flow in Vienna rectifier at “010” state for Sector 1

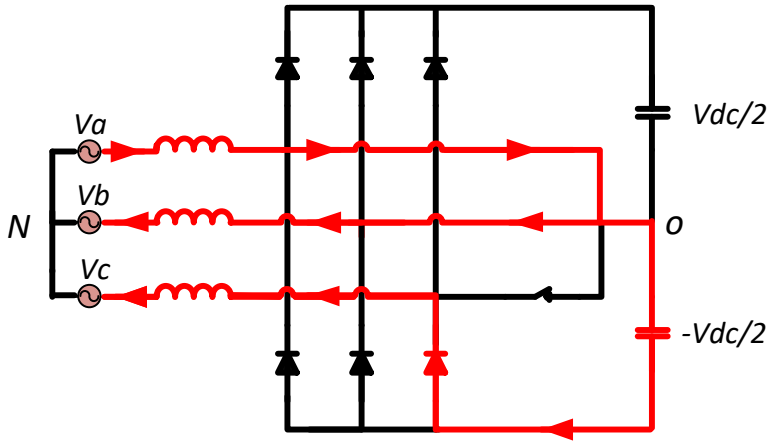

Figure 3.13: Current flow in Vienna rectifier at “110” state for Sector 1

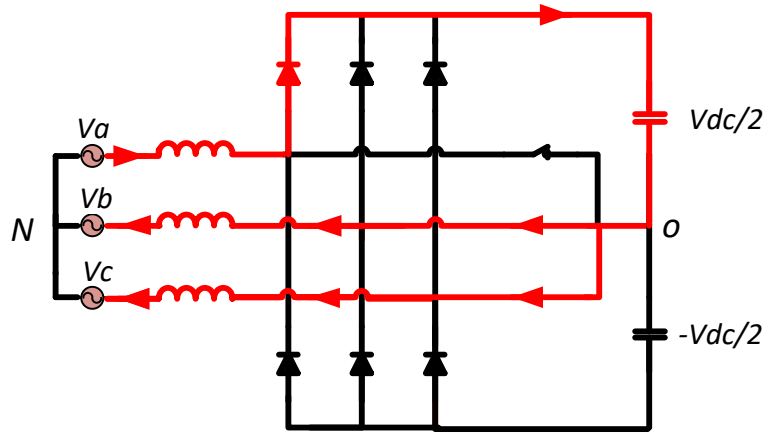

Figure 3.14: Current flow in Vienna rectifier at “011” state for Sector 1

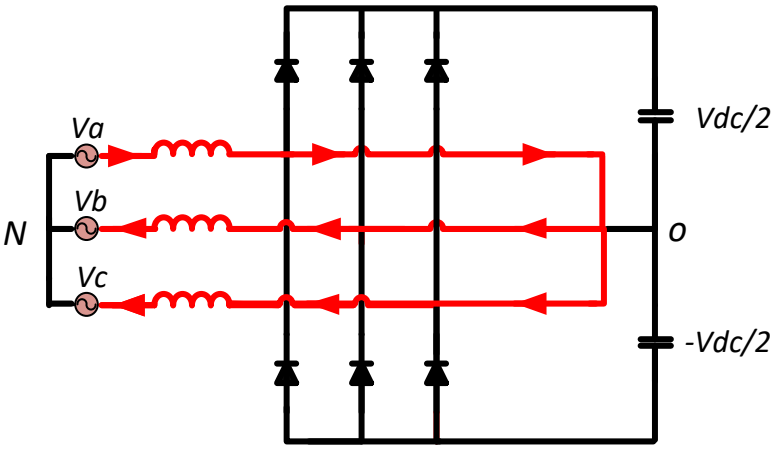

Figure 3.15: Current flow in Vienna rectifier at “111” state for Sector 1

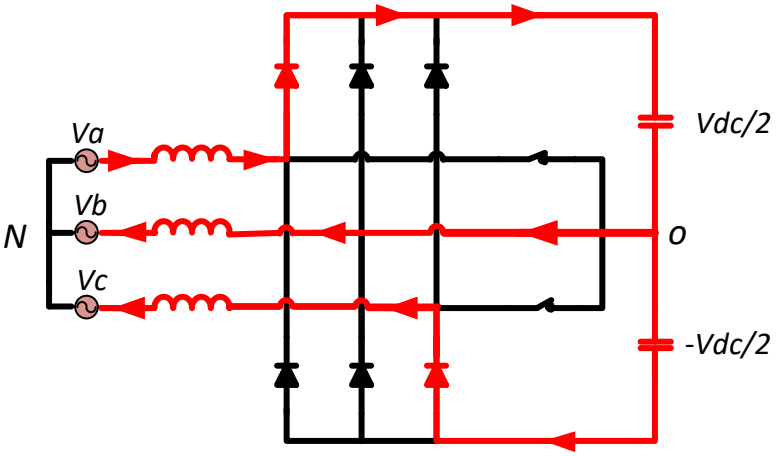

Figure 3.16: Current flow when the switching state is (010) and the phase polarity is (+ - -)

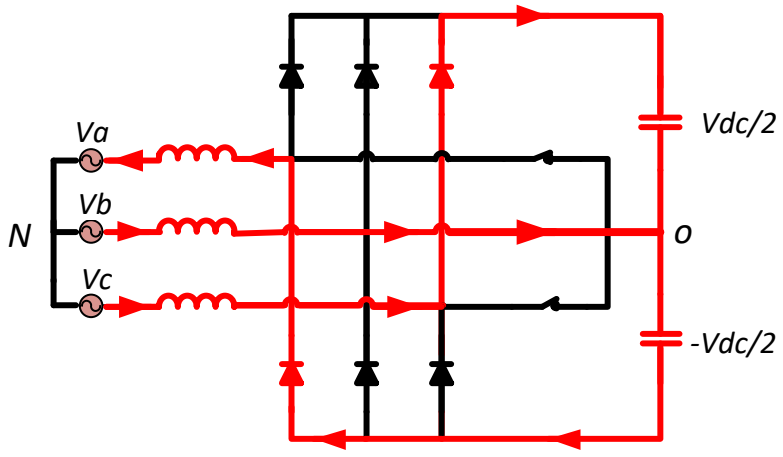

Figure 3.17: Current flow when the switching stat is (010) and the phase polarity is (- + +)

Figures 3.16 and 3.17 depict the effect when the same switching state is applied in two different sectors. Although the switching state or the switches' position for both circuits are identical, the conducting diodes are different due to the difference in the phase currents' direction. In other words, in both circuits, the switching state (010) is applied in sector (+ - -) and (- + +). The switching state (010) means the switches Sa and Sc are OFF while the switch Sb is ON. The figure illustrates how one switching state can result in different circuits and produce different voltage levels.

For several switching states, different current (io) is injected to the capacitor midpoint. The presence of io causes voltage unbalance between the two capacitors C1 and C2. It is therefore imperative that this current needs to be further analyzed. Table 3.2 shows the current io for each switching state in sector 1.

Table 3.2: Current flowing to the mid-point (i0) for each switching state

Switching State	Current in Capacitor midpoint (io)
0 0 0	0
1 0 0	ia
0 0 1	ic
1 0 1	-ib
0 1 0	ib
1 1 0	-ic
0 1 1	-ia
1 1 1	0

As mentioned earlier, the Vienna rectifier is a 3-level rectifier, which means three levels of voltage can be applied to points a, b and c with respect to point (o). Table 3.3 shows the voltage levels that correspond to each switching state in Sector 1.

Table 3.3: Voltage levels produced in each switching state for Sector 1

Sector	Sa	Sb	Sc	Vao	Vbo	Vco
Sector 1	0	0	0	$+\frac{Vdc}{2}$	$-\frac{Vdc}{2}$	$-\frac{Vdc}{2}$
	1	0	0	0	$-\frac{Vdc}{2}$	$-\frac{Vdc}{2}$
	0	0	1	$+\frac{Vdc}{2}$	$-\frac{Vdc}{2}$	0
	1	0	1	0	$-\frac{Vdc}{2}$	0
	0	1	0	$+\frac{Vdc}{2}$	0	$-\frac{Vdc}{2}$
	1	1	0	0	0	$-\frac{Vdc}{2}$
	0	1	1	$+\frac{Vdc}{2}$	0	0
	1	**1**	**1**	**0**	**0**	**0**

In conclusion, the topology and various modes of operation of the Vienna rectifier are studied and explained in this chapter. In addition, the effect of switching states on the operation and the produced voltage levels is illustrated. The impact of the mid-point current is also provided in this chapter. Since Vienna rectifier's operation differs from other converters, it has special requirement for its control; therefore, SVPWM must consider this unique structure of Vienna rectifier which is illustrated in Chapter 5. Before explaining the simplified 3-level SVPWM for the Vienna rectifier, a simple 2-level SVPWM is discussed first in Chapter 4.

Chapter 4. SVPWM for 2-level Converters

This chapter illustrates the basics of the simplest 2-level space vector modulation technique. It also explains the Clarke and Park transformations which are essential in understanding the space vector modulation method. Finally, the switching states that produce the space vectors and the Dwell time calculation are discussed.

4.1. Introduction to Space Vector

SVPWM is a real-time modulation technique that can be applied to any balanced 3-phase system and it is widely used for digital control of voltage source converters. The main idea of the space vector method is transforming the three phase quantities into a 2-dimensional complex plane. Depending on the converter's level, specific numbers of space vector voltages can be applied to the converter. In each switching period, three of these vectors are applied to approximate the reference vector ($\overrightarrow{V_{ref}}$). The time duration for the three vectors must be determined. In order to transform the 3-phase quantities onto a 2-dimentional plane, the Park and Clarke transformations are used, as explained in this chapter.

4.1.1. Definition:

The three phase voltages can be added as a sum of vectors as shown in Figure 4.1:

$$\overrightarrow{V_{abc}} = \overrightarrow{V_a} + \overrightarrow{V_b} + \overrightarrow{V_c} = |V_a|e^{j0} + |V_b|e^{j\frac{2}{3}\pi} + |V_c|e^{-j\frac{2}{3}\pi} \quad (5)$$

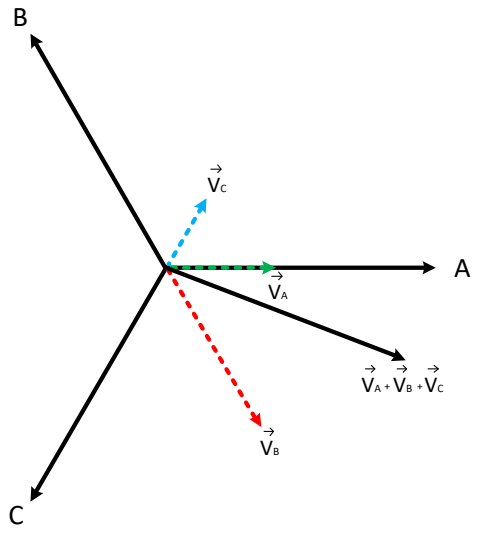

Figure 4.1: Addition of the three vectors

Euler's formula states: $e^{j\alpha} = \cos(\alpha) + j\ \sin(\alpha)$; hence, using Euler's formula in equation (5) results in the following equation:

$$\overrightarrow{V_{abc}} = |V_a| - \frac{1}{2}|V_b| - \frac{1}{2}|V_c| + \mathrm{j}\frac{\sqrt{3}}{2}|V_b| - \mathrm{j}\frac{\sqrt{3}}{2}|V_c| \tag{6}$$

In order to keep the magnitude of the vectors constant during transformation, a coefficient $\frac{2}{3}$ is multiplied to the vector $\overrightarrow{V_{abc}}$:

$$\overrightarrow{V_{ref}} = \frac{2}{3}\ \overrightarrow{V_{abc}} = \frac{2}{3}\left[\ |V_a| - \frac{1}{2}|V_b| - \frac{1}{2}|V_c| + \mathrm{j}\frac{\sqrt{3}}{2}|V_b| - \mathrm{j}\frac{\sqrt{3}}{2}|V_c|\right] \tag{7}$$

$$\overrightarrow{V_{ref}} = \frac{2}{3}\left[|V_a|e^{j0} + |V_b|e^{j\frac{2}{3}\pi} + |V_c|e^{-j\frac{2}{3}\pi}\right] = |V_{ref}|e^{j\theta} \tag{8}$$

In equation (8), θ is the angle and V_{ref} is the magnitude of the reference voltage vector. Equations (5) to (8) above describe the transformation from 3-phase into a 2-dimensional

complex plane. However, more mathematical analysis is required to complete the transformation.

4.1.2. Clarke Transformation

Clarke's transformation is a mathematical transformation used to simplify the 3-phase system. It is a significant method in the space vector modulation technique which generates the reference signal. According to Euler's formula and based on equation (8):

$$\overrightarrow{V_{ref}} = |V_{ref}| \, [\cos(\theta) + j \, \sin(\theta)] \tag{9}$$

In equation (9), the magnitude V_{ref} is multiplied by real and imaginary values which can be separated as follows:

$$V\alpha = Re \, \{ \overrightarrow{V_{ref}} \} = \frac{2}{3} \left[\, |V_a| - \frac{1}{2} |V_b| - \frac{1}{2} |V_c| \right] \tag{10}$$

$$V\beta = Im \, \{ \overrightarrow{V_{ref}} \} = \frac{2}{3} \left[j \frac{\sqrt{3}}{2} |V_b| - j \frac{\sqrt{3}}{2} |V_c| \right] \tag{11}$$

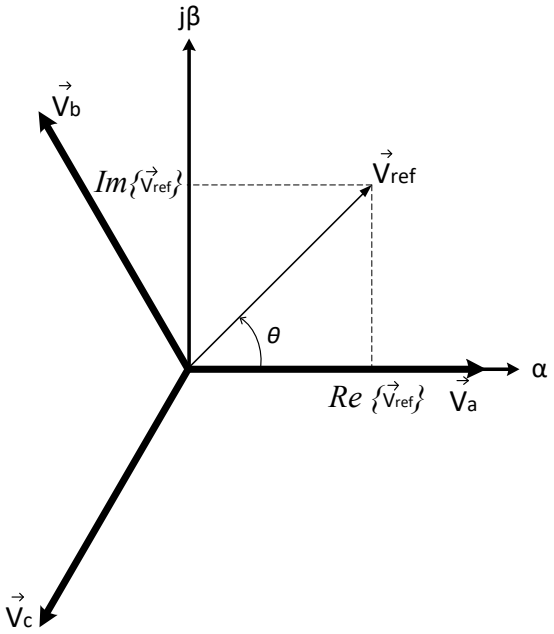

Figure 4.2: Space vector in $\alpha\beta$-domain

As illustrated in Figure 4.2, the 3-phase system is transformed into a 2-phase system. This transformation produces a new coordinate system that is called a stator coordinate system because its coordinates are fixed; where the α-axis corresponds to vector $\overrightarrow{V_a}$ and the β-axis is perpendicular to the α-axis.

Equation (12) provides a mathematical explanation of the transformation of a 3-phase system into a 2-phase system, while equation (13) shows the conversion from a 2-phase to a 3-phase system.

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \frac{2}{3} & 0 \\ \frac{-1}{3} & \frac{1}{\sqrt{3}} \\ \frac{-1}{3} & \frac{-1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} \tag{13}$$

4.1.3. Park's Transformation:

Park's transformation is used to simplify complex mathematical models. It uses the stationary coordinate (Clarke's transformation) to produce a rotating coordinate system which is simpler and more useful for controlling purposes. In addition, Park's transformation allows the d-axis to rotate around a fixed coordinate system. The d-axis is shifted from the fixed axis alpha by an angle known as ∅, while the q-axis is perpendicular to the d-axis. Figure 4.3 illustrates Park's transformation graphically.

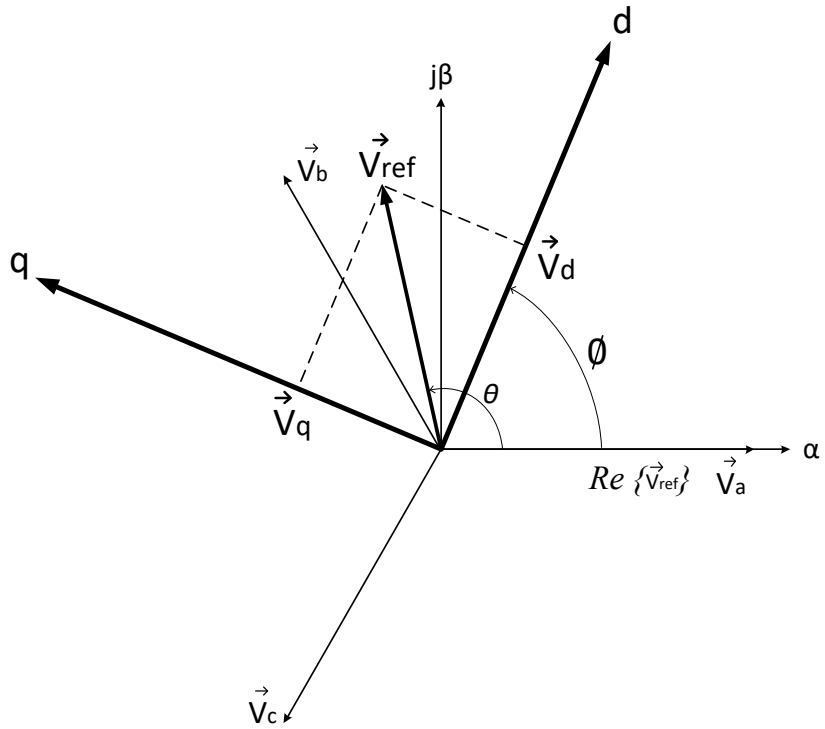

Figure 4.3: Vectors in dq-coordinate.

As shown in equation (13), d and q components can be found from the space vector definition:

$$\overrightarrow{V_{ref,dq}} = \frac{2}{3}\left[|V_a| + |V_b|e^{j\frac{2}{3}\pi} + |V_c|e^{-j\frac{2}{3}\pi}\right] e^{-j(\emptyset)} \tag{14}$$

Using Euler's formula, the following equations are found.

$$V_d = Re\ \{\overrightarrow{V_{ref,dq}}\} = |V_a|\cos(\emptyset) + |V_b|\sin(\emptyset) \tag{15}$$

$$V_q = Im\ \{\overrightarrow{V_{ref,dq}}\} = -|V_a|\sin(\emptyset) + |V_b|\cos(\emptyset) \tag{16}$$

The matrix in equation (17) shows the transformation from a 3-phase system into a d-q system, which is known as Park's transformation.

$$\begin{bmatrix} d \\ q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\emptyset) & \cos(\emptyset - \frac{2\pi}{3}) & \cos(\emptyset + \frac{2\pi}{3}) \\ \sin(\emptyset) & \sin(\emptyset - \frac{2\pi}{3}) & \sin(\emptyset + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} \mathrm{V_a} \\ \mathrm{V_b} \\ \mathrm{V_c} \end{bmatrix} \quad (17)$$

4.2. Space Vector for 2-level-Converters:

4.2.1. Switching States:

The conventional 2-level converter has six active switches, as shown in Figure 4.4. Each phase has two controllable switches. One switch connects the phase to the positive side of the capacitor ($+V_{dc}$), while the other switch connects the phase to the negative side of the capacitor or to the ground (0 V). Only two voltage levels can be applied to the rectifier's input, which is why it is known as a 2-level converter. The position of each switch can be represented by two bits 0 and 1. The bit number "1" means the upper switch is turned ON while the lower switch is OFF. However, the bit number "0" means the upper switch is OFF while the lower switch is turned ON. Since there are only six switches, and the two switches in each phase cannot be both ON simultaneously, three bits are enough to represent the positions of all the switches.

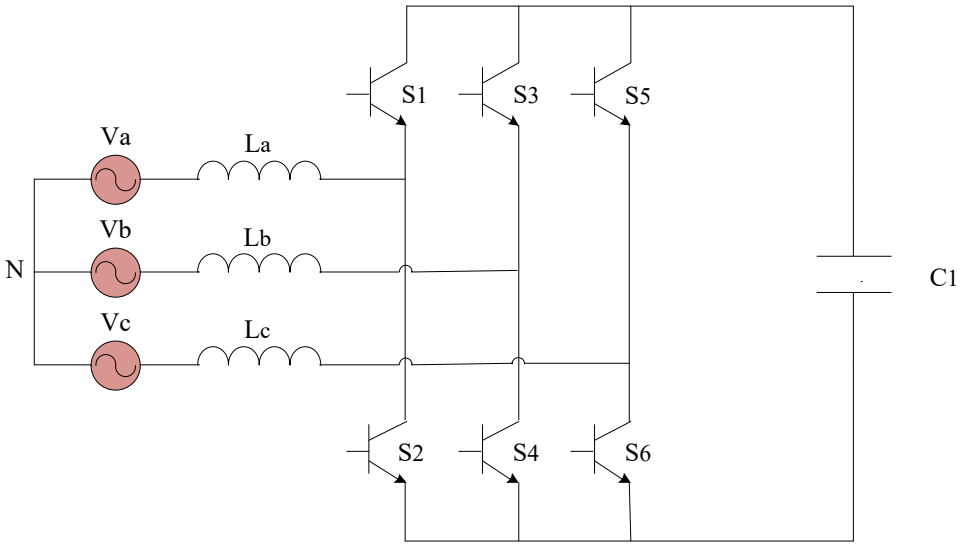

Figure 4.4: Conventional 3-phase, 2-level full controlled rectifier

As shown in Table 4.1, eight different switching states can be applied to the converter. The two switching states “000” and “111” are called the zero states while the rest are called active states.

Table 4.1: Relation between switching states and the switches in the conventional 3-phase rectifier

Switching State	Phase A		Phase B		Phase C	
	Upper Switch	Lower Switch	Upper Switch	Lower Switch	Upper Switch	Lower Switch
0 0 0	OFF	ON	OFF	ON	OFF	ON
1 0 0	ON	OFF	OFF	ON	OFF	ON
0 0 1	OFF	ON	OFF	ON	ON	OFF
1 0 1	ON	OFF	OFF	ON	ON	OFF
0 1 0	OFF	ON	ON	OFF	OFF	ON
1 1 0	ON	OFF	ON	OFF	OFF	ON
0 1 1	OFF	ON	ON	OFF	ON	OFF
1 1 1	ON	OFF	ON	OFF	ON	OFF

4.2.2. Space Vectors:

The switching states explained earlier can be represented as space vectors. Both Table 4.2 and Figure 4.5 explain the relationship between the switching states and the voltage space vector. Applying the switching states to the converter produces two zero vectors and six active vectors. The hexagon in Figure 4.5 shows the switching states as vectors where the zero vectors are located at the center of the hexogen while the active vectors are located at the edges of the hexogen. The active vectors divide the hexogen into six sectors, with each sector consisting of an equilateral triangle (all the angles are equal to 60 degrees).

Table 4.2: Vectors produced by different switching states in 2-Level converters

Space Vector	Switching State	Vector Definition
$\overrightarrow{V0}$	0 0 0	0
	1 1 1	
$\overrightarrow{V1}$	1 0 0	$\frac{2}{3}V_d e^{j0}$
$\overrightarrow{V2}$	1 1 0	$\frac{2}{3}V_d e^{j\frac{\pi}{3}}$
$\overrightarrow{V3}$	0 1 0	$\frac{2}{3}V_d e^{j\frac{2\pi}{3}}$
$\overrightarrow{V4}$	0 1 1	$\frac{2}{3}V_d e^{j\frac{3\pi}{3}}$
$\overrightarrow{V5}$	0 0 1	$\frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
$\overrightarrow{V6}$	1 0 1	$\frac{2}{3}V_d e^{j\frac{5\pi}{3}}$

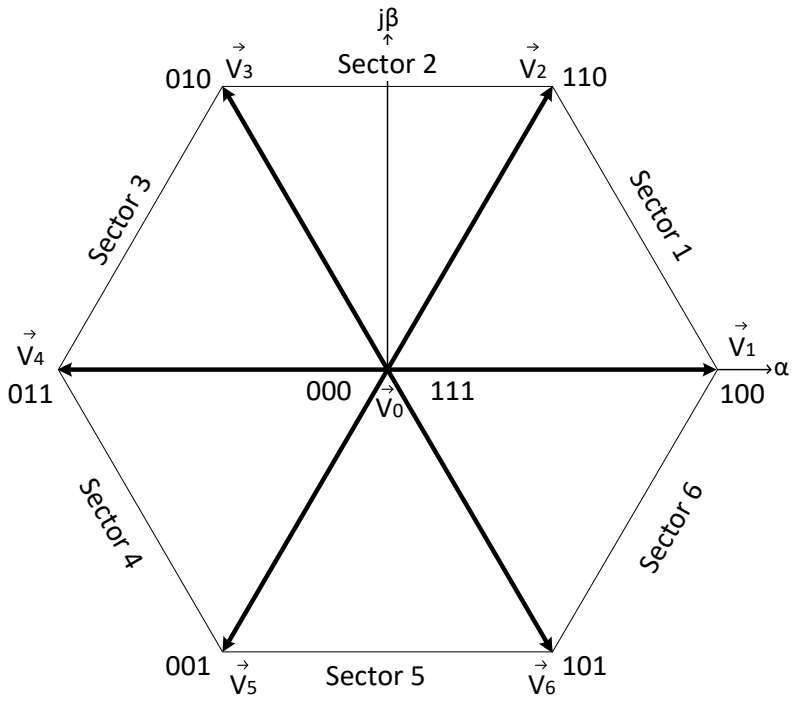

Figure 4.5: Space vector diagram for 2-level converters

4.2.3. Dwell Time Calculation:

The reference vector rotates around the hexogen. In each switching period, three vectors are used for a specific period of time (Dwell time) to approximate the reference vector. The Dwell time calculation is explained in this section.

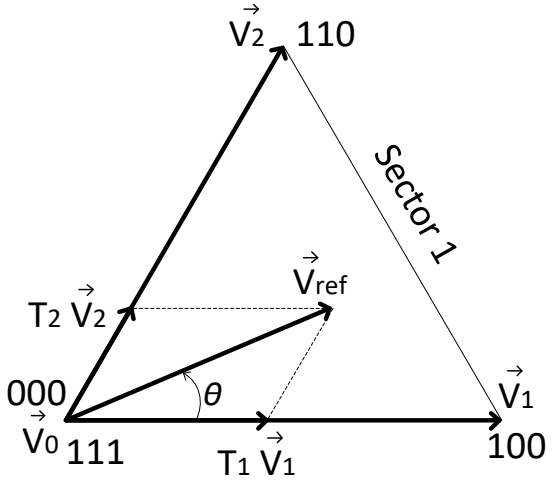

Figure 4.6: Approximating the reference space vector voltage using two active vectors and two zero vectors

Figure 4.6 depicts an example of a reference vector ($\overrightarrow{V_{ref}}$) that falls in sector 1 of the hexogen. The reference vector ($\overrightarrow{V_{ref}}$) can be approximated using the three adjacent vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$. Using the definition of volt-second balance, equation (18) and (19) can be derived:

$$T_s \overrightarrow{V_{ref}} = T_1 \overrightarrow{V_1} + T_2 \overrightarrow{V_2} + T_0 \overrightarrow{V_0} \quad (18)$$

$$T_s = T_1 + T_2 + T_0 \quad (19)$$

Where T_1 , T_2 and T_0 are found using basic trigonometric relations, as shown in equations (20) to (22):

$$T_1 = \frac{\sqrt{3}}{V_{dc}} T_s \, |V_{ref}| \sin(60 - \theta) \quad (20)$$

$$T_2 = \frac{\sqrt{3}}{V_{dc}} T_s |V_{ref}| \sin(\theta) \quad (21)$$

$$T_0 = T_s - (T_2 + T_1) \quad (22)$$

T_1 and T_2 are the Dwell time for the vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ respectively. Since these two vectors are stationary and cannot be changed, time division between $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ is used to obtain an approximated vector that is almost equal to the reference vector. In Figure 4.6, the reference vector does not touch the boundary of the hexogen. As a result, the sum of T_1 and T_2 is less than the switching time T_s, which means $\overrightarrow{V_0}$ must be applied for the remaining time of the switching period (T_0). Table 4.3 explains the relationship between the reference vector's angle and the Dwell time.

Table 4.3: Relation between the reference vector's angle and dwell time

Reference Angle (θ^o)	0^o	$0^o < \theta < 30^o$	30^o	$30^o < \theta < 60^o$	60^o
Dwell Time (s)	*T1 > 0* *T2 = 0*	*T1 > T2> 0*	*T1 = T2*	*T2 > T1> 0*	*T1 = 0* *T2 > 0*

After finding the Dwell time for each vector, the results will be combined and applied to the controllable switches. This process is repeated in each sampling time. Figure 3.7 illustrates how vectors can be combined using the calculated Dwell time.

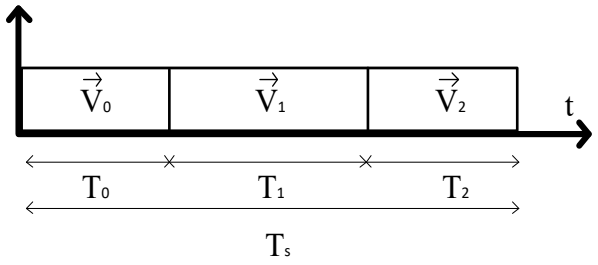

Figure 4.7: Applying each vector for its dwell time

In conclusion, this chapter discusses the basic idea of the 2-level SVPWM. In addition, Clarke and Park transformations are explained in this chapter and space vectors for 2-level converters are derived. Finally, the procedure of synthesizing the reference vector by the adjacent vectors is illustrated. The next chapter illustrates the 3-level SVPWM for the Vienna rectifier.

Chapter 5. Modulation and Control of The Vienna Rectifier Using Simplified 3-level SVPWM

In this chapter, a detailed space vector analysis of the Vienna rectifier is provided. All possible space vectors for the Vienna rectifier are derived. Also, a step-by-step explanation of the simplified SVPWM, which reduces the THD and the computational effort, is illustrated in this chapter. Finally, the controller of the Vienna rectifier is explained.

5.1. Space Vector Analysis for Vienna rectifier:

Unlike conventional Pulse Width Modulation (PWM) techniques, SVPWM is a modulation technique that provides the ability to control the pulse placement and provides the capability to reduce the THD. The SVPWM for the Vienna rectifier differs from the conventional 3-level SVPWM method due to various reasons. The main reason is that the degree of freedom in the Vienna rectifier is different from the conventional converter. The conventional SV method considers the voltage vector as the primary vector, which is used to locate the nearest space vectors for the purpose of synthesizing the reference vector. Using the conventional SVPWM for the Vienna rectifier leads to a wrong selection of the nearest space vectors since the polarity of the phase currents choose which voltage level is to be applied. In other words, when applying the conventional space vector method, not all voltage space vectors are visible at a given time because of the direction of the phase current, which limits the applicable voltage vectors. Therefore, the SVPWM for the Vienna rectifier uses the current vector as the primary vector.

5.1.1. Switching States

As the Vienna rectifier consists of three controllable switches and produces three voltage levels, its space vector analysis differs from the 2-level rectifiers. Based on the basic

operations of the Vienna rectifier, $+\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$ are three applicable voltages to the input of the rectifier system. A 3-level space vector has six sectors, with each sector containing eight switching states. However, as several switching states are repeated in multiple sectors, there are only 25 unique applicable switching states. These 25 switching states will be derived mathematically in the next section.

The six sectors can be identified based on the polarity of the 3-phase voltage, as shown in Table 5.1. They can also be identified by the angle of the space vector voltage, as shown in Table 5.2.

Table 5.1: Identification of the sectors based on the polarity of phases

Sectors	Phase A	Phase B	Phase C
Sector 1	Positive	Negative	Negative
Sector 2	Positive	Positive	Negative
Sector 3	Negative	Positive	Negative
Sector 4	Negative	Positive	Positive
Sector 5	Negative	Negative	Positive
Sector 6	Positive	Negative	Positive

Table 5.2: Identification of the sectors based on the angle of the space vector

Sectors	Angle (θ^o)	Sectors	Angle (θ^o)
Sector 1	$-30 \leq \theta < 30$	**Sector 4**	$150 \leq \theta < -150$
Sector 2	$30 \leq \theta < 90$	**Sector 5**	$-150 \leq \theta < -90$
Sector 3	$90 \leq \theta < 150$	**Sector 6**	$-90 \leq \theta < -30$

The switching states can also be represented by three different numbers, namely +1, 0 and -1. The number +1 means the active switch is OFF and signifies that the phase current flows through the upper diode of the rectifier system, thus producing $+\frac{V_{dc}}{2}$ volt at the

rectifier's input. Alternatively, the number -1 means the active switch is OFF and the phase current travels through the lower diode of the rectifier system and the applied voltage to the rectifier's input is $-\frac{V_{dc}}{2}$ volt. Finally, the number 0 means that the active switch conducts and 0 volt is applied to the input of the rectifier system.

As shown in equation (23), the switching function is defined by knowing the Switching Status (SS) 1 or 0 and the sign of the phase current + or -.

$$S_i = \text{sign}(i_i)\ [1 - SS_i] \tag{23}$$

Where i indicates the phase a, b or c.

Table 5.3 depicts the results of equation (23) for all eight switching states in the six sectors:

Table 5.3: Results of switching function in each sector

Sectors	000	100	001	101	010	110	011	111
Sector 1	+1, -1, -1	0, -1, -1	+1, -1, 0	0, -1, 0	+1, 0, -1	0, 0, -1	+1, 0, 0	000
Sector 2	+1, +1, -1	0, +1, -1	+1, +1, 0	0, +1, 0	+1, 0, -1	0, 0, -1	+1, 0, 0	000
Sector 3	-1, +1, -1	0, +1, -1	-1, +1, 0	0, +1, 0	-1, 0, -1	0, 0, -1	-1, 0, 0	000
Sector 4	-1, +1, +1	0, +1, +1	-1, +1, 0	0, +1, 0	-1, 0, +1	0, 0, +1	-1, 0, 0	000
Sector 5	-1, -1, +1	0, -1, +1	-1, -1, 0	0, -1, 0	-1, 0, +1	0, 0, +1	-1, 0, 0	000
Sector 6	-1, -1, +1	0, -1, +1	-1, -1, 0	0, -1, 0	-1, 0, +1	0, 0, +1	-1, 0, 0	000

5.1.2. Space Vectors for the Vienna Rectifier:

Based on the previous section, 25 switching states are sufficient to find the Vienna rectifier's voltage space vectors. To drive the equations for the voltage space vectors, several assumptions must be made, which includes assuming a balanced input voltage, equal capacitor

voltages ($V_{c1} = V_{c2} = \frac{V_{dc}}{2}$) and phase currents in phase with the phase voltages. Accordingly, equation (24) is used to calculate the voltage at the input of the rectifier system with respect to the capacitor mid-point (o):

$$V_{io} = \frac{V_{dc}}{2} S_i \tag{24}$$

Where i indicates the phase a, b or c.

The voltage between the neutral point (N) and the capacitor midpoint (o) can be calculated in equation (25):

$$V_{No} = \frac{V_{dc}}{6} (S_a + S_b + S_c) \tag{25}$$

Since the voltages V_{io} and V_{No} are determined, it is possible to find the voltage at the input of the rectifier system with respect to the Neutral point (N) as shown in equation (26):

$$V_{iN} = V_{io} - V_{No} \tag{26}$$

Therefore, the voltage space vectors of the Vienna rectifier are determined using equation (27):

$$\overrightarrow{V_{ref}} = \frac{2}{3} [V_{aN} e^{j0} + V_{bN} e^{j\frac{2}{3}\pi} + V_{cN} e^{-j\frac{2}{3}\pi}] = \frac{2}{3} [V_{ao} e^{j0} + V_{bo} e^{j\frac{2}{3}\pi} + V_{co} e^{-j\frac{2}{3}\pi}] = \frac{V_{dc}}{3} [S_a e^{j0} + S_b e^{j\frac{2}{3}\pi} + S_c e^{-j\frac{2}{3}\pi}] \tag{27}$$

Table 5.4 illustrates the voltage analysis of the Vienna rectifier using equations (24) to (26). It also illustrates the change in the voltage as the switching state and the sector are

changing. This analysis is sufficient to understand the behavior of the system and to find the rectifier's voltage space vector.

Table 5.4: Voltage analysis in the Vienna rectifier

Sectors	Switching State	V_{ao}	V_{bo}	V_{co}	V_{No}	V_{aN}	V_{bN}	V_{cN}
1	0 0 0	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{2}{3}Vdc$	$\frac{-1}{3}Vdc$	$\frac{-1}{3}Vdc$
	0 0 1	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0	0	$\frac{1}{2}Vdc$	$\frac{-1}{2}Vdc$	0
	0 1 0	$\frac{V_{dc}}{2}$	0	$-\frac{V_{dc}}{2}$	0	$\frac{1}{2}Vdc$	0	$\frac{-1}{2}Vdc$
	0 1 1	$\frac{V_{dc}}{2}$	0	0	$\frac{1}{6}$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$
	1 0 0	0	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{-1}{3}$	$\frac{-1}{3}Vdc$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$
	1 0 1	0	$-\frac{V_{dc}}{2}$	0	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$
	1 1 0	0	0	$-\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$
	1 1 1	0	0	0	0	0	0	0
2	0 0 0	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{1}{3}Vdc$	$\frac{1}{3}Vdc$	$\frac{-2}{3}Vdc$
	0 0 1	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0	$\frac{1}{3}$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$
	0 1 0	$\frac{V_{dc}}{2}$	0	$-\frac{V_{dc}}{2}$	0	$\frac{1}{2}Vdc$	0	$\frac{-1}{2}Vdc$
	0 1 1	$\frac{V_{dc}}{2}$	0	0	$\frac{1}{6}$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$
	1 0 0	0	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0	0	$\frac{1}{2}Vdc$	$\frac{-1}{2}Vdc$
	1 0 1	0	$\frac{V_{dc}}{2}$	0	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$
	1 1 0	0	0	$-\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$

	1 1 1	0	0	0	0	0	0	0
3	0 0 0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{-1}{3}Vdc$	$\frac{2}{3}Vdc$	$\frac{-1}{3}Vdc$
	0 0 1	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0	0	$\frac{-1}{2}Vdc$	$\frac{1}{2}Vdc$	0
	0 1 0	$-\frac{V_{dc}}{2}$	0	$-\frac{V_{dc}}{2}$	$\frac{-1}{3}$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$
	0 1 1	$-\frac{V_{dc}}{2}$	0	0	$\frac{-1}{6}$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$
	1 0 0	0	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0	0	$\frac{1}{2}Vdc$	$\frac{-1}{2}Vdc$
	1 0 1	0	$\frac{V_{dc}}{2}$	0	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$
	1 1 0	0	0	$-\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$
	1 1 1	0	0	0	0	0	0	0
4	0 0 0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{-2}{3}Vdc$	$\frac{1}{3}Vdc$	$\frac{1}{3}Vdc$
	0 0 1	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0	0	$\frac{-1}{2}Vdc$	$\frac{1}{2}Vdc$	0
	0 1 0	$-\frac{V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$	0	$\frac{-1}{2}Vdc$	0	$\frac{1}{2}Vdc$
	0 1 1	$-\frac{V_{dc}}{2}$	0	0	$\frac{-1}{6}$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$
	1 0 0	0	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{1}{3}$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$
	1 0 1	0	$\frac{V_{dc}}{2}$	0	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$
	1 1 0	0	0	$\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$
	1 1 1	0	0	0	0	0	0	0
	0 0 0	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{-1}{6}$	$\frac{-1}{3}Vdc$	$\frac{-1}{3}Vdc$	$\frac{2}{3}Vdc$
	0 0 1	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0	$\frac{-1}{3}$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$

5	0 1 0	$-\frac{V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$	0	$\frac{-1}{2}Vdc$	0	$\frac{1}{2}Vdc$
	0 1 1	$-\frac{V_{dc}}{2}$	0	0	$\frac{-1}{6}$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$	$\frac{1}{6}Vdc$
	1 0 0	0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0	0	$\frac{-1}{2}Vdc$	$\frac{1}{2}Vdc$
	1 0 1	0	$-\frac{V_{dc}}{2}$	0	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$
	1 1 0	0	0	$\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$
	1 1 1	0	0	0	0	0	0	0
6	0 0 0	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{1}{3}Vdc$	$\frac{-2}{3}Vdc$	$\frac{1}{3}Vdc$
	0 0 1	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0	0	$\frac{1}{2}Vdc$	$\frac{-1}{2}Vdc$	0
	0 1 0	$\frac{V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$	$\frac{1}{3}$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$
	0 1 1	$\frac{V_{dc}}{2}$	0	0	$\frac{1}{6}$	$\frac{1}{3}Vdc$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$
	1 0 0	0	$-\frac{V_{dc}}{2}$	Vdc2	0	0	$\frac{-1}{2}Vdc$	$\frac{1}{2}Vdc$
	1 0 1	0	$-\frac{V_{dc}}{2}$	0	$\frac{-1}{6}$	$\frac{1}{6}Vdc$	$\frac{-1}{3}Vdc$	$\frac{1}{6}Vdc$
	1 1 0	0	0	$\frac{V_{dc}}{2}$	$\frac{1}{6}$	$\frac{-1}{6}Vdc$	$\frac{-1}{6}Vdc$	$\frac{1}{3}Vdc$
	1 1 1	0	0	0	0	0	0	0

The magnitude and angle of the voltage space vector is found in Table 5.5 using equation (27). The data provided in Table 5.4 is used to derive the voltage space vectors. Table 5.5 illustrates the effect of the switching states on the rectifier operation, and also depicts the vector's magnitude and angle produced by these switching states.

Table 5.5: Voltage space vectors in each sector

Sectors	Switching State	V_{ref}	θ^o	Vector Name	Sectors	Switching State	V_{ref}	θ^o	Vector Name
1	0 0 0	$\frac{2}{3}V_{dc}$	0	$\overrightarrow{V_2}$	2	0 0 0	$\frac{2}{3}V_{dc}$	60	$\overrightarrow{V_5}$
	0 0 1	$\frac{1}{\sqrt{3}}V_{dc}$	-30	$\overrightarrow{V_{18}}$		0 0 1	$\frac{1}{3}V_{dc}$	60	$\overrightarrow{V_4}$
	0 1 0	$\frac{1}{\sqrt{3}}V_{dc}$	30	$\overrightarrow{V_3}$		0 1 0	$\frac{1}{\sqrt{3}}V_{dc}$	30	$\overrightarrow{V_3}$
	0 1 1	$\frac{1}{3}V_{dc}$	0	$\overrightarrow{V_1}$		0 1 1	$\frac{1}{3}V_{dc}$	0	$\overrightarrow{V_1}$
	1 0 0	$\frac{1}{3}V_{dc}$	0	$\overrightarrow{V_1}$		1 0 0	$\frac{1}{\sqrt{3}}V_{dc}$	90	$\overrightarrow{V_6}$
	1 0 1	$\frac{1}{3}V_{dc}$	-60	$\overrightarrow{V_{16}}$		1 0 1	$\frac{1}{3}V_{dc}$	120	$\overrightarrow{V_7}$
	1 1 0	$\frac{1}{3}V_{dc}$	60	$\overrightarrow{V_4}$		1 1 0	$\frac{1}{3}V_{dc}$	60	$\overrightarrow{V_4}$
	1 1 1	0	0	$\overrightarrow{V_{19}}$		1 1 1	0	0	$\overrightarrow{V_{19}}$
3	0 0 0	$\frac{2}{3}V_{dc}$	120	$\overrightarrow{V_8}$	4	0 0 0	$\frac{2}{3}V_{dc}$	180	$\overrightarrow{V_{11}}$
	0 0 1	$\frac{1}{\sqrt{3}}V_{dc}$	150	$\overrightarrow{V_9}$		0 0 1	$\frac{1}{\sqrt{3}}V_{dc}$	150	$\overrightarrow{V_9}$
	0 1 0	$\frac{1}{3}V_{dc}$	120	$\overrightarrow{V_7}$		0 1 0	$\frac{1}{\sqrt{3}}V_{dc}$	-150	$\overrightarrow{V_{12}}$
	0 1 1	$\frac{1}{3}V_{dc}$	180	$\overrightarrow{V_{10}}$		0 1 1	$\frac{1}{3}V_{dc}$	180	$\overrightarrow{V_{10}}$
	1 0 0	$\frac{1}{\sqrt{3}}V_{dc}$	90	$\overrightarrow{V_6}$		1 0 0	$\frac{1}{3}V_{dc}$	180	$\overrightarrow{V_{10}}$
	1 0 1	$\frac{1}{3}V_{dc}$	120	$\overrightarrow{V_7}$		1 0 1	$\frac{1}{3}V_{dc}$	120	$\overrightarrow{V_7}$
	1 1 0	$\frac{1}{3}V_{dc}$	60	$\overrightarrow{V_4}$		1 1 0	$\frac{1}{3}V_{dc}$	-120	$\overrightarrow{V_{13}}$
	1 1 1	0	0	$\overrightarrow{V_{19}}$		1 1 1	0	0	$\overrightarrow{V_{19}}$

5	0 0 0	$\frac{2}{3}V_{dc}$	-120	$\overrightarrow{V_{14}}$	**6**	0 0 0	$\frac{2}{3}V_{dc}$	-60	$\overrightarrow{V_{17}}$
	0 0 1	$\frac{1}{3}V_{dc}$	-120	$\overrightarrow{V_{13}}$		0 0 1	$\frac{1}{\sqrt{3}}V_{d}$	-30	$\overrightarrow{V_{18}}$
	0 1 0	$\frac{1}{\sqrt{3}}V_{dc}$	-150	$\overrightarrow{V_{12}}$		0 1 0	$\frac{1}{3}V_{dc}$	-60	$\overrightarrow{V_{16}}$
	0 1 1	$\frac{1}{3}V_{dc}$	180	$\overrightarrow{V_{10}}$		0 1 1	$\frac{1}{3}V_{dc}$	0	$\overrightarrow{V_{1}}$
	1 0 0	$\frac{1}{\sqrt{3}}V_{dc}$	-90	$\overrightarrow{V_{15}}$		1 0 0	$\frac{1}{\sqrt{3}}V_{d}$	-90	$\overrightarrow{V_{15}}$
	1 0 1	$\frac{1}{3}V_{dc}$	-60	$\overrightarrow{V_{16}}$		1 0 1	$\frac{1}{3}V_{dc}$	-60	$\overrightarrow{V_{16}}$
	1 1 0	$\frac{1}{3}V_{dc}$	-120	$\overrightarrow{V_{13}}$		1 1 0	$\frac{1}{3}V_{dc}$	-120	$\overrightarrow{V_{13}}$
	1 1 1	0	0	$\overrightarrow{V_{19}}$		1 1 1	0	0	$\overrightarrow{V_{19}}$

As shown in Table 5.5, there are four different vector lengths and a total of 19 vectors. 6 of these vectors are called long vectors ($\frac{2}{3}V_{dc}$) , another 6 are known as medium vectors ($\frac{1}{\sqrt{3}}V_{dc}$), and 6 are named short vectors ($\frac{1}{3}V_{dc}$) . The last vector is the zero vector which is located at the center of the hexagon. All of the information presented in Table 5.5 is illustrated graphically as shown in Figure 5.1. This figure shows six different hexagons located inside of the big hexagon. Each one of these hexagons represent a sector. The center of each sector has two switching states (short vectors) which are called the redundant switching states.

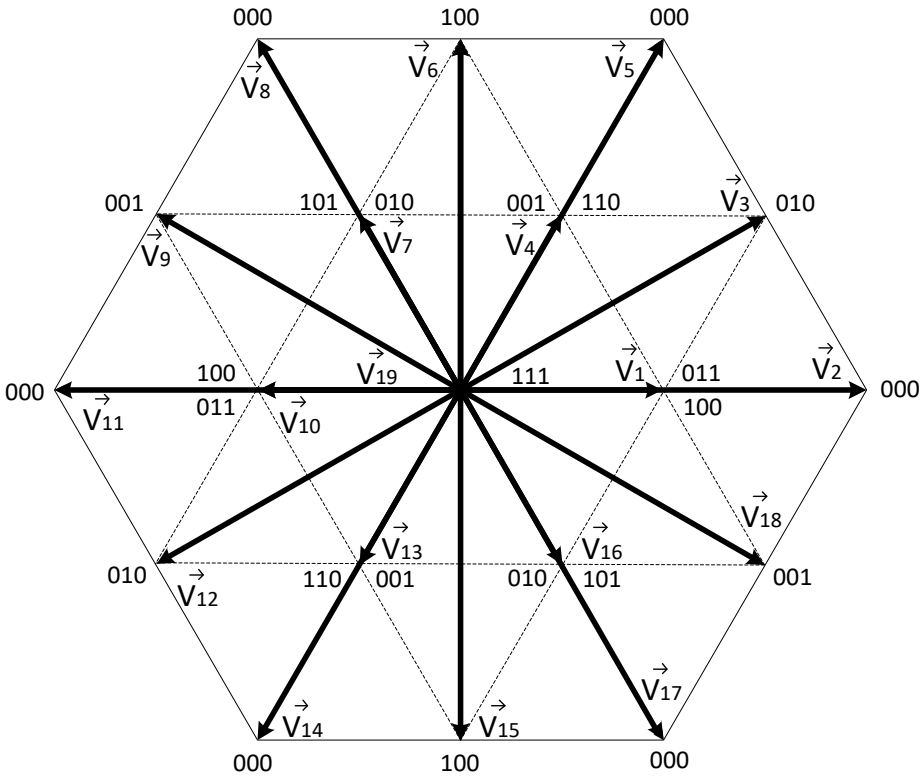

Figure 5.1: Space vector diagram for 3-level converters

5.2. Space Vector Modulation for Vienna Rectifier:

The controller of the Vienna rectifier generates the required voltage reference in the dq-coordinate which is transferred into the Alpha-Beta coordinate system in the space vector modulation technique. As a further step, the magnitude $|(Vref)|$ and the angle (θ) of the reference vector must be extracted to further continue with the SVPWM technique. The novel simplified SVPWM is discussed in detail in this section.

5.2.1. Sector Identification

A significant step in SVPWM is to identify which sector the voltage and current vectors lay in. This can be done by using simple comparators to determine the polarity of the phases. Figure 5.2 depicts the procedure of sector identification. As explained earlier, since it is a 3-

phase system and the phases cannot have the same polarity at the same time, there are six different sectors.

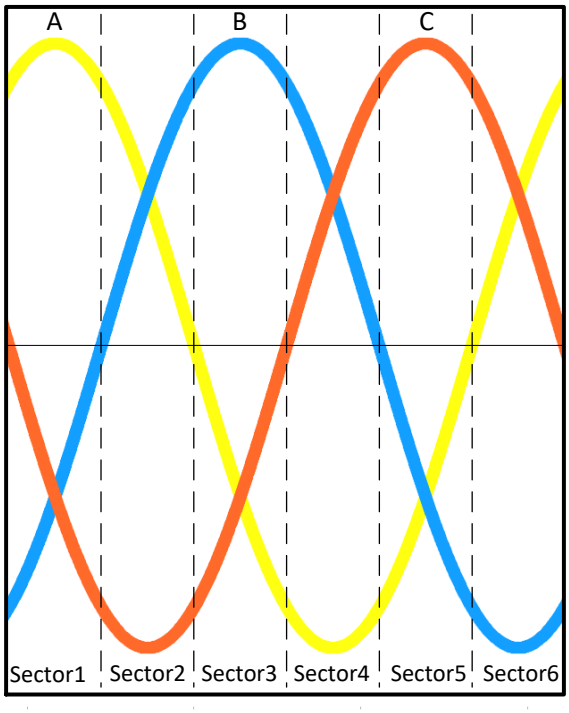

Figure 5.2: Location of the six sectors in the 3-phase waveform

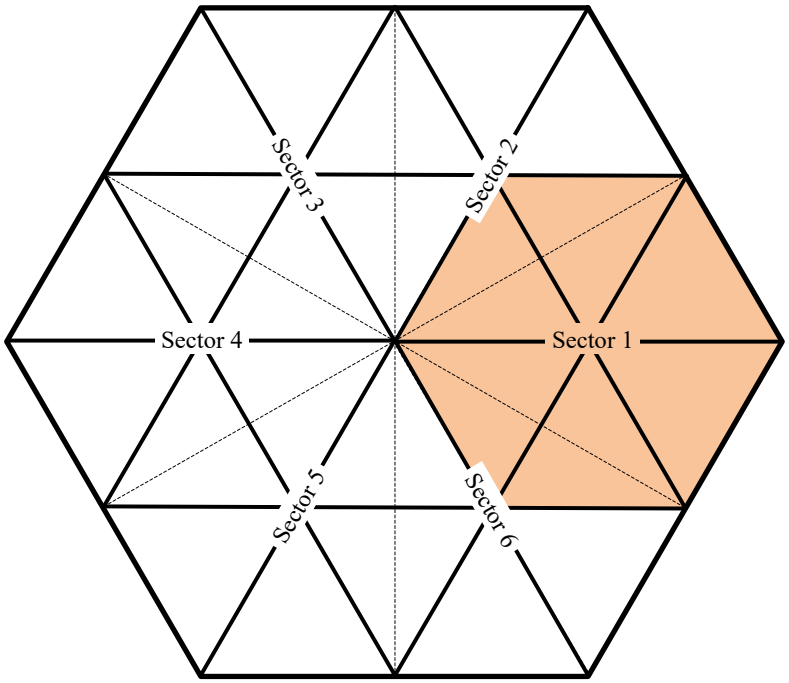

Figure 5.3: Boundary of the sectors in the 3-level space vector diagram

Figure 5.3 depicts the boundary of Sector 1 in the 3-level space vector diagram. It also shows that Sector 1 intersects with Sectors 2 and 6. The remaining sectors can be explained in a similar manner. In other words, there are six identical overlapping sectors in the 3-level space vector diagram. Each sector overlaps with two adjacent sectors. In the case where the voltage and current vectors are not in phase, the voltage vector might lay in one of the intersected areas. However, the location of the current sector decides which sector the sub-vectors' calculation should be based on.

Figure 5.4 depicts the location of the six sectors in the ideal case where the polarity of both voltage and current vectors is identical. In this case, the voltage vector cannot lie on the intersected areas since both vectors are moving together around the space vector diagram.

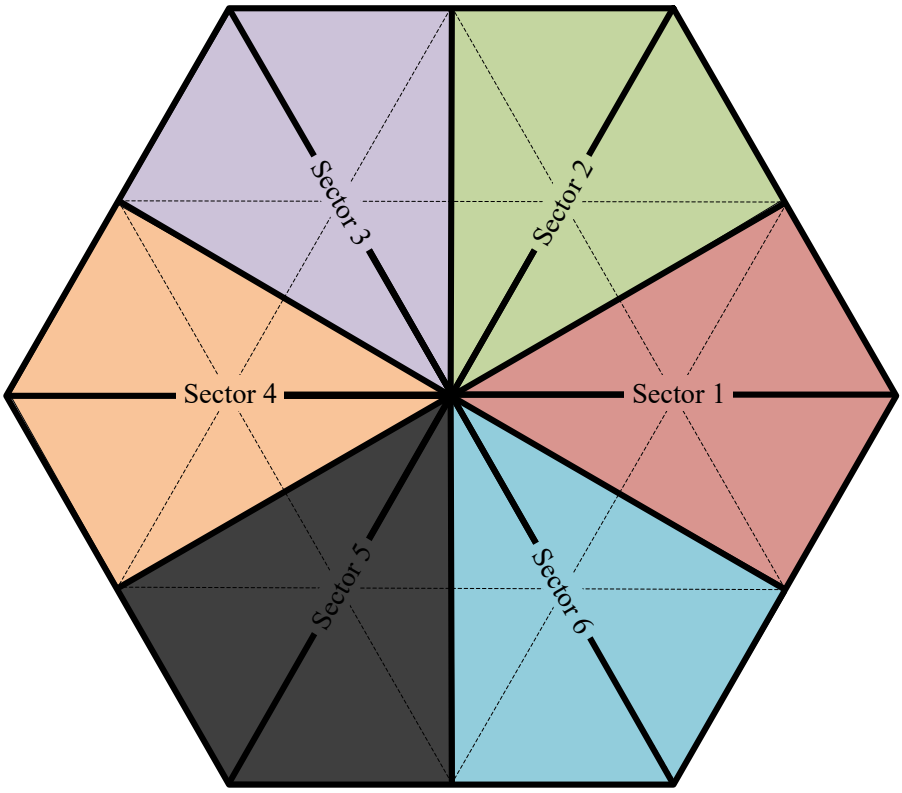

Figure 5.4: Sectors in the 3-level space vector diagram

5.2.2. Angle Normalization

Normalizing the angle (Φ) is a significant step in simplifying the SVPWM for the Vienna rectifier. The main idea of angle normalization is to rotate the voltage vector, which is located in Sectors 2 to 6, to Sector 1. The calculations are then performed on the basis of Sector 1, despite the location of the reference vector. Equation (28) illustrates the mathematical explanation of angle normalization:

$$\Phi = \theta - [Sector\ (I) - 1] * 60^{o} \tag{28}$$

Note: $Sector\ (I)$ is the current sector.

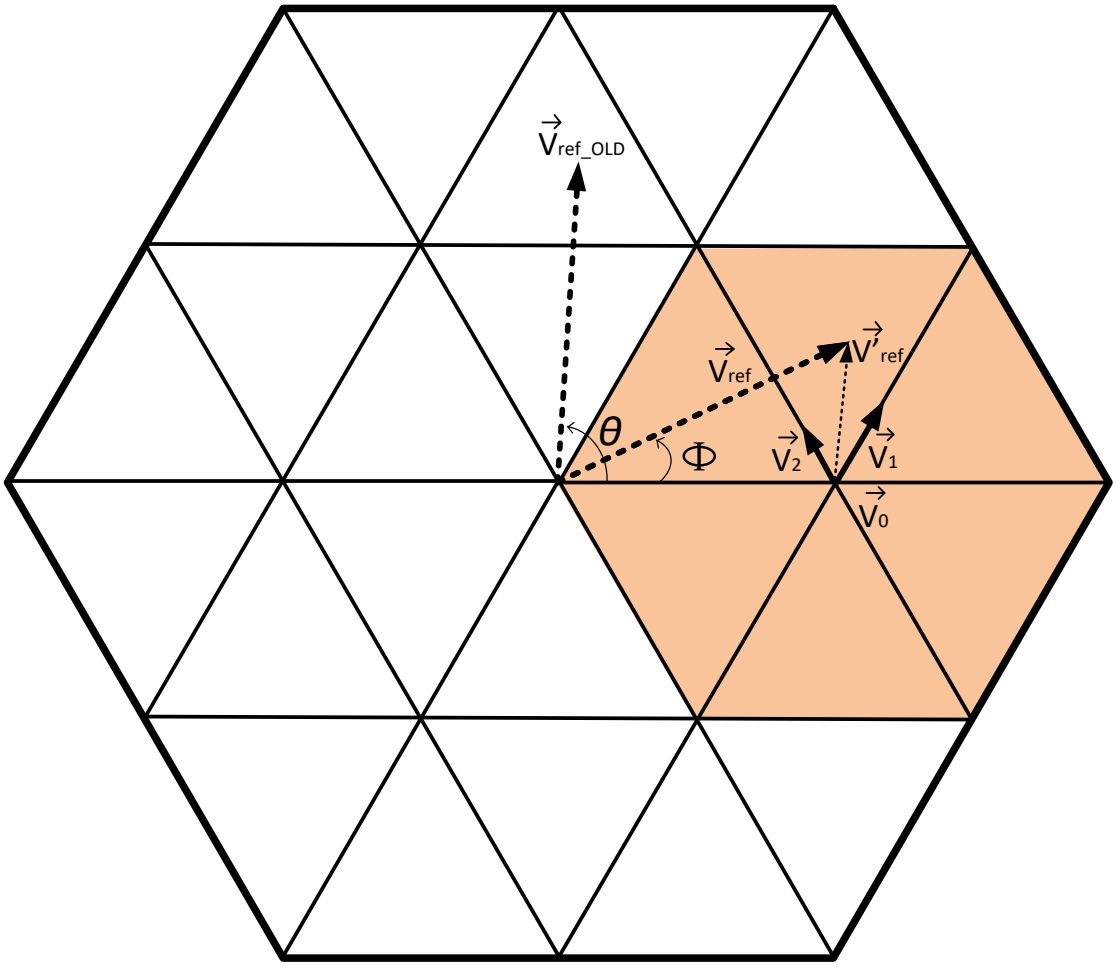

Figure 5.5: Example of the normalized angle

Figure 5.5 depicts the rotation of the reference vector (Vref) on the 3-level space vector diagram to lie in Sector 1. As illustrated in Figure 5.5 the reference vector (Vref_OLD) is located in Sector 2. The normalization method is then used to shift the reference vector to Sector 1 (shaded in pink). The result of the normalization method is the new vector (V′ref). Since the six sectors are identical, there is no need for a unique formula for each sector. In other words, the reference vector is rotated by an offset angle (φ) to make it arbitrarily fall in the first sector, which simplifies the Dwell time calculation process. For instance, if the reference vector has an angle of 70 degrees, which falls in Sector 2, the angle will be normalized (Φ), using equation (26), to be equal to 10 degrees, which falls in Sector 1. This process unifies the Dwell time calculation for all of the sectors to only perform in Sector 1. As shown in Figure 5.5, the reference vector is shifted by the offset angle (φ) in order for all of the Dwell time calculations to be performed based on Sector 1.

5.2.3. Sub-vector Calculations:

In SVPWM, the reference vector is synthesized by the three nearest vectors. In order to do that, the location of the reference vector within Sector 1 must be specified via several steps:

1- The location of the reference vector is determined whether it is in the upper or lower half of Sector 1.
2- The triangle, which the reference vector lies in, is identified.
3- Calculating the sub-vectors V1, V2, V0

The listed steps are explained further in this chapter.

In the first step, the location of the reference vector is determined whether it is in the upper or lower half of Sector 1. Figure 5.6 depicts a zoomed-in picture of Sector 1, where the

location of the reference vector is determined based on the polarity of the normalized angle (Φ). For instance, if the normalized angle is positive, the reference vector is located in the upper half of the hexagon (colored in blue).

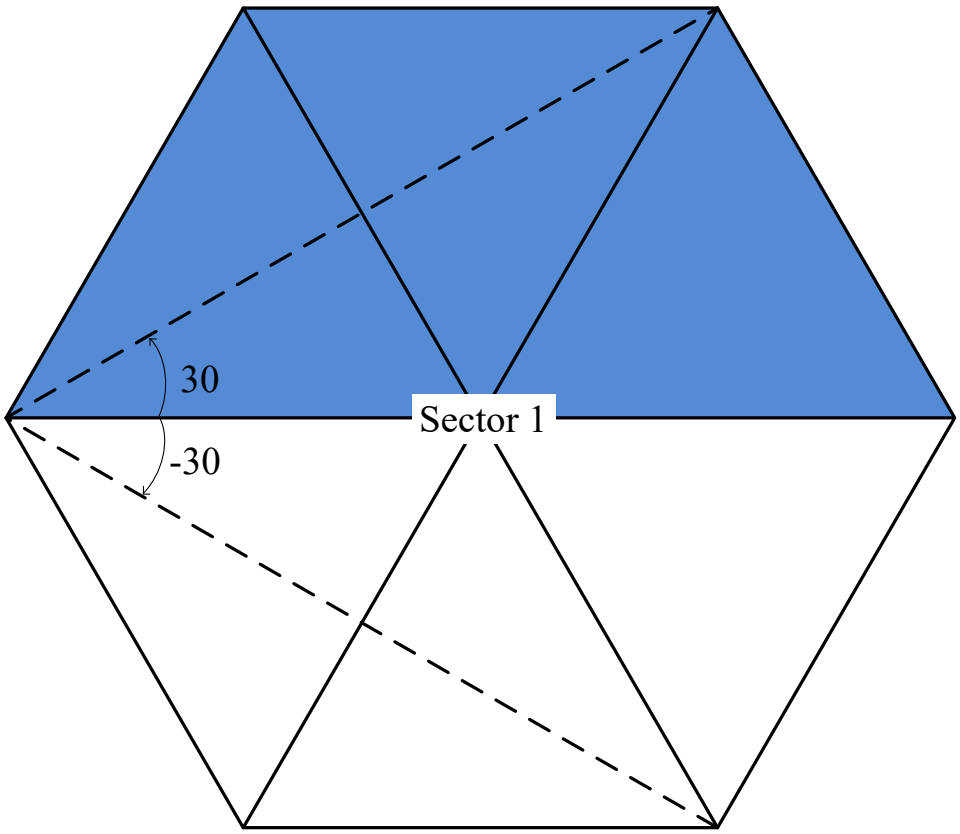

Figure 5.6: Zoom-in Sector 1 of the 3-level space vector diagram

Figure 5.6 shows a bigger picture of Sector 1, which contains six equilateral triangles. Three of these equilateral triangles are located in the upper half of the sector (colored in blue), from 0 to 30 degrees, while the other three are in the lower half of the sector, from 0 to -30 degrees. In addition, the six triangles are identical, which makes the Dwell time calculations or calculating the sub-vectors even simpler because the upper half is used in the calculations while ignoring the lower half. Indeed, an absolute value of the normalized angle $|\Phi|$ is used in the Dwell time calculations.

Similar to the 2-level space vector method, three different vectors (V_1, V_2 and V_0) are used for a specific period of time (T_1, T_2 and T_0) to approximate the reference vector. However, the procedure of calculating the Dwell time is totally different than the 2-level space vector method, as explained in this section.

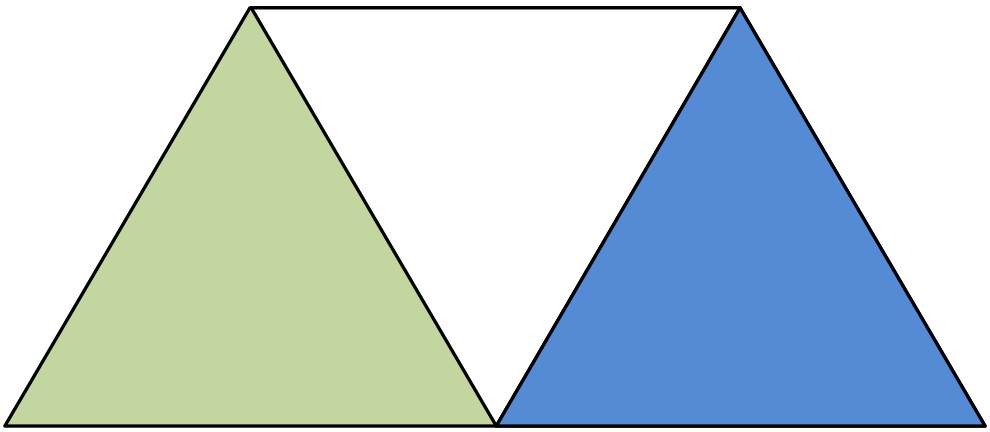

Figure 55.7: Triangles in the upper half of Sector 1

Figure 5.7 depicts the three triangles that are located in the upper half of Sector 1. Since the absolute value of the normalized angle is used in the calculations, as shown in equations (29) to (36), the three triangles shown in Figure 5.7 are enough to calculate the sub-vectors at any location in the 3-level space vector diagram. This illustrates the significant simplification attained by the provided SVPWM method. Figure 5.7 also illustrates the three equilateral triangles that are needed for calculating the Dwell time. Each equilateral triangle has its own formulas for calculating. Therefore, the second step is to determine which of these three triangles the reference vector falls in, as shown in equations (29) to (30).

$$|V_{ref}| \leq \frac{\cos(30^o)}{\sin(60^o+|\Phi|)} \tag{29}$$

$$|V_{ref}| \geq \frac{\cos(30^o)}{\sin(60^o-|\Phi|)} \tag{30}$$

If the condition in equation (29) is satisfied, the reference vector (V_{ref}) falls in the first triangle (colored in green as shown in Figure 5.7. However, if the condition in equation (30) is satisfied, the reference vector (V_{ref}) falls in the third triangle (colored in blue as shown in Figure 6). If neither equation (29) nor equation (30) are satisfied, the reference vector (Vref) falls in the middle triangle.

The third step is to calculate the sub-vectors V1, V2 (known as Dwell time calculation) as explained in this section.

Equations (31) to (32) determine the Dwell time for the vectors when the reference falls in the first triangle, as follows:

$$V_1 = 1 - |V_{ref}| \frac{\sin(60^o + |\Phi|)}{\cos(30^o)} \tag{31}$$

$$V_2 = |V_{ref}| \frac{\sin(|\Phi|)}{\cos(30^o)} \tag{32}$$

Figure 5.8 to 5.10 depict the axis locations of the sub-vectors when the reference vector lies in one of the three triangles. It also shows that the center of the hexagon is shifted from the center.

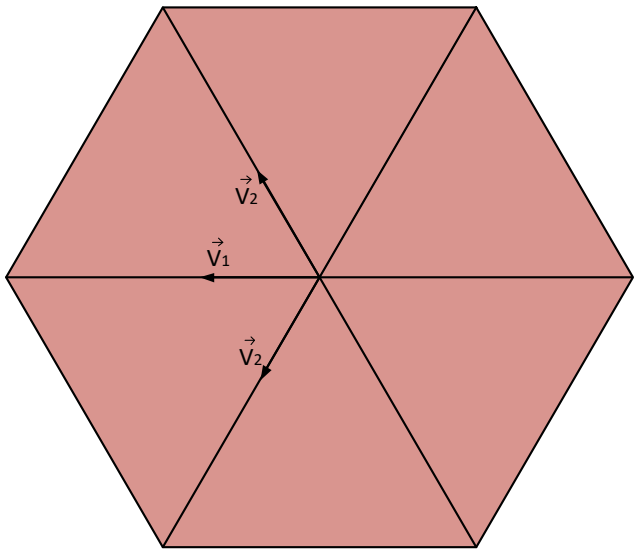

Figure 5.8: Position of the vectors V_1 and V_2 when V_{ref} falls in the first triangle

Equations (33) and (34) calculate the Dwell time when the reference voltage $|V_{ref}|$ falls in the middle triangle.

$$V_1 = |V_{ref}| \frac{\sin(60^o + |\Phi|)}{\cos(30^o)} - 1 \quad (33)$$

$$V_2 = 1 - |V_{ref}| \frac{\sin(60^o - |\Phi|)}{\cos(30^o)} \quad (34)$$

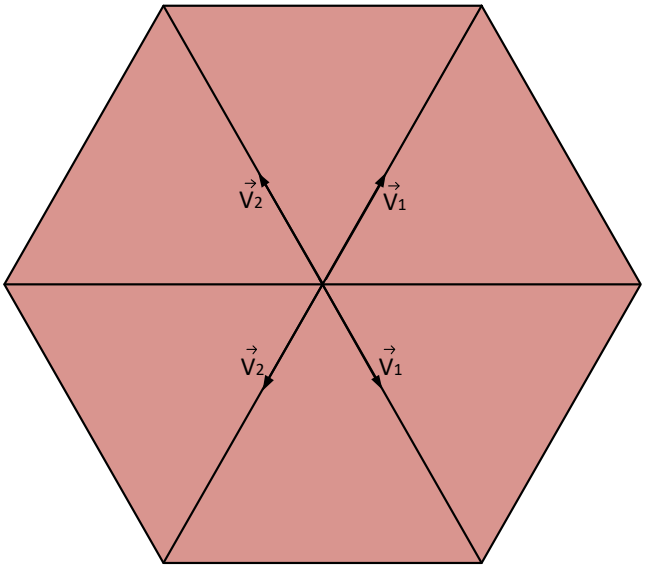

Figure 5.9: Position of the vectors V_1 and V_2 when V_{ref} falls in the middle triangle

Finally, Equations (35) and (36) calculate the Dwell time when the reference falls in the third triangle:

$$V_1 = |V_{ref}| \frac{\sin(60^o - |\Phi|)}{\cos(30^o)} - 1 \quad (35)$$

$$V_2 = |V_{ref}| \frac{\sin|\Phi|}{\cos(30^o)} \quad (36)$$

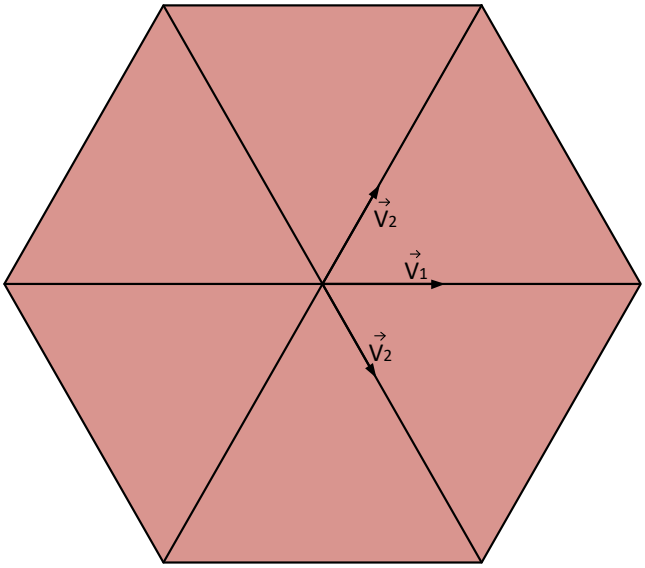

Figure 5.10: Position of vectors V_1 and V_2 when V_{ref} falls in the third triangle

Note: Equations (31) and (36) calculate the sub-vectors based on the new center point of Sector 1 with the redundant vector for all triangles provided in equation (37).

$$V0 \ = 1 - V2 - V1 \tag{37}$$

5.2.4. Shortening Sub-vectors:

Since the sub-vectors calculated in the previous section are a percentage of the switching time, their summation should not exceed 1. However, where the reference vector is located outside of the hexagon, action must be taken by the modulator in order to avoid a failure in the system. In fact, the simplified SVPWM method provides an optimized selection of sub-vector reduction to minimize the error. The values of the sub-vectors represent the time ratio of each switching state for a given switching cycle. Therefore, the sub-vectors are required to be shortened when their sum is greater than one.

Figures 5.11 to 5.13 depict the procedure of shortening the sub-vectors. As illustrated, the shortening is performed for the longer sub-vector in the outer and the inner triangle while it is applied to the shorter sub-vector in the middle triangle.

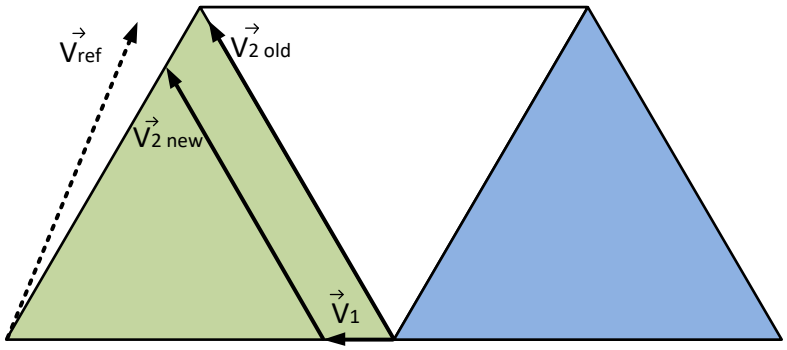

Figure 5.11: Examples of sub-vectors shortening in the inner triangle

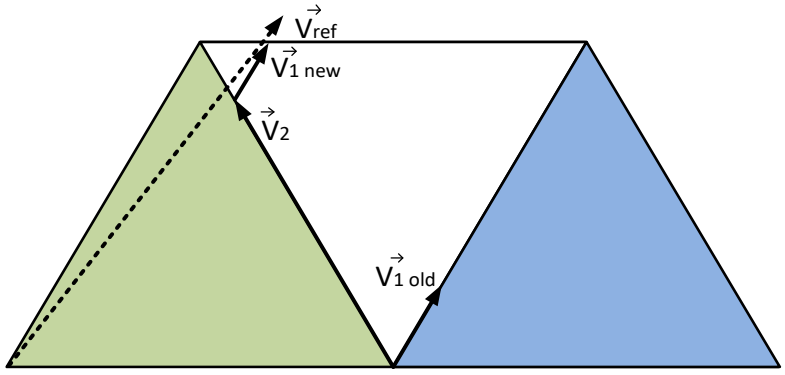

Figure 5.12: Examples of sub-vectors shortening in the middle triangle

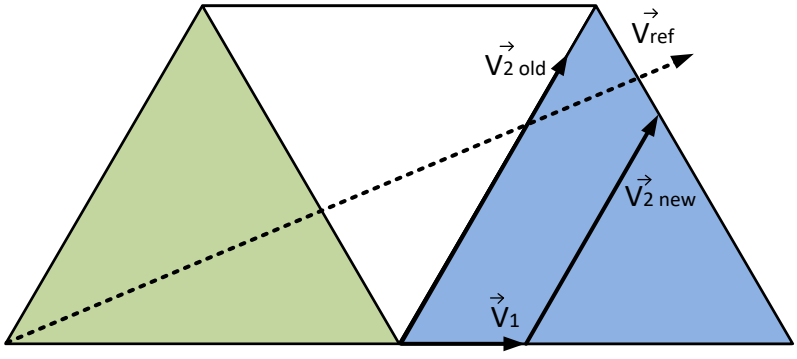

Figure 5.13: Examples of sub-vectors shortening in the outter triangle

5.2.5. Pulse Generation

The last step in the simplified SVPWM technique is generating the pulses. This step uses the results of the previous sections. As illustrated in Figure 5.14, each triangle has a unique switching pattern. A lookup table needs to be implemented to retrieve the switching pattern of each triangle. In the lookup table, each triangle is represented by a number called (S), which is the sum of several numbers. In the section of the Sector Identification, the sector is identified and a number is added to S as illustrated in equation (38).

$$S = Sector\ (I) - 1 \tag{38}$$

Then, the number 18 is added to S if the reference vector lays in the negative half of the sector, while nothing is added to S when the reference vector falls in the positive half of the sector. Finally, the numbers 1, 7 and 13 are added to S if the reference vector lays in the outer, middle and inner triangles respectively.

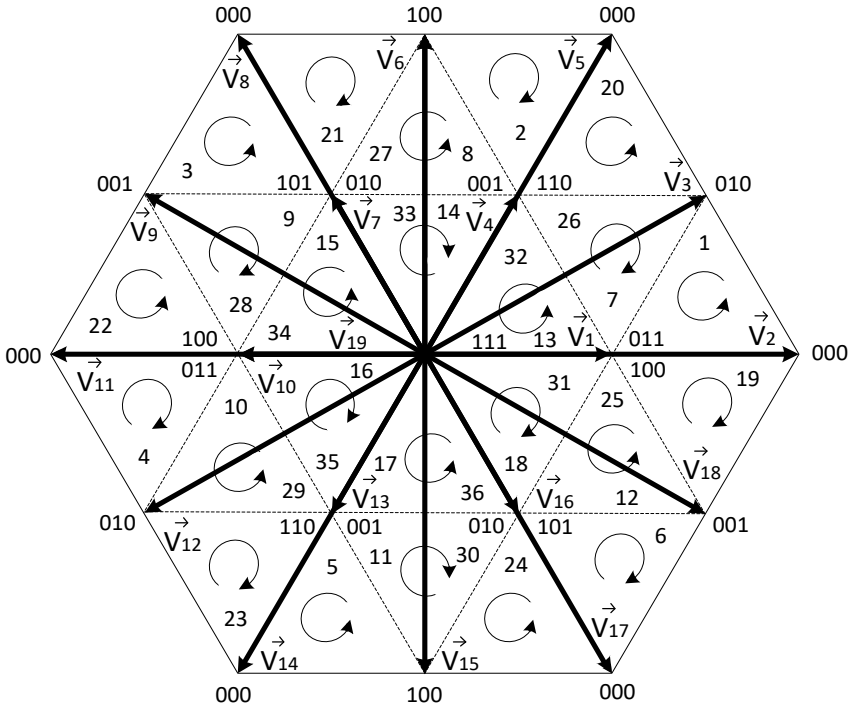

Figure 5.14: Directions of the switching states in the 3-level SVPWM method

Figure 5.14 depicts the directions of the switching patterns in each triangle which minimizes the number of times the switches are turned ON and OFF and reduces the switching losses when the reference vector travels from one triangle to another. In addition, the illustration shows that each triangle is represented by a unique number, which provides the ability to retrieve the switching pattern of each triangle easily. Figure 5.15 depicts how the switching sequence is produced when the reference vector falls in Triangle 1 (S=1). It illustrates that the resultant sub-vectors are compared to a triangular wave which then generates a 7-segment switching pattern.

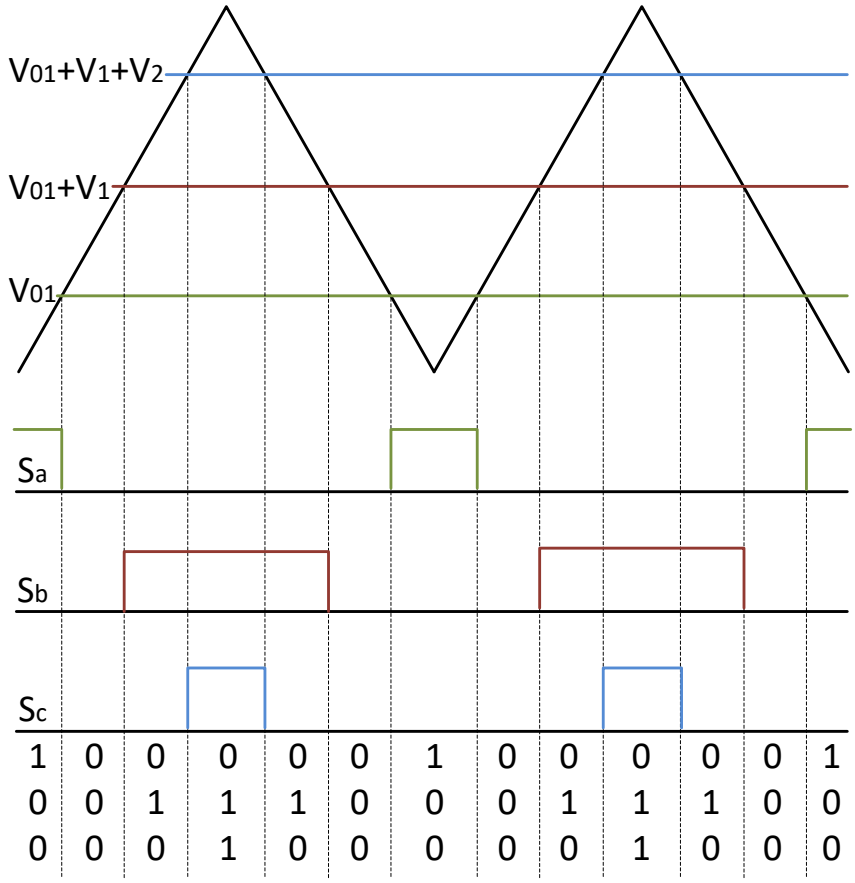

Figure 5.15: Example of the pulse generation when the reference vector falls in triangle 1

5.3. Capacitor Voltage Balancing

As one requirement of the topology is to force the capacitors mid-point to have zero volt (an average of zero), the procedure of capacitor balancing is explained in this section. At the center of each sector, there are vectors that can be applied using two different switching states. These vectors are known as the redundant vectors. Although the two switching states result in the same voltage vector, their effect on the capacitor mid-point is the opposite. For example, if the redundant state "100" charges the capacitors' mid-point, the redundant state "011" discharges the capacitors' mid-point. In order to balance the capacitors' voltages, a PI controller is used to generate the required ratio for the two redundant states, as shown in equations (39) and (40). Table 5.6 illustrates the effect of the redundant states on the capacitor mid-point.

$$V01 = V0 * k \tag{39}$$

$$V02 = V0 - V01 \tag{40}$$

Where k is the output of the PI controller

Table 5.6: Impact of each switching state on the neutral point (n)

Switching State	Current in Capacitor mid-point (io)
0 0 0	0
1 0 0	ia
0 0 1	ic
1 0 1	-ib
0 1 0	ib
1 1 0	-ic
0 1 1	-ia
1 1 1	0

In conclusion, in this chapter, space vector analysis for the Vienna rectifier is carried out and a step-by-step explanation of the novel simplified SVPWM for the Vienna rectifier is provided. The method adopted reduces the computational effort and reduces the harmonics, as the deployment of the turning ON and OFF for the active switch is minimized. Finally, a method for balancing the capacitors is illustrated.

5.4. Space Vector Controller Circuit

As depicted in Figure 5.16, the Vienna rectifier contains two main control loops, known as a faster inner control loop (shaded in light pink) and a slower outer control loop (shaded in dark pink). The outer control loop is responsible for controlling the output voltage. As illustrated in Figure 5.16, the reference voltage is compared to the sensed output voltage to extract the error signal. A PI controller (PI1) is then used to process the error and provide a reference for the required active power. The inner control loop is used to control the rectifier's input current. The rectifier's input current is sensed and synchronized with the mains. Then, the current's active component is compared to the reference active power produced by the voltage control loop, which needs to be processed (by PI2) to provide the "d" component of the space vector's reference vector. However, the reactive component of the input current is compared to zero to attain a unity PF. Hence, the produced error signal is then processed by a PI controller (PI3) to produce the "q" component of the space vector's reference vector.

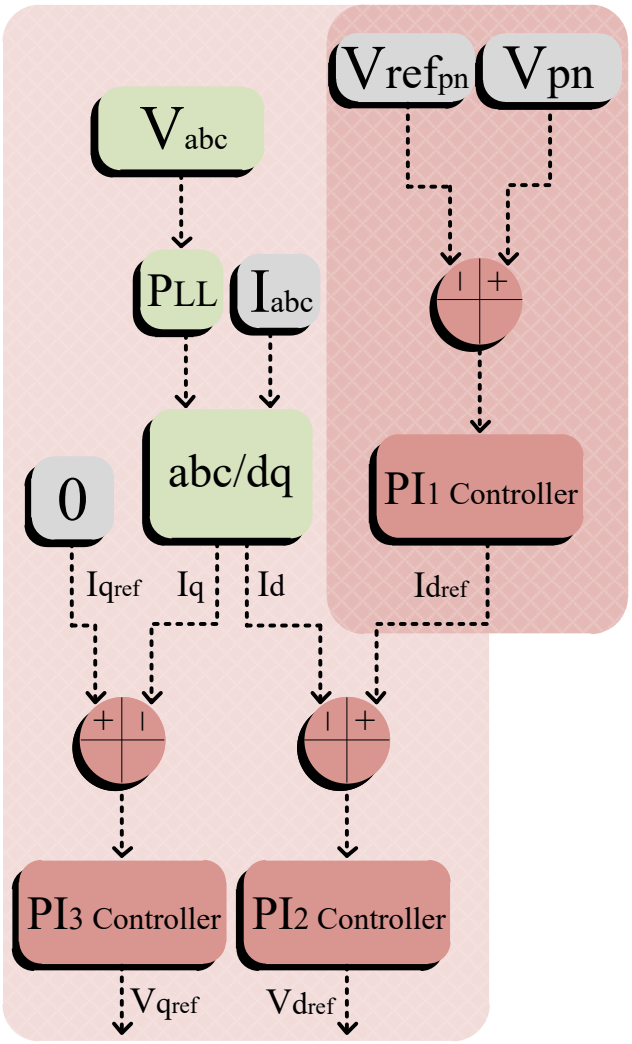

Figure 5.16: Vienna rectifier's controller circuit

5.5. Implementing the Simplified SVPWM

Figure 5.17 depicts the block diagram for the explained simplified SVPWM. The light green blocks are responsible for synchronization and extraction of the reference vector's amplitude and angle. On the other hand, the pink blocks represent steps of the simplified SVPWM method. The switching sequence block is the block that contains the switching patterns of each triangle in the 3-level SVPWM diagram, as shown in Figure 5.1.

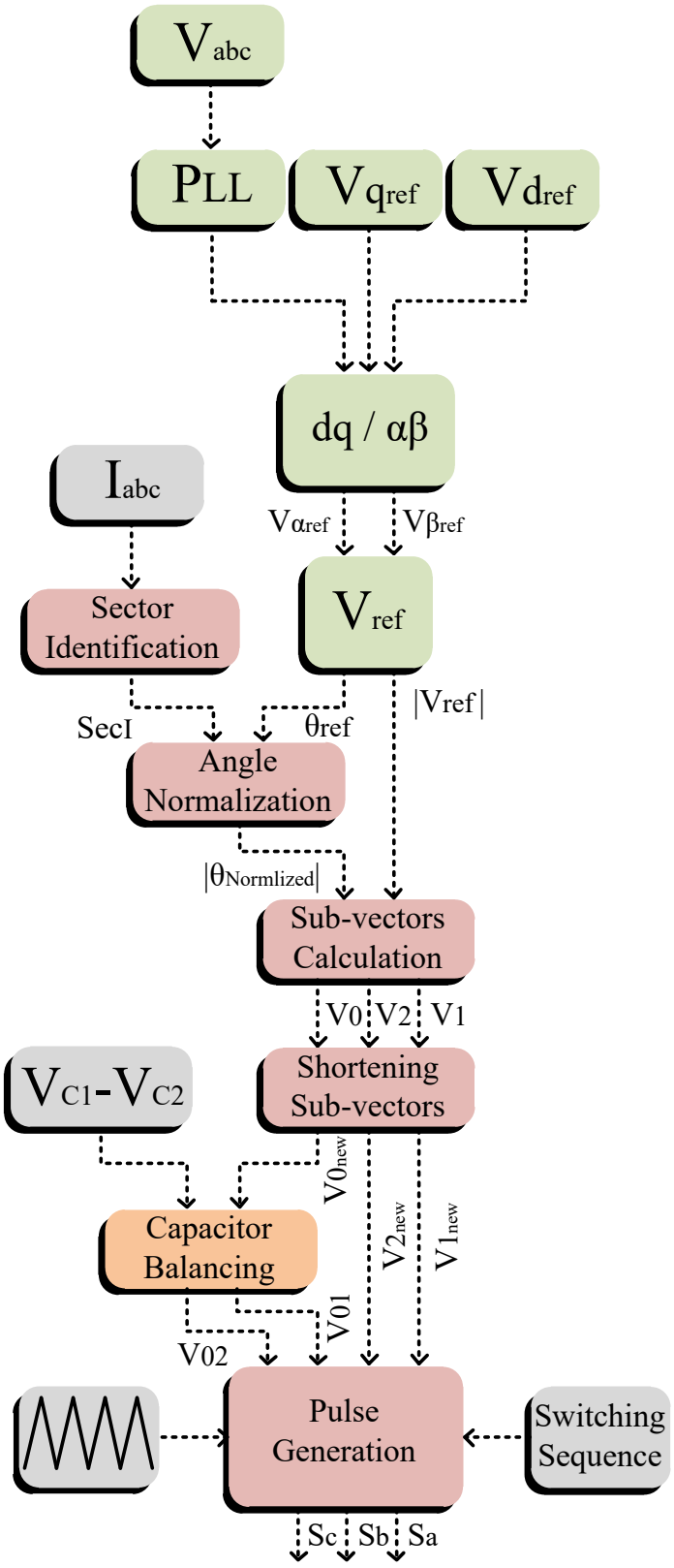

Figure 5.17: Block diagram for the simplified SVPWM for the Vienna rectifier

Chapter 6. Simulation Results for the Vienna Rectifier Using the Simplified SVPWM

In this chapter, the simulation result of the Vienna rectifier using the simplified SVPWM is provided. Several tests are performed to verify the robustness of the explained modulation method. Also, the maximum and minimum boosting ratio is explained. The results of different tests are discussed and analyzed in this chapter.

6.1. Simulation Tests:

In order to verify the functionality of the simplified SVPWM method, a simulation model has been designed and implemented in MATLAB/Simulink, the results of which are discussed in this chapter. To check the robustness of the analysed modulation technique, different faults have been applied. The model is tested under sudden load change, unbalanced capacitors voltage, capacitor mismatch and capacitor short-circuit. Finally, the relationship between the rectifier's efficiency and output power is explained. The model parameters used for the simulation are shown in Table 6.1.

Table 6.1: Vienna rectifier's parameters

Parameters	Value
Input Voltage	220 V
Output Power	78 kW
Output Voltage	750V
Mains Frequency	50 Hz
Switching Frequency	10 kHz
Inductor filters	0.7 mH
Capacitor filters	6000 uF

6.1.1. The Ideal Case (no fault applied)

Figure 6.1 depicts the voltage and current sectors attained in the simplified SVPWM. It is clear that the modulation technique successfully derived the voltage and current vectors to be in phase.

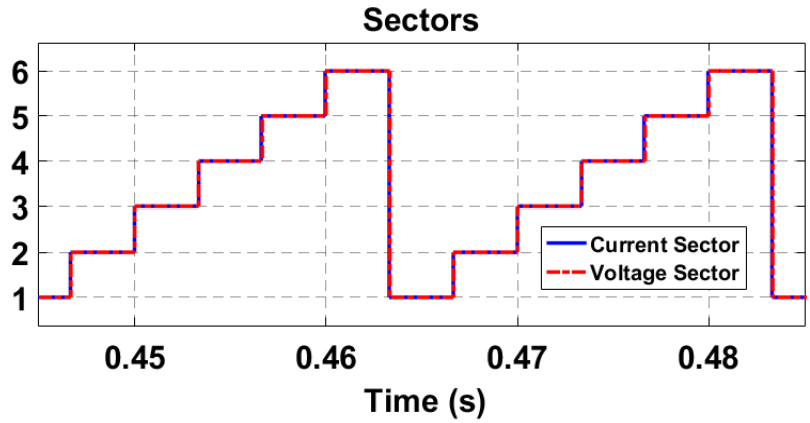

Figure 6.1: Voltage and current sectors

Figures 6.2 to 6.7 depict the simulation results for the ideal case (no fault is applied). The results illustrate a sinusoidal input current, a low ripple output voltage, a well-balanced capacitor's voltage, and a near unity PF.

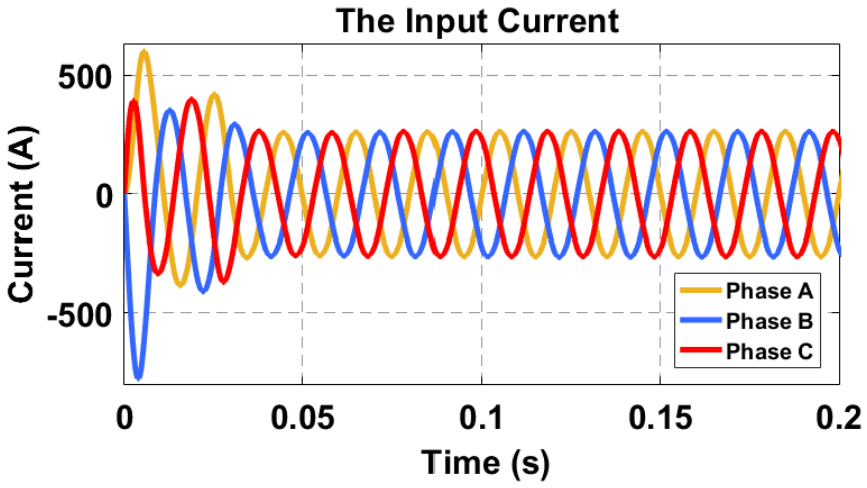

Figure 6.2: Vienna rectifier's input current

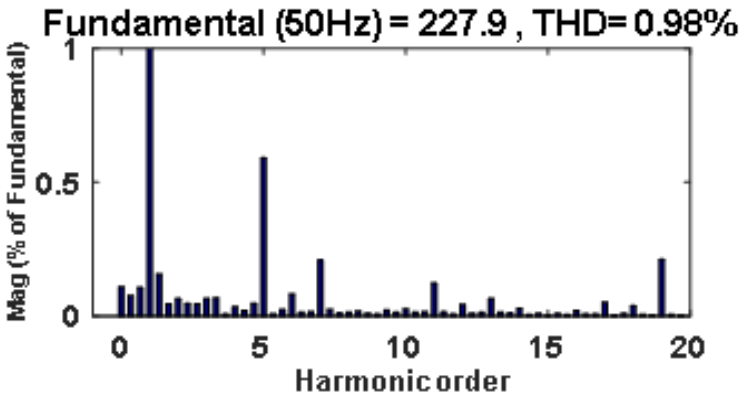

Figure 6.3: THD of the input current

The Vienna rectifier's 3-phase input current is depicted in Figure 6.2. It is clear that the modulation technique forces the input current to have a sinusoidal shape. Figure 6.3 illustrates detailed information of the input current harmonics. The THD is very low (less than 1%), which means the rectifier's filters can be reduced even more. The THD figure illustrates that the fundamental component is 100% while 5^{th} harmonics is 0.6 %, 7^{th} is harmonics is 0.2%, 11^{th} harmonics is 0.1% and 13^{th} harmonics is 0.08%.

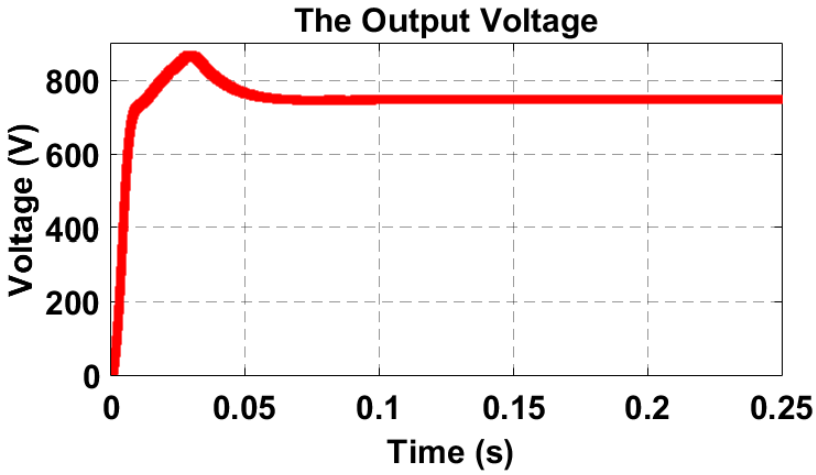

Figure 6.4: Output voltage of the Vienna rectifier

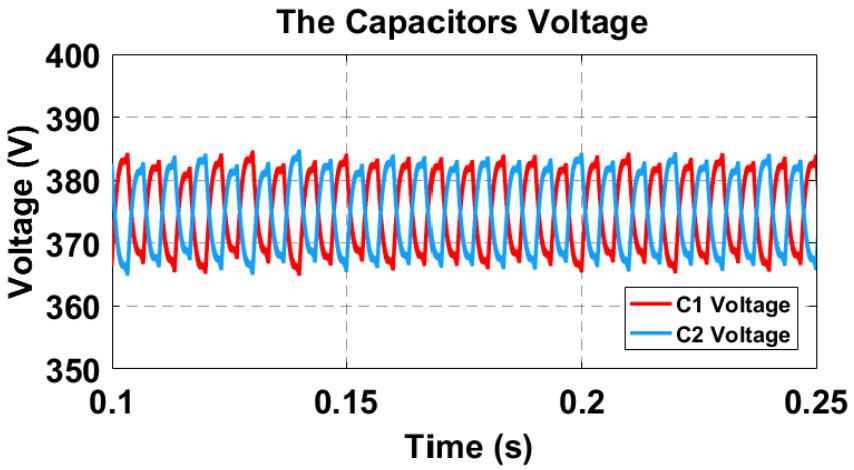

Figure 6.5: Capacitors voltages of the Vienna rectifier

The rectifier's output voltage is depicted in Figure 6.4. It is obvious that the voltage ripple is small. In addition, Figure 6.5 illustrates the well-balanced capacitor voltages gained by using the space vector method. Proper balancing for the capacitor voltages leads to a smaller voltage ripple at the output and a better sinusoidal shaped current. Both figures shows that the simplified modulation method can result in a well-balanced voltage at the DC-link.

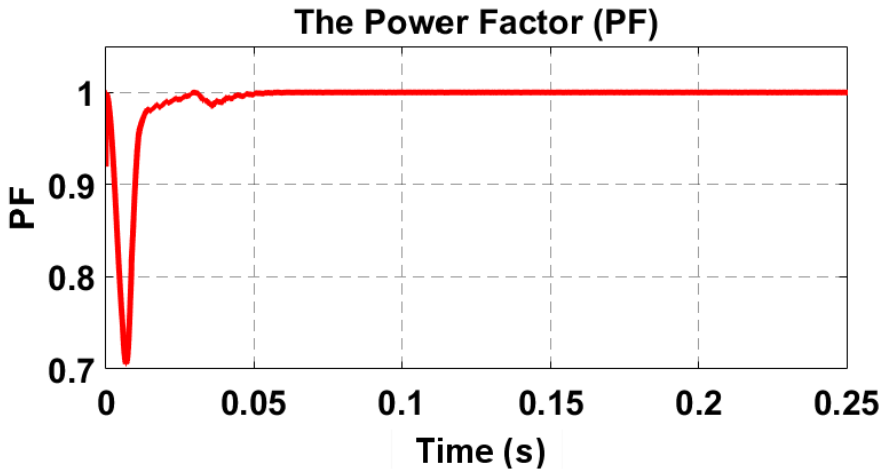

Figure 6.6: Power factor in the Vienna rectifier

Near unity PF is achieved in the Vienna rectifier which reaches 0.9999 as illustrated in Figure 6.6. Figure 6.7 depicts the multi-level phase-phase voltage of the Vienna rectifier.

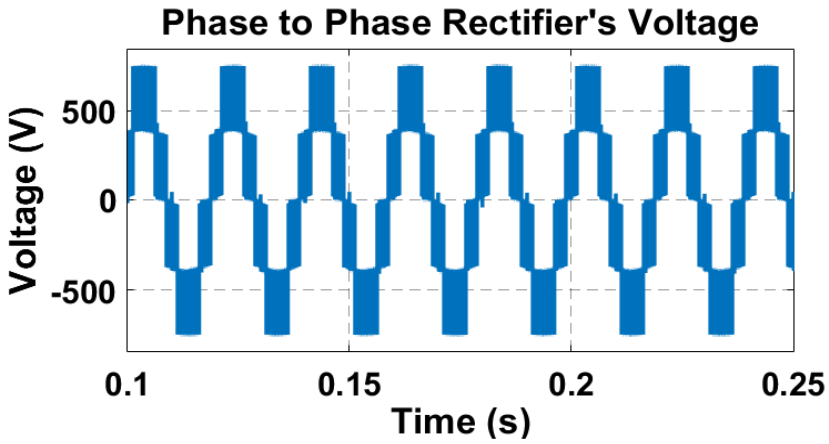

Figure 6.7: Vienna rectifier's phase-phase voltage

6.1.2. Capacitors Voltage Balance under Fault Condition

In this test, a fault resister is connected in parallel with one of the capacitors (C1) to check the capability of the modulation method. Figures 6.8 to 6.12 depict the resulting THD, PF, output voltage ripple and capacitors voltage ripple at different levels of unbalanced capacitor voltages.

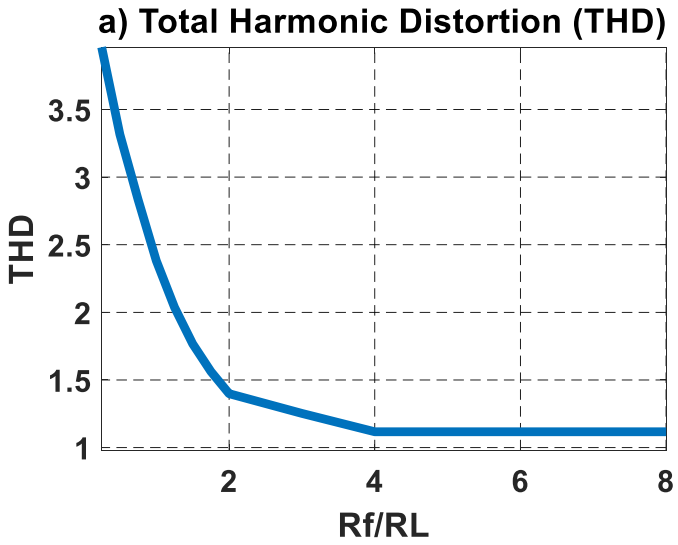

Figure 6.8: THD in voltage unbalance test

Figure 6.8 shows that the THD reaches around 4% when the maximum fault is applied and drops to less than 1% as the fault is reduced. In fact, the THD is below 1.5% when the fault resistor is larger than 200% of the load resistor.

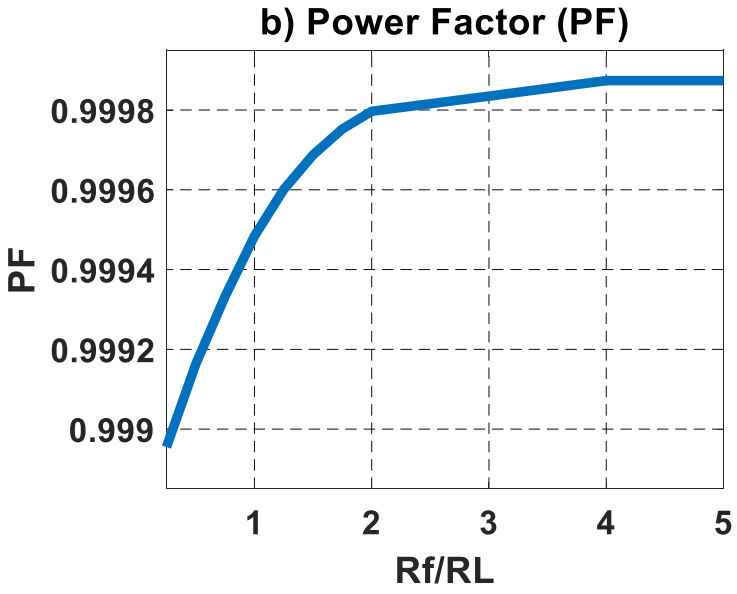

Figure 6.9: Power factor in voltage unbalance test

Figure 6.9 depicts the change in PF as the fault is changed. The minimum PF of 0.9987 is obtained at the maximum applied fault, while the PF reaches up to 0.9996 as the fault is decreased. However, the change in PF is not significant as the capacitor balancing technique has the ability to balance the capacitor voltages even when capacitor C1 is drawing larger current than C2 or vice versa. In other words, the modulation technique has the ability to deal with high capacitor parametric tolerance. This illustrates the robustness of the explained SVPWM technique as near unity PF is achieved even under the high fault condition.

Figure 6.10 shows that the output voltage ripple reaches 14.7 volts when the maximum fault is applied, which is only 1.9 % of the output voltage. The ripple then starts dropping as the fault is reduced, until it reaches less than 0.03%.

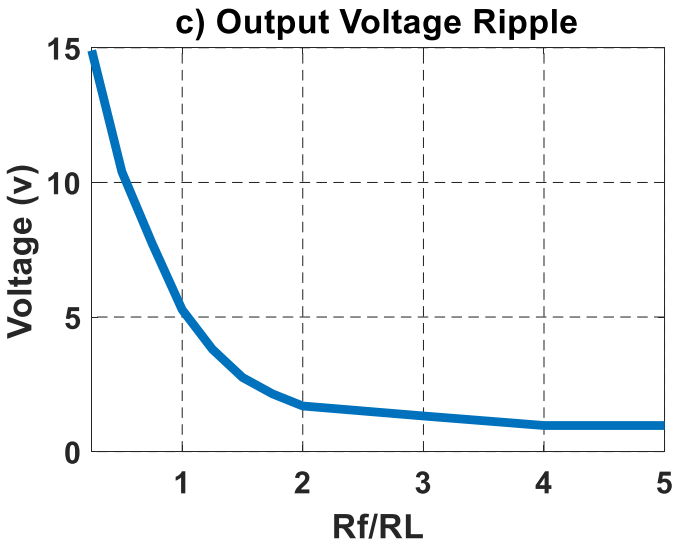

Figure 6.10: Output voltage ripple in voltage unbalance test

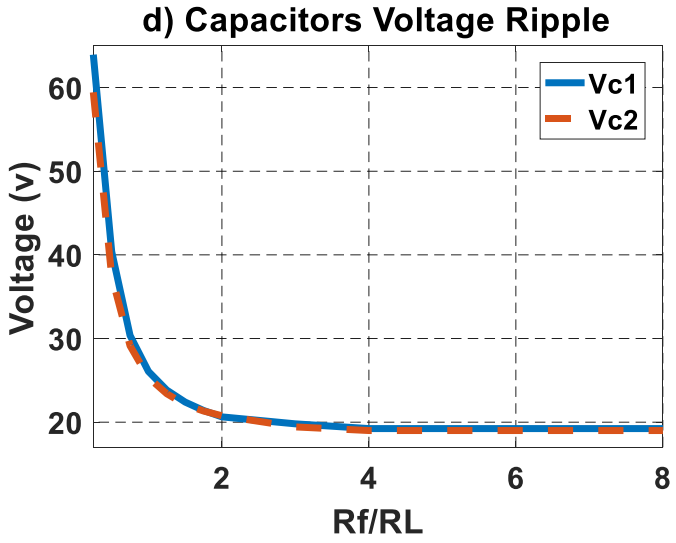

Figure 6.11: Capacitor voltages ripple in voltage unbalance test

As shown Figure 6.11, the capacitors voltage ripple is highly affected by the voltage unbalance test. The voltage ripple reaches approximately 60 volts (17 %) for both capacitors at the maximum applied fault, while it drops to less than 20 volts (5.7 %) as the fault is decreased. In general, the modulation method is able to keep the capacitors voltage balanced and draw a sinusoidal input current for this test.

6.1.3. Capacitors Mismatch Test

The second test is changing the value of the output capacitor (C1) to illustrate the response of the explained modulation technique. Figures 6.12 to 6.15 illustrate how changing the capacitors values effect the THD, PF, output voltage ripple and capacitors voltage ripple. The results are discussed further in this chapter.

Figure 6.12 illustrates the effect on the THD when the capacitors are mismatched. It also shows that the THD reaches 5.25% when C1 is reduced to half of C2. As the value of C1 increases to equal C2, the THD drops down to 0.98%. This shows that the system is capable of maintaining the low THD even when capacitor values are mismatched.

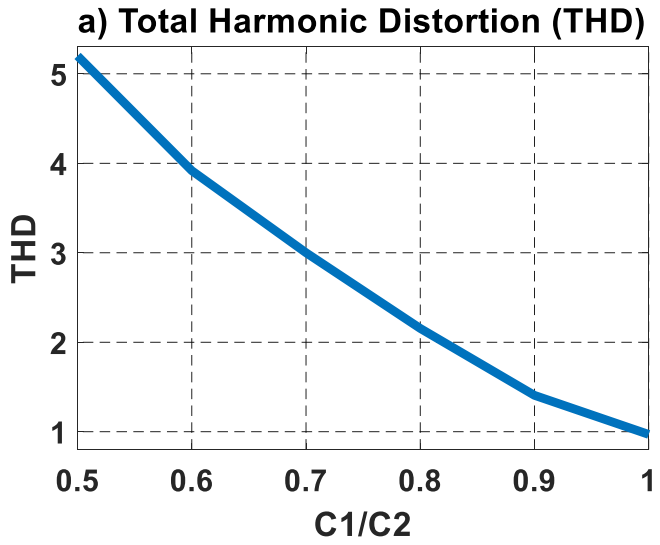

Figure 6.12: THD in capacitor mismatch test

In Figure 6.13, the effect on PF is illustrated where the PF is improving as the similarity of both capacitors is increasing. However, at the extreme fault, when C1 is half of C2, the PF is still above 0.998; this explains the robustness of the system.

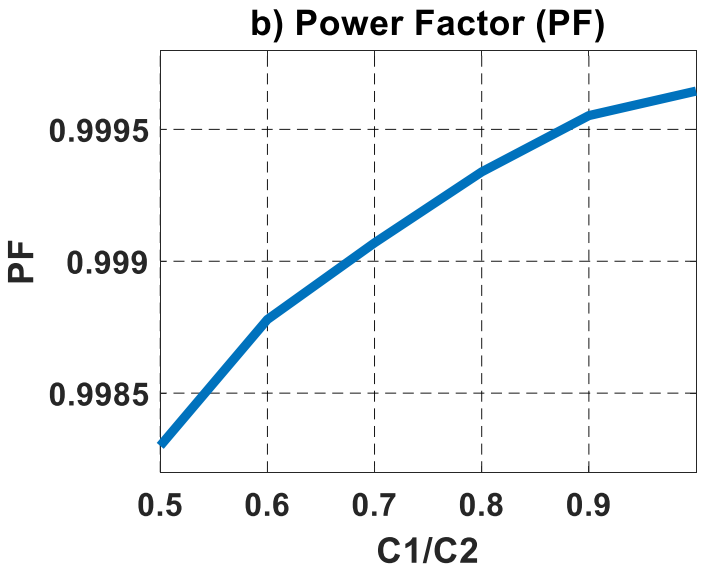

Figure 6.13: Power factor in capacitor mismatch test

In addition, as illustrated in Figure 6.14 reducing C1 to half of the value of C2 increases the output voltage ripple to 3.3%, which is still considered an acceptable voltage ripple. As the percentage of the similarity increases, the voltage ripple decreases, until it reaches 0.26%.

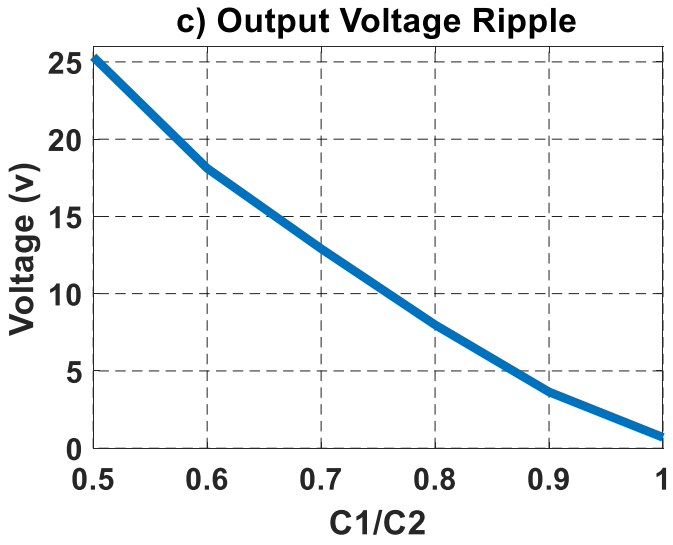

Figure 6.14: Output voltage ripple in capacitor mismatch test

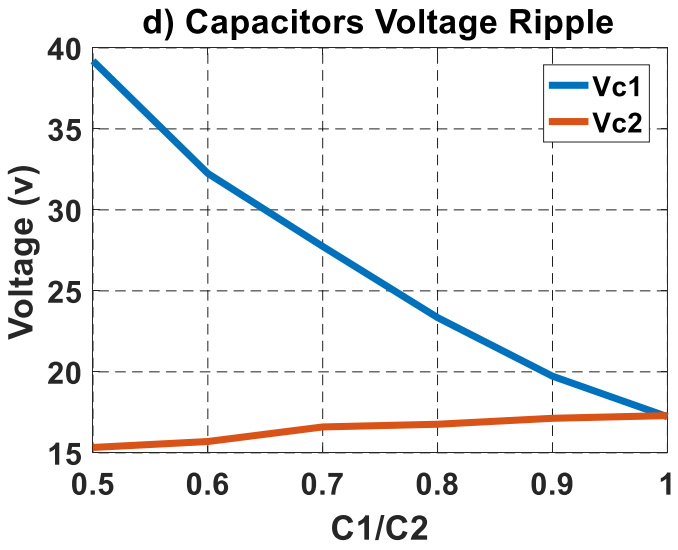

Figure 6.15: Capacitor voltages ripple in capacitor mismatch test

The voltage ripple in the capacitors is illustrated in Figure 6.15as reducing the C1 value to half of C2 increases the voltage ripple on C1 to 40 V while it reduces the voltage ripple on C2 to 15 V.

6.1.4. Capacitor's Short-circuit Test

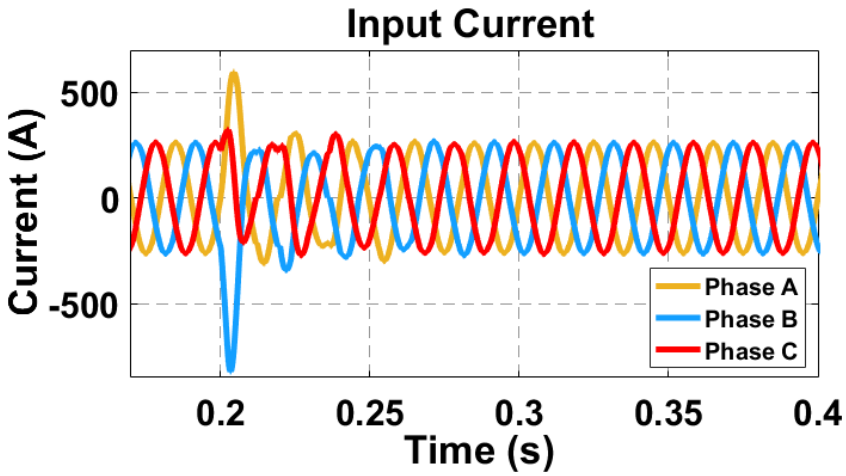

Figure 6.16: Input current when a capacitor is short-circuited temporarly

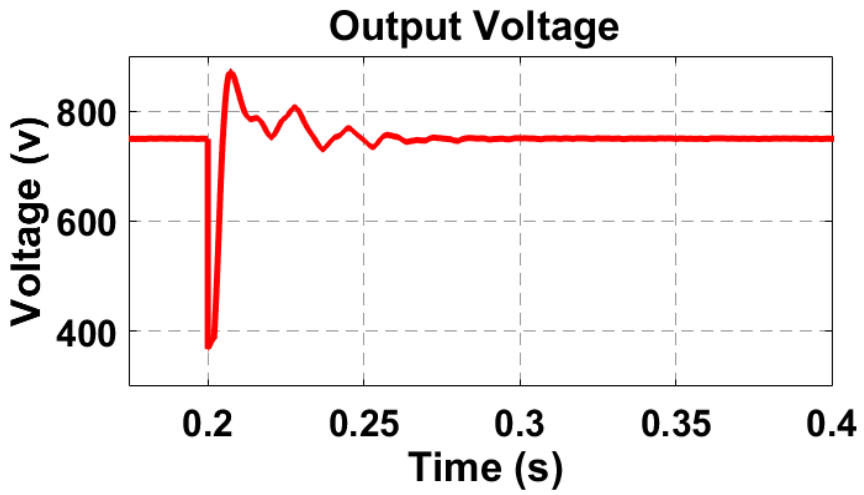

Figure 6.17: Output voltage when a capacitor is short-circuited temporarly

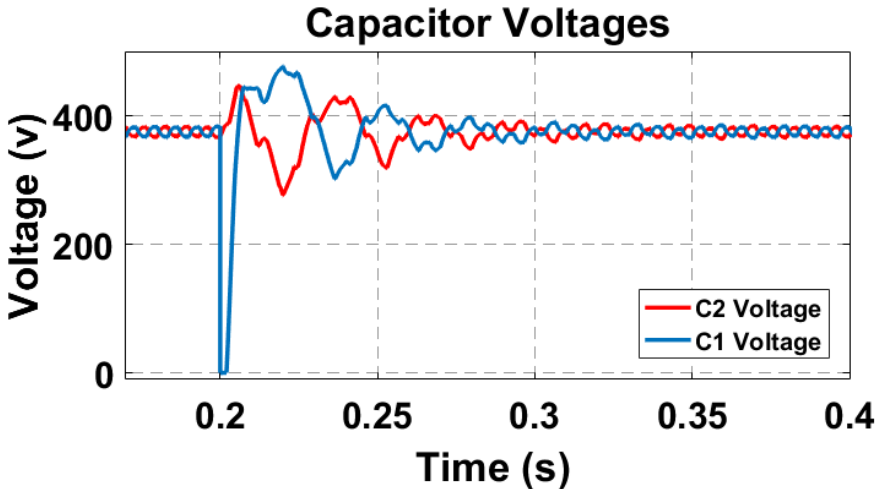

Figure 6.18: Capacitor voltages when a capacitor is short-circuited temporarly

In this test, the capacitor (C1) is short-circuited for 20 switching cycles (2 ms) at t=0.2 s (f = 50Hz). Figure 6.16 shows the response of the rectifier's input current as the capacitor (C1) is short-circuited. The 3-phase current is started to increase at t=0.2s as the capacitor (C1) is short-circuited; then, decreased after t=0.202s when the capacitor (C1) is connected back. It illustrates that the system is able to handle this extreme type of fault and to reshape the sinusoidal input current in less than 60 ms after the fault is applied.

Figures 6.17 and 6.18 depict the response in the output voltage and capacitor's voltages respectively. As shown in Figure 6.17, the voltage of capacitor C1 reached zero at t=0.2 s since it was short-circuited, while Figure 6.18 shows that the output voltage decreased to half of its value at t=0.2s, as only C2 is supplying voltage to the load. Both figures show that the output capacitor voltages reached a steady-state in 60 ms. This means the system has a reliable balancing technique which forces the capacitor voltages to be balanced when an extreme fault is applied.

6.1.5. Load Step Change Test

In this test, a sudden increment of 100% in the load is applied at $t = 0.2s$ seconds. Figure 6.19 depicts the response of the input current during this increment. The input current during this test is decreased to almost half because the load is reduced (required less current). The input current reaches a steady-state in less than 20 ms. On the other hand, the response of the output voltage during this increment is shown in Figure 6.20, while Figure 6.21 shows the response of the capacitor's voltages. The output voltage shows an increment of 8% as the load is changed suddenly, while the current needs time to respond to this change. As illustrated, the output voltage and the capacitor's voltages need around 50 ms to reach steady-state.

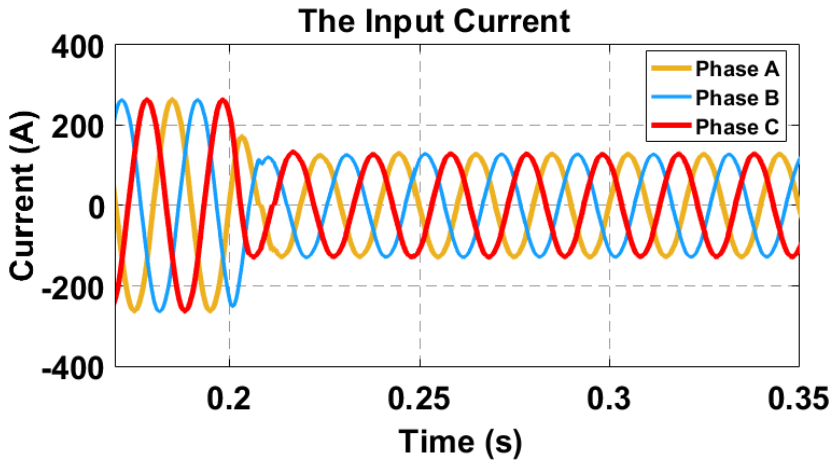

Figure 6.19: Rectifier's input current at a sudden load change test

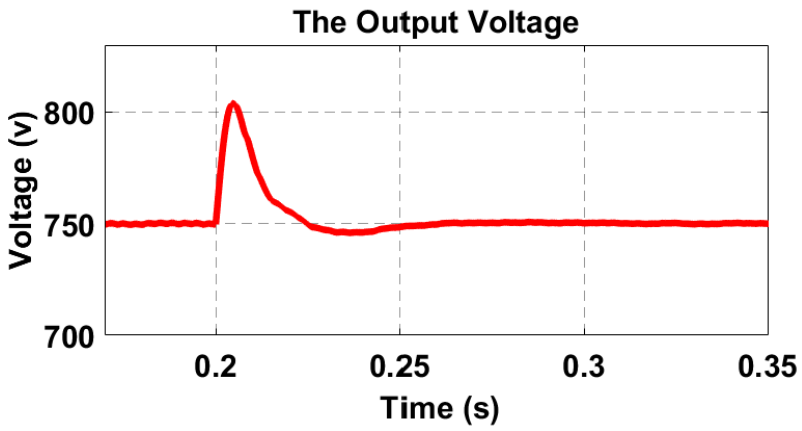

Figure 6.20: Rectifier's output voltage at a sudden load change test

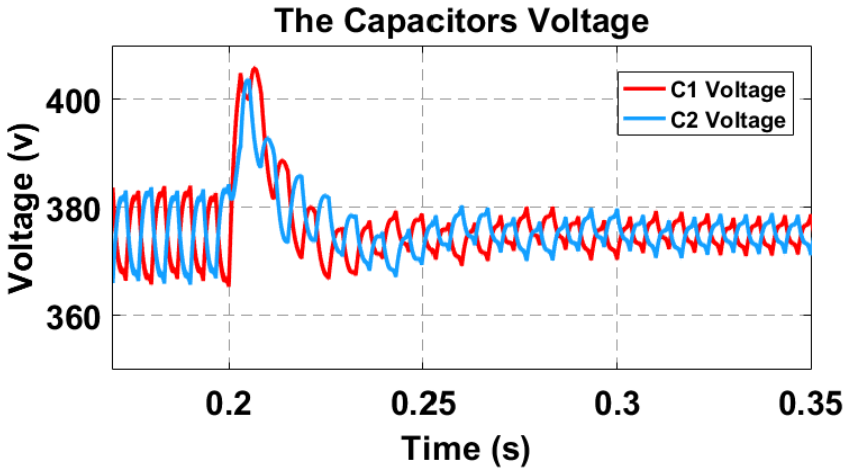

Figure 6.21: Rectifier's capacitors voltage at a sudden load change test

6.2. Vienna Rectifier's Boosting Ratio:

The relation between the boosting ratio of the rectifier and the space vector reference vector is illustrated in Figure 6.22. The figure depicts the 3-level SVPWM diagram with three different circles inside it. The biggest and smallest circles represents the boundary of the reference vector. The smallest circle represent the maximum boosting ratio of the Vienna rectifier which is equal to more than six times of the input phase voltage ($6.3*V_{Phase}$). If the reference vector is moving in the path of the medium sized circle, the boosting ratio is going to be ($3.8*V_{Phase}$). In contrast, the biggest circle represents the minimum acceptable boosting

ratio of the Vienna rectifier. The minimum boosting ratio is twice the input phase voltage ($2.4*V_{Phase}$). In other words, the closer the reference vector to the center of the hexagon the higher the boosting ratio which is logical since the center of the hexagon represents the "111' switching state (meaning all the active switches are conducting and the boost inductors are charging). This means that each capacitor can have a minimum voltage that is equal to the rms input phase voltage. Therefore, the Vienna rectifier is known to have high boosting ratio, which depending on the application, can be an advantage or disadvantage.

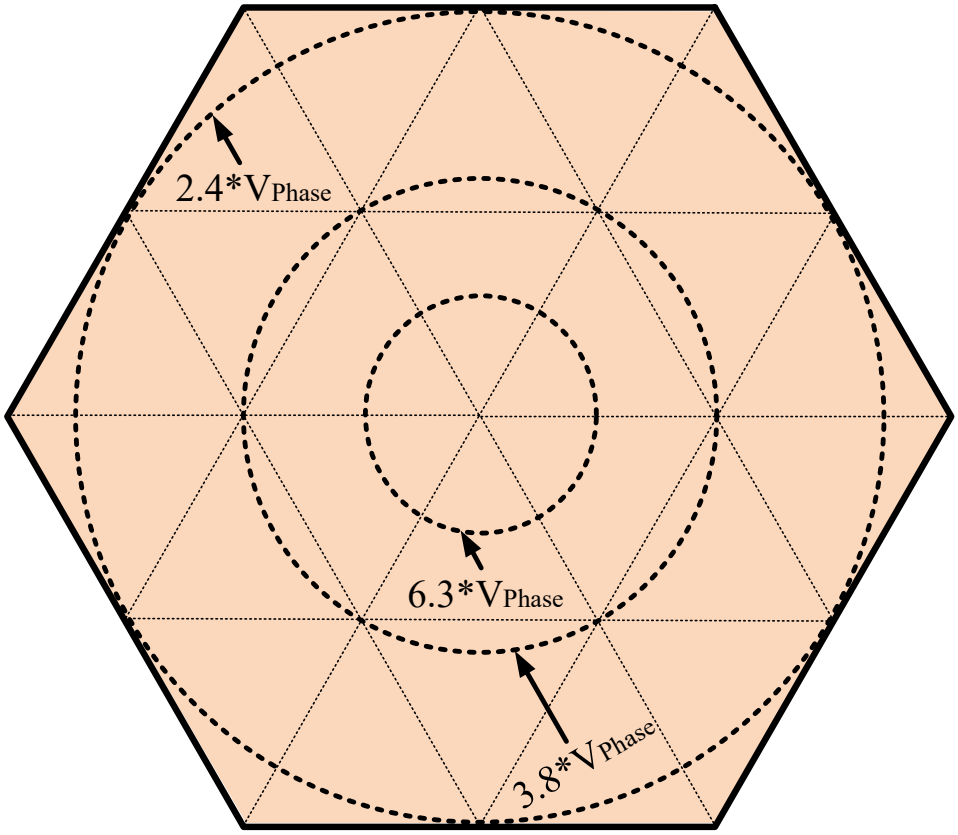

Figure 6.22: Relation between the Vienna rectifier's boosting ratio and SVPWM reference vector

In summary, the simulation results shown in this section illustrated the robustness of the simplified modulation technique explained in this thesis. The simplified SVPWM shows an excellent performance when applying extreme faults, such as unbalanced capacitors voltage,

mismatched capacitors and short-circuited capacitor, and sudden load change. The results prove that less than 1% THD, unity PF and well-balanced capacitors voltage are attainable. Furthermore, the explained modulation technique is proven to successfully function and balance capacitor mid-point under a capacitor mismatch, a fault resistor connected in parallel with a capacitor, a sudden change in the load, and a short-circuited capacitor. Finally, the relationship between the reference vector value and the boosting ratio is explained in this chapter which shows that the Vienna rectifier is useful only for high voltage applications. In the next chapter, the issue of high boosting ratio for the Vienna rectifier is discussed.

Chapter 7. The Vienna rectifier for low voltage applications

For relatively low voltage applications such as battery charging, the disadvantage of the Vienna rectifier is the high boost ratio. For example, in electric vehicles (EVs) the rated voltage of 120 kWh battery array is in the range of 350 V, which is lower than the minimum output voltage of Vienna rectifier when supplied from the grid. When the Vienna rectifier is connected to a 220 V grid, the minimum output voltage for the DC link is 532 V. To overcome this issue, a second stage can be added to reduce the output voltage. Conventionally, 2-stage converters are not preferable as the second stage further reduces the system overall efficiency and increases the bulkiness of the overall system [41 - 42]. Nonetheless, 2-stage converters offer better flexibility in controlling the output voltage as they allow the two converters to operate at their optimal duty cycle. Hence, the feasibility of the 2-stage configuration depends on implementing two high efficiency converters, by which the converter's overall efficiency will be comparable to the single stage configuration [43 - 44]. Therefore, in this thesis, the second stage converter is a 4-switch buck converter with two resonance tanks [45] (Figure 7.1).

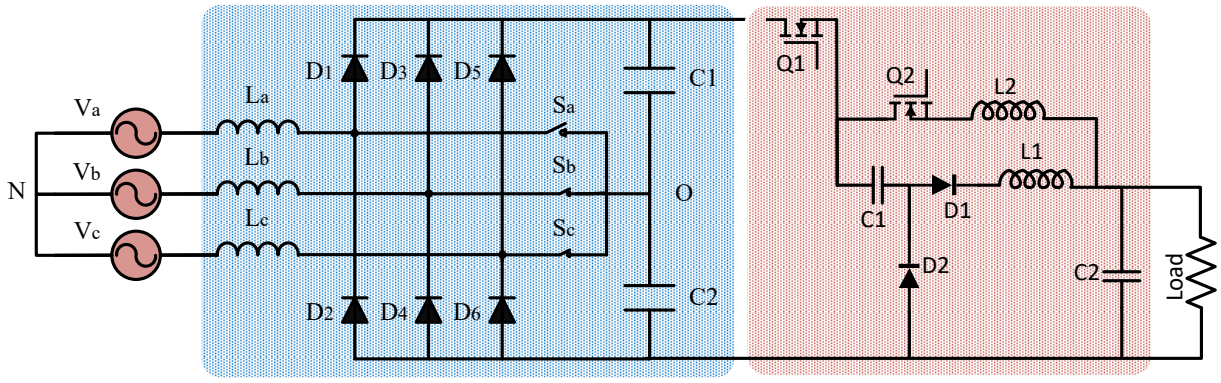

Figure 7.1: Two stages Vienna boost rectifier and 4-switch buck converter

The main advantages of such a converter are: 1) zero current switching for all four switches; and 2) all passive elements within the resonance tanks are storage-less which significantly reduces the size and weight of the converter. The reported efficiency of this converter is 99%, which eliminates the disadvantage of 2-stage converters when combined with the high efficiency Vienna rectifier. The result of this combination is very high overall efficiency with reduced component sizing.

7.1. 4-switch Buck Converter

The overall 2-stage converter is shown in Figure 7.1 The second stage (Figure 7.2) is a 4-switch buck converter [11]. The output of the Vienna rectifier is connected to its input, while the output of the second stage is connected to the load through the resonance switching circuit. Two series resonance tanks are formed, one with C1 and L1 and the other with C1 and L2. In this design, both L1 and L2 are equal. However, different values of L1 and L2 can be chosen, if desired. The converter is switched at the resonance switching frequency defined by the values of C1 and L1/L2. In this circuit, each pair Q1, D1 and Q2, D2 are operated in a complementary manner.

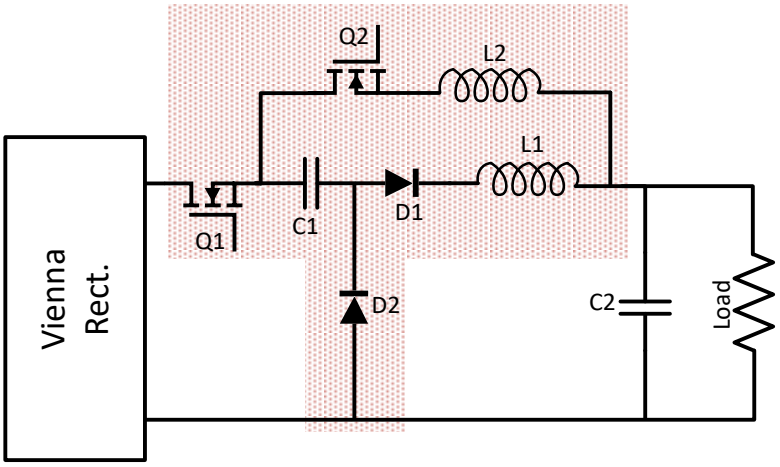

Figure 7.2: 4-switch Zero Currrent Switching (ZCS) buck converter with two series resonance tanks

When Q1 is closed, the rectified DC voltage is connected to output capacitor C2 though C1 , D1 and L1, as shown in Figure 7.3. As C1 and L1 form a series resonance tank, a sinusoidal resonance current starts to flow within the time interval $D * Ts$ (where D is the duty cycle and Ts is the total switching time), as shown in Figure 7.4 Once the current tends to reverse its direction, the rectifying diode D1 blocks the negative current, allowing for zero current switching (ZCS) of the active switch Q1.

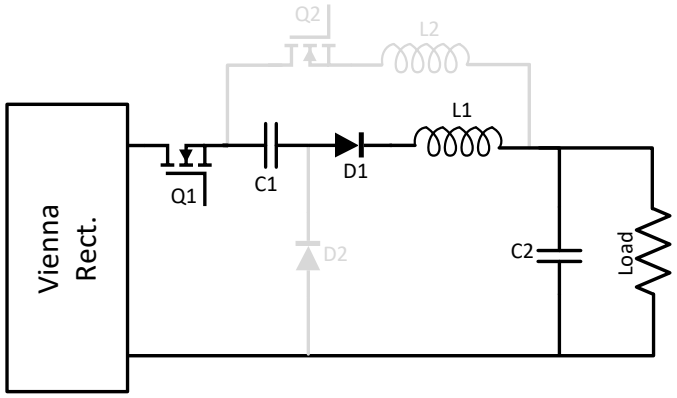

Figure 7.3: Conduction of the 4-switch converter at the first switching interval D*Ts

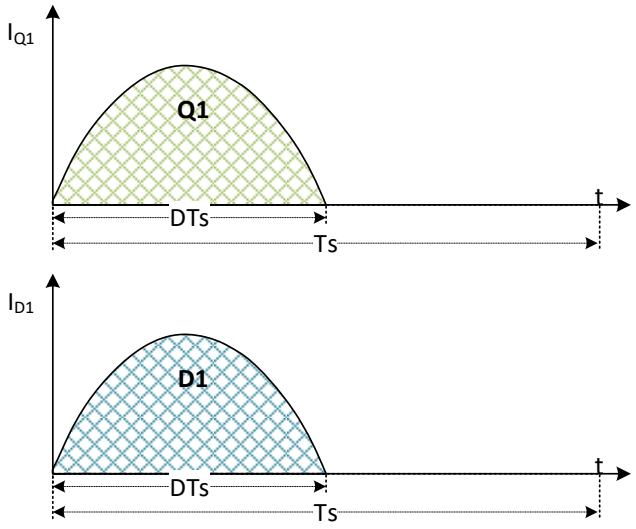

Figure 7.4: Q1 and D1 resonance current within one switching cycle Ts

For the second time interval $(1 - D)Ts$, Q2 is closed, which connects C1 to L2, thereby forming the second series resonance tank, as shown in Figure 7.5. The response current then flows from C1 to the load though L2. As depicted in Figure 7.6 and as will be explained later, by the end of this time interval, the total energy stored in the resonance tanks is transferred to the load. However, if this is not the case, the rectifying diode D2 will prevent the current from reversing its direction, which ensures ZCS of the second active switch S2. In general, each switching pair $Q1, D1$ or $Q2, D2$ form a 2-quadrant switch that is able to block voltage in two polarities and conduct the current in one direction, which facilitates the desired operation.

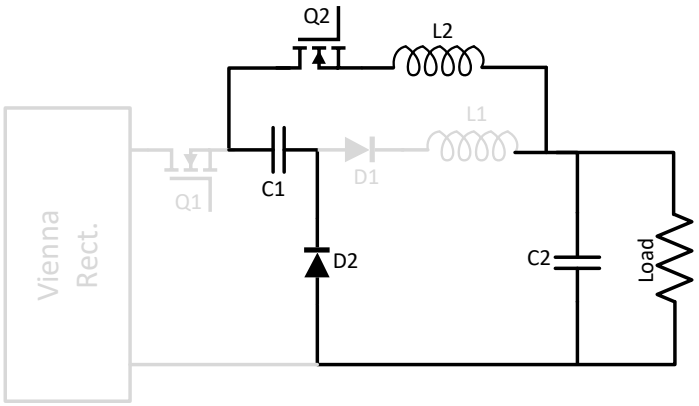

Figure 7.5: Conduction of the 4-switch converter at the second switching interval (1-D)Ts

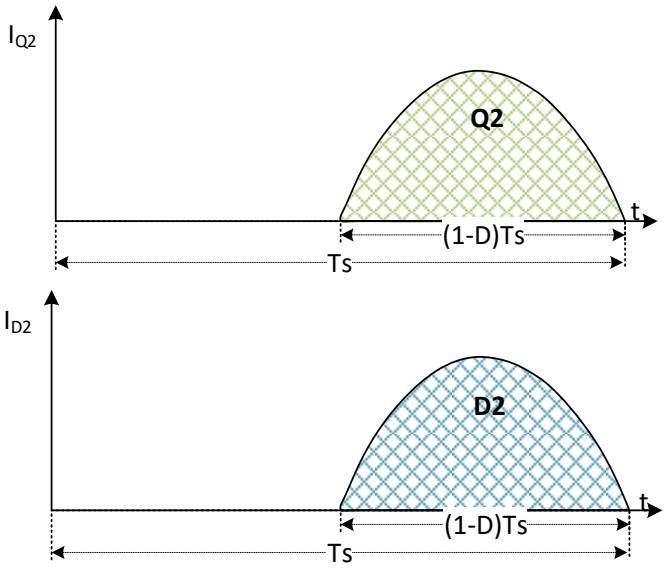

Figure 7.6: Q2 and D2 resonance current within one switching cycle Ts

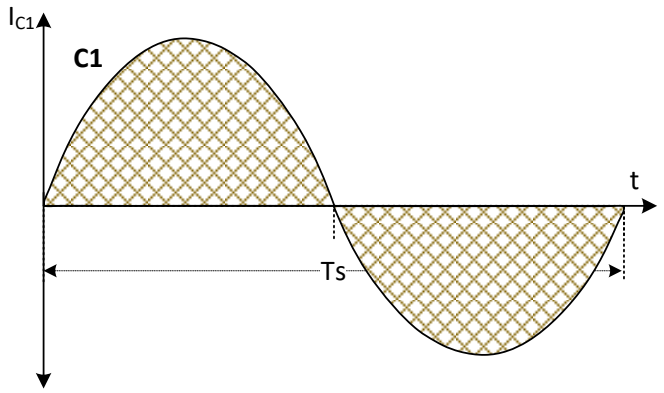

Figure 7.7: Capacitor C1 resonance current within one switching cycle Ts

As explained earlier, the operation of the converter is based on allowing the resonance current to flow within two separate branches, each of which allows the flow in one direction. Hence, ZCS for all switches can be realized. That is all done without the need for any additional control loops or zero crossing detectors.

Moreover, as shown in Figure 7.5, Figure 7.6, and Figure 7.7, the energy stored in each inductor is completely transferred to the load within one switching interval $D * Ts$ or $(1 - D)Ts$. This means that the principle of voltage-second balance is applicable within one time interval, but not with the whole switching period Ts. Thus, the inductors are storage-less, which is one of the main features of this converter. The design of the inductors is based on the desired resonance frequency and range of the duty cycle, which results in a significant reduction in their values compared to the ones in conventional converters.

As mentioned earlier, the inductor volt-second balance is applicable to each inductor within each time interval. Thus, the converter's output gain can be deduced as follow:

$$\int v_{l1} dt = V_{pn} - (V_{out} + V_{C1}) = 0 \tag{41}$$

$$\int v_{l2} dt = V_{C1} - V_{out} = 0 \tag{42}$$

From (41) and (42)

$$\int v_{l1}\,dt = V_{pn} - (V_{out} + V_{C1}) = 0 \tag{43}$$

It should be noted that, for this converter, with two active switches and two diodes, the gain of the converter is fixed at 0.5, despite the variation in the duty cycle. Furthermore, this converter, in terms of construction and operation is similar to a switched-capacitor converter. This converter is derived with a constant 0.5 duty cycle to keep its efficiency as high as possible. Variation in the duty cycle will have little impact on the output voltage, but will reduce its efficiency. However, the advantage of this converter is its ability to operate in soft switching mode within all of its four switches and its energy storage-less passive elements.

As the switching frequency of this converter is the resonance frequency of both resonance tanks, the values of the resonance components can be calculated as follow:

$$f_r = f_{sw} \tag{44}$$

$$f_r = 1/2\pi\sqrt{L_{1,2}C_1} \tag{45}$$

By choosing a value for $\mathrm{C1}$, $\mathrm{L1}$ and $\mathrm{L2}$ can be calculated, knowing that $\mathrm{L_1 = L_2 = L_{1,2}}$.

7.2. Simulation Results

A MATLAB / Simulink model is used to verify the performance of the proposed configuration. The design parameters are listed in Table 7.1. It should be noted that with respect to the designed power level and resultant PF and THD, the proposed configuration implements relatively small passive components (i.e. inductors and capacitors). Thus, the overall converter size and weight can be significantly reduced. Further reduction in the passive components can be achieved by increasing the switching frequency of both stages. It is important to note that,

for a stable operation, the switching frequency of the first stage should always be about ten times the switching frequency of the next stage.

Table 7.1: System's parameters

Parameters	Value
System's Input Voltage	220 V
Output Power	78 kW
System's Output Voltage	350 V
Mains Frequency	50 Hz
First-stage Switching Frequency	10 kHz
First-stage Inductors	0.7 mH
First-stage Capacitors	6000 uF
Second-stage Switching Frequency	1 kHz
Second-stage Resonance Inductors	0.1 mH
Second-stage Resonance Capacitor	250 uF
Second-stage Output Capacitor	5000 uF

Figure 7.8 and 7.9 depict the transient and steady state values of the 3-phase input current and the rectifier line voltage respectively. A step change in the output voltage reference from 350 V to 400 V is applied at $t = 0.3s$. In all cases, the THD of the input current is kept within 1%, which is considerably lower when compared to conventional rectifiers, as shown in Figure 7.10. The THD figure also illustrates that the fundamental component is 100% while 5^{th} harmonics is 0.6 %, 7^{th} is harmonics is 0.2%, 11^{th} harmonics is 0.1% and 13^{th} harmonics is 0.08%. Figure 7.11 shows the change in the PF, which is kept above 0.996 at all times, with near unity at steady state operation. The size of the input filter can be further reduced without increasing the input current THD above the regulation limit.

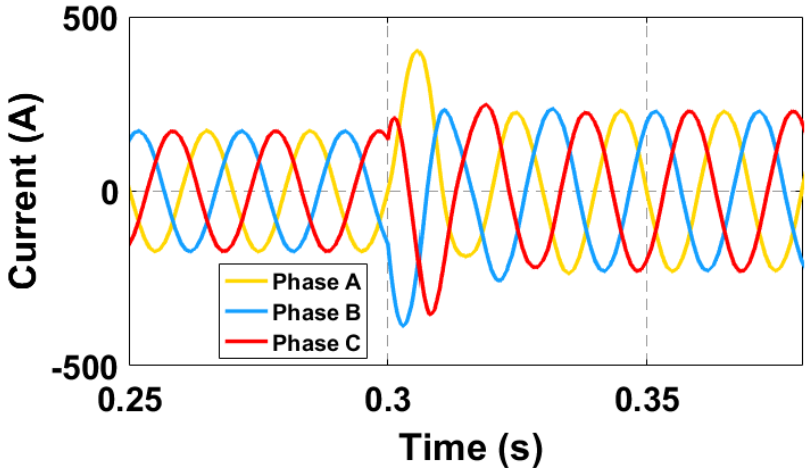

Figure 7.8: Converter's 3-phase input current

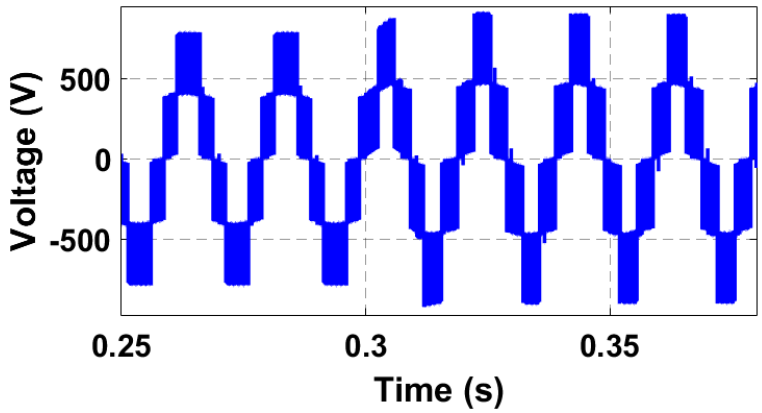

Figure 7.9: Converter's rectified multilevel voltage

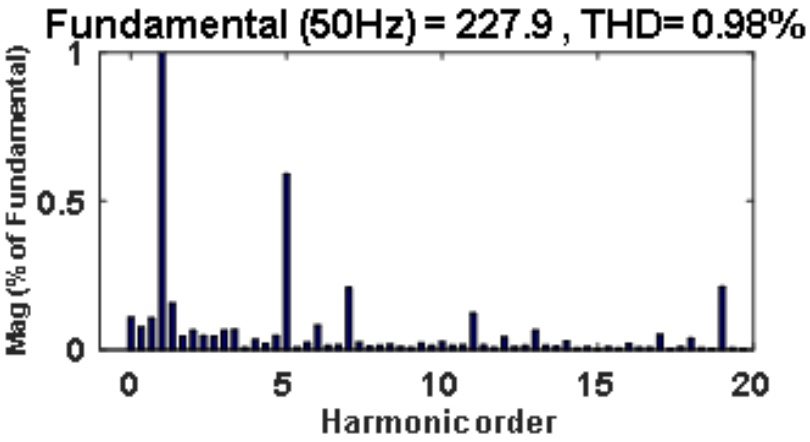

Figure 7.10: Input current THD

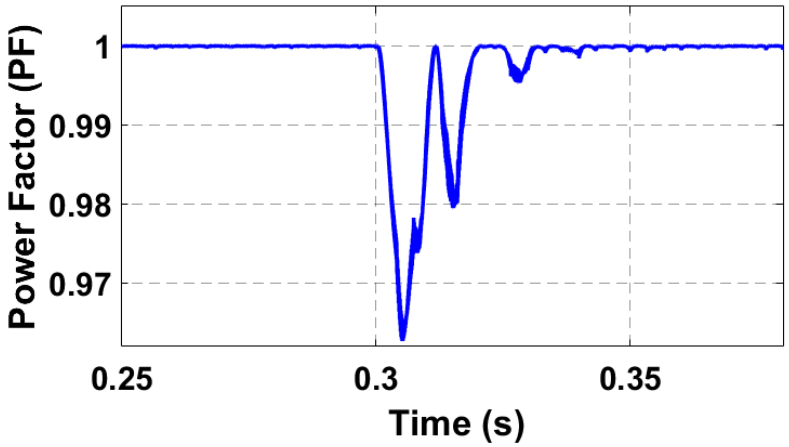

Figure 7.11: Input power factor

The output voltage of the first stage (Vienna rectifier) is depicted in Figure 7.12, which is the input of 4-switch buck converter V_{pn}. When the step change in the output voltage reference is applied at $t = 0.3s$, from 350 V to 400 V, the output voltage of Vienna rectifier follows the reference voltage firmly. Figure 7.13 depicts the response of the system's output voltage V_{out} (i.e. output voltage of the second stage four switches converter) to the applied step change. The figure shows a similar response as observed in the output voltage of the Vienna rectifier, and always reaches the desired steady state values.

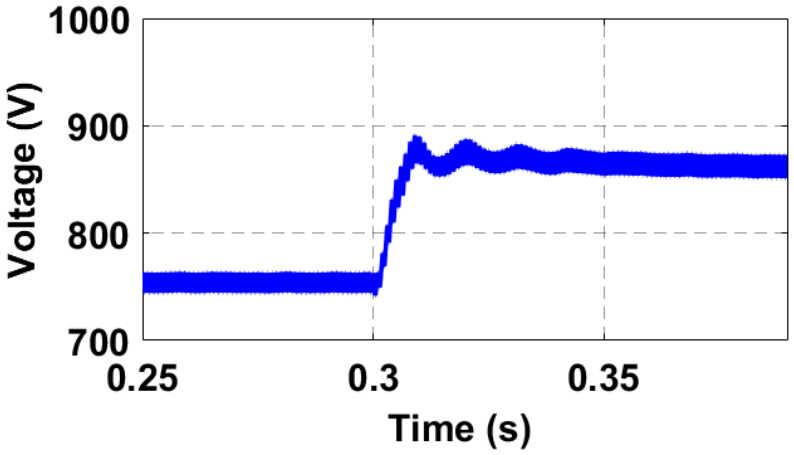

Figure 7.12: Output voltage of the Vienna rectifier(V_{pn})

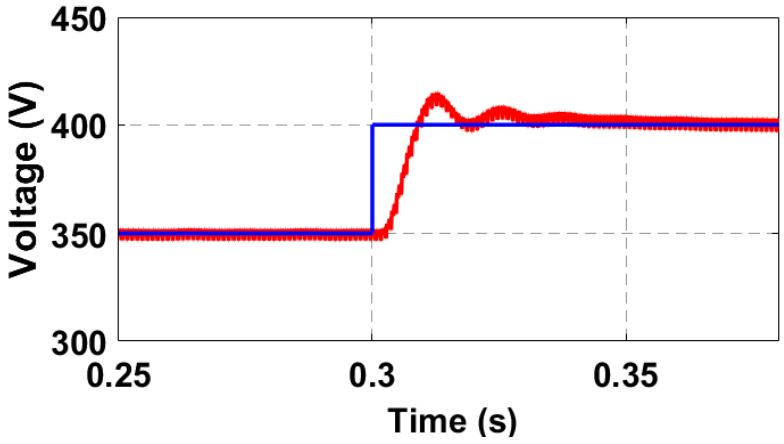

Figure 7.13: Output voltage of the second stage 4-switch converter V_{out}.

Figure 7.14 illustrates the duty cycle of the switch Q1. It shows that the duty ratio of the switch is 50%. Since the switches Q1 and Q2 are complementary, Q2 is turned ON when Q1 is OFF and vice versa. Figure 7.15 depicts the voltage and current measured in the switch Q1. The advantage of soft switching is proven, as the current starts to flow from zero through the switch after it is fully ON. It is illustrated that the current increases from zero to the peak, then returns to zero, within one switching interval (DTs). This is not only a proof of soft switch but also proves that the inductor L1 is storage-less as well. Similarly, Figure 7.16 depicts the voltage and current waveforms at the switch Q2. The soft switching is attained as ZCS, as explained for Q2. It also shows that the inductor L2 is charged and discharged fully within one interval $(1 - D)Ts$; which shows that storage-less inductor (L2) is used. Similar to Q1 and Q2, Figure 7.17 and 7.18 depict the currents and voltages measured at the rectifying diodes D1 and D2 respectively. Both figures illustrate the zero current switching during the turn ON and turn OFF intervals ($D * Ts$ and $(1 - D)Ts$).

It can be seen that, the Vienna rectifier is able to maintain high PF and low THD at all time. While, four switches buck converter maintains ZCS within all of is four switches and

storage-less operation which enables high efficiency power conversion and reduced passive components values.

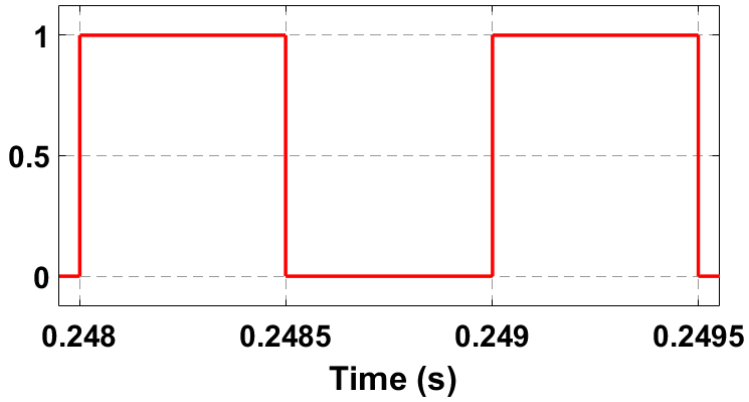

Figure 7.14: Applied duty cycle at Q1

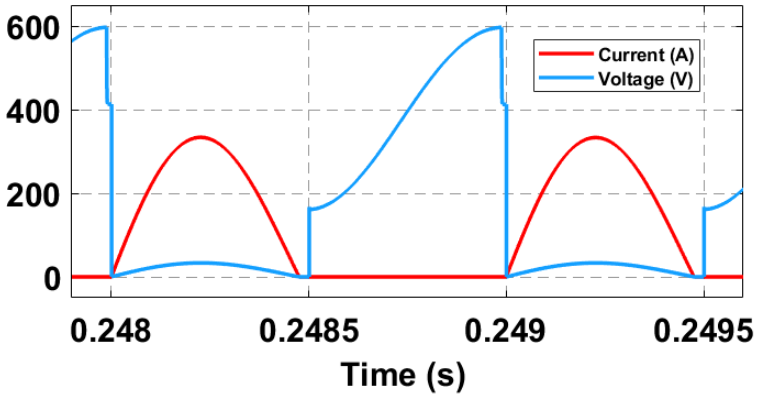

Figure 7.15: Voltage (V) in blue across $Q1$ and its current (A) in red

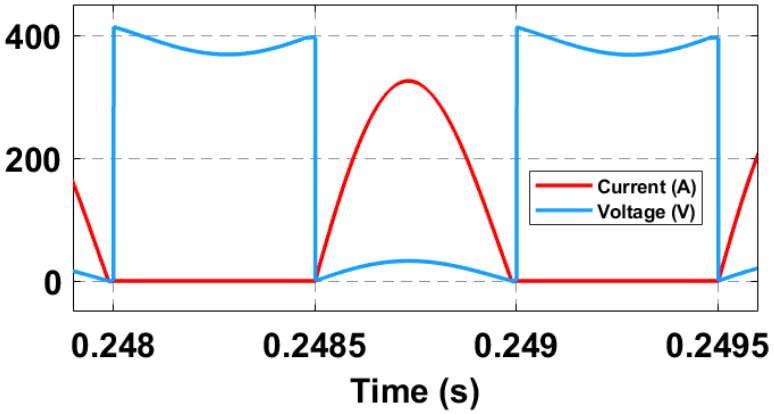

Figure 7.16: Voltage (V) in blue across $Q2$ and its current (A) in red

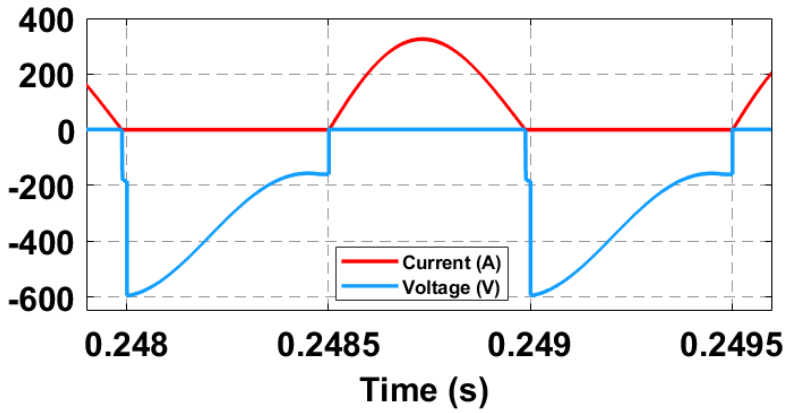

Figure 7.17: Voltage (V) in blue across $D1$ and its current (A) in red

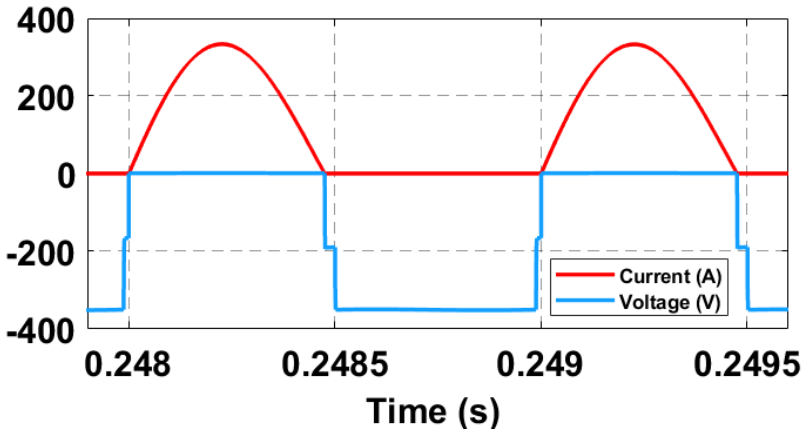

Figure 7.18: Voltage (V) in blue across $D2$ and its current (A) in red

In conclusion, 2-stage boost-buck PFC converter is introduced in this chapter. The first stage is based on the Vienna rectifier which, as proven by the simulation result, is capable to supply high power at high PF above 0.96 and low THD (less than 1%). However, its output voltage is relatively high if applications such as EV battery charger are considered. Therefore, a second stage 4-switch buck converter is cascaded with the Vienna rectifier. It has the advantage of using storage-less passive components. Hence, their sizing can be significantly reduced when compared to other types of converters. Moreover, its efficiency is very high due to its ability to operate in ZCS within all of its switches, which reduces the losses and the

required heatsinks as well. It has been seen that although single stage PFC are more attractive due to its lower components count and higher efficiency. The proposed two stages configuration can perform similarly while reserving the flexibility of regulating the output power and maintain high PF and low THD over a wide range of operation.

Chapter 8. Experimental Validation

In order to validate the simulation results of the simplified SVPWM, a 2.4 kW prototype for the Vienna rectifier is employed. This chapter discusses the hardware implementation and experimental results for the Vienna rectifier using the simplified SVPWM technique.

8.1. Breakdown of the Prototype:

8.1.1. Vienna Rectifier Power Stage:

As shown in Figure 8.1, Texas Instrument's Vienna rectifier prototype (TIDM-100) is used in this thesis. The power rating for this prototype is 2.4 kW. It accepts a universal 3-phase input voltage (110 – 220 AC voltage). In case the prototype is fed by 110 AC voltage, the output produces an output DC voltage of 600 V and 1.2 kW power. On the other hand, 2.4 kW power and 700 V DC voltage are produced when 220 AC voltage is fed to the prototype. The MOSFETs used in the prototype are manufactured by Infineon Technology and have ratings of 700V and 13 A. On the other hand, Schottky diodes, which are manufactured by Cree, are used. These diodes have ratings of 1200 V and 8 A. Aluminum Electrolytic Capacitors with rating of 450 V are employed for the output DC bus. These capacitors are manufactured by TDK while the input boost inductors are manufactured by Vitec Corporation. The component details are shown in Table 8.1

Table 8.1: Details of the prototype's components

	Quantity	Value/Type	Manufacturer	Ratings	Part Number
MOSFETs	6	- /N-CH	Infineon Technology	700V, 13 A	IPP65R190C7FKSA1
Diodes	6	- /Schottky	Cree	1200 V, 8 A	C4D08120A
Inductors	3	3mH / -	Vitec Corporation	-	53PR116-292
Capacitors	4	Aluminum Electrolytic /220uF	TDK	450 V	B43504C5227M

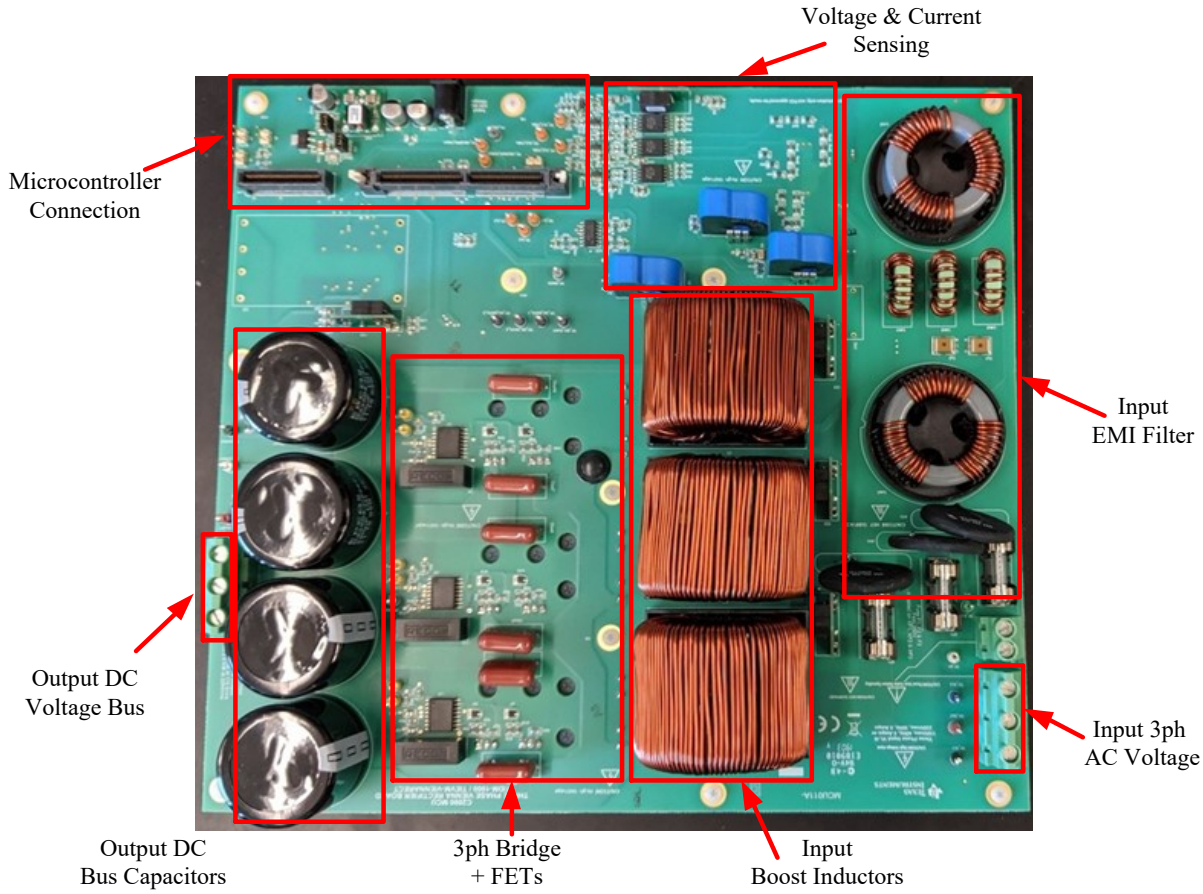

Figure 8.1: Texas Instruments Vienna rectifier Kit (TIDM-100)

For safety purposes, protection fuses are added and the power level is reduced to 600 W by using 12 series 50 W resistors as shown in Figure 8.2.

$$50\Omega * 12 = 600\ \Omega \tag{46}$$

Since the voltage of the DC link is 600 VDC at 110 VAC:

$$\text{Power} = \frac{V^2}{R} = \frac{600^2}{600} = 600\ \text{W} \tag{47}$$

Figure 8.2: Prototype's load

Table 8.2: Prototype's parameters

Parameters	Value
Input Voltage	110 - 220 V
Output Power	1.2 - 2.4 kW
Output Voltage	600 - 700V
Mains Frequency	60 Hz
Switching Frequency	50 kHz
Inductor filters	3 mH
Capacitor filters	180 uF

8.1.2. Control Card:

The power stage can be controlled and monitored using any C2000™ family microcontroller (MCU). As illustrated in Figure 8.3, the microcontroller used in this prototype is C2000™ F28379D.

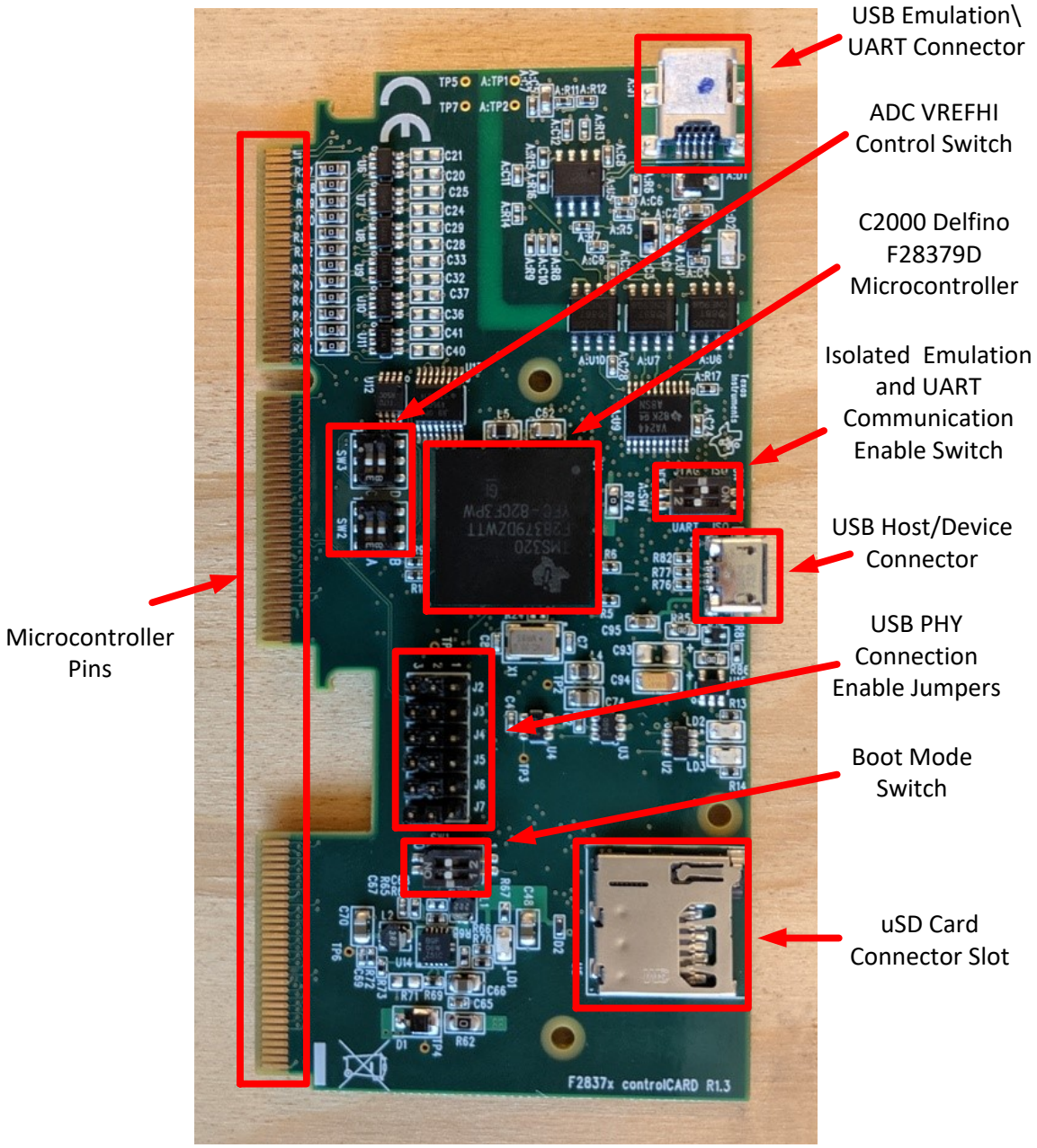

Figure 8.3: $C2000^{TM}$ F28379D microcontroller (MCU)

Figure 8.4 depicts connections to the MCU pins. Table 8.3 illustrates the microcontroller's key connectors and their function.

Table 8.3: MCU key connections and their function

Name of the Signal	PIN Number	Function
PWM 1-A	49	PWM for Ph_{1A}
PWM 1-B	51	PWM for Ph_{1B}
PWM 2-A	53	PWM for Ph_{2A}
PWM 2-B	55	PWM for Ph_{2B}
PWM 3-A	50	PWM for Ph_{3A}
PWM 3-B	52	PWM for Ph_{3B}
I_{L1}	15, 20	Inductor Current Measurement Ph_1
I_{L2}	21, 27	Inductor Current Measurement Ph_2
I_{L3}	25	Inductor Current Measurement Ph_3
V_1	18	AC Voltage Sensing Ph_1
V_2	28	AC Voltage Sensing Ph_2
V_3	34	AC Voltage Sensing Ph_3
V_{bus_PM}	31, 24	DC Voltage from Positive to Midpoint
V_{bus_MN}	37, 26	DC Voltage from Midpoint to Negative

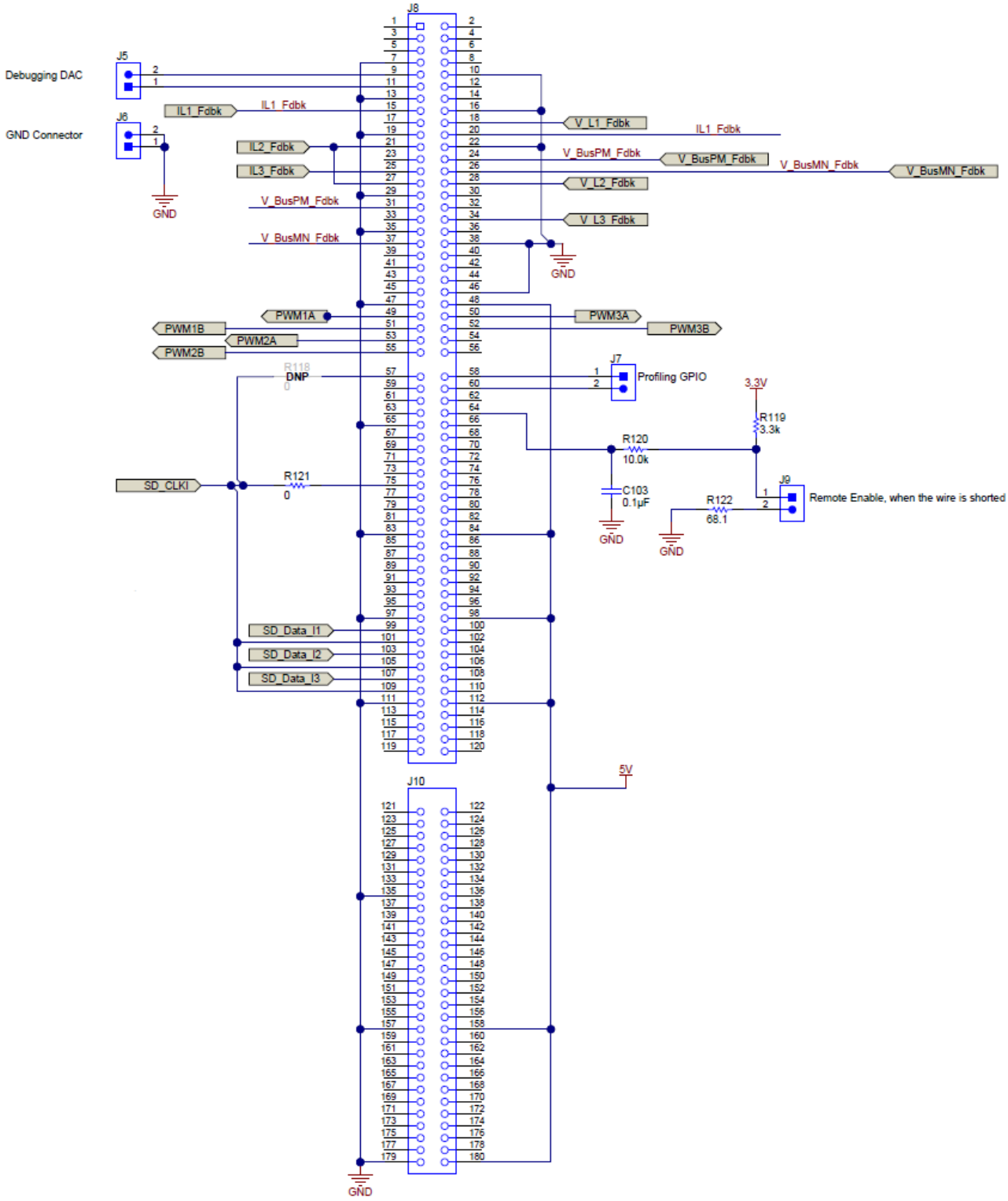

Figure 8.4: Schematic of $C2000^{TM}$ F28379D microcontroller (MCU)

8.3. Experimental Results:

The experimental results are shown in Figures 8.5 to 8.12. Figure 8.5 depicts the switching signal applied to the switch (Sa) (dark blue), phase A voltage (pink), and the current injected in phase A (light blue). This figure illustrates the unity PF as the voltage and current are in phase. In addition, the controller along with the simplified SVPWM technique succeed to draw a sinusoidal input current. The scaling for the current signal is 5 A/div while the scale for phase A voltage is 100 V/div. Finally, the scale is 5 V/div for the switching signal.

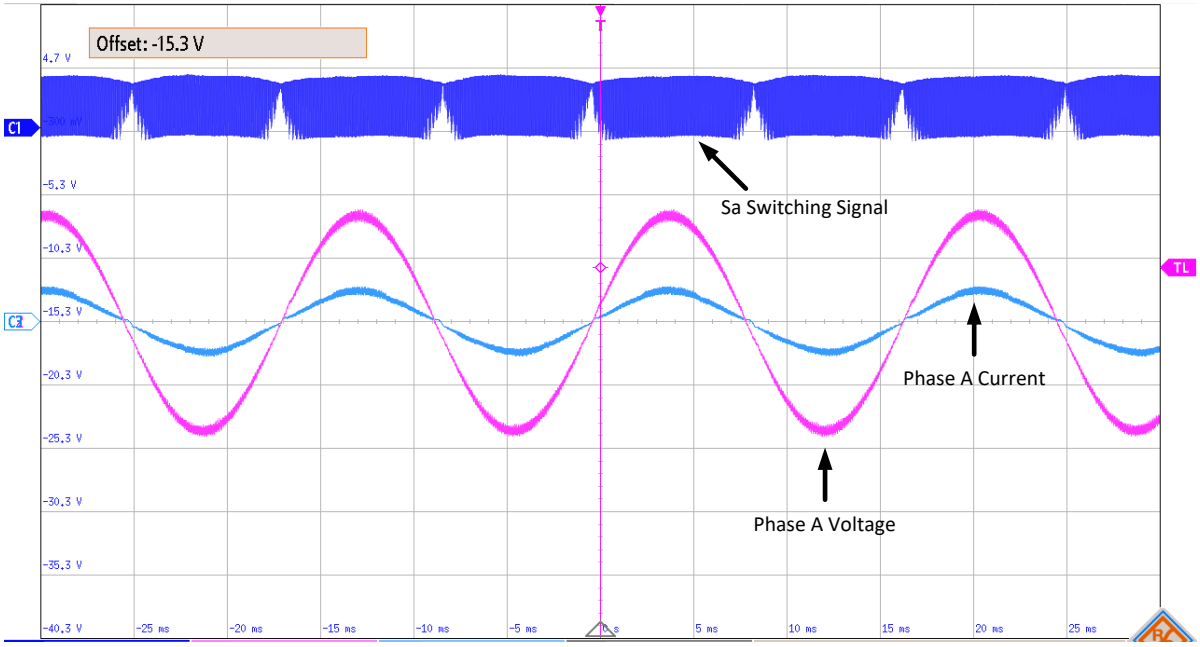

Figure 8.5: Experimental results for current and voltage in phase A and the switching signal to switch A

Figure 8.6 illustrates the well-balanced three phase currents along with the phase A voltage (pink). This figure shows a similar result as illustrated in Figure 6.2 in the simulation results. It is also illustrated that the system provides a balanced 3-phase input currents with low

THD. The scale in this figure is equal to 50 V/div for the voltage signal while it is 5 A/div for the input currents.

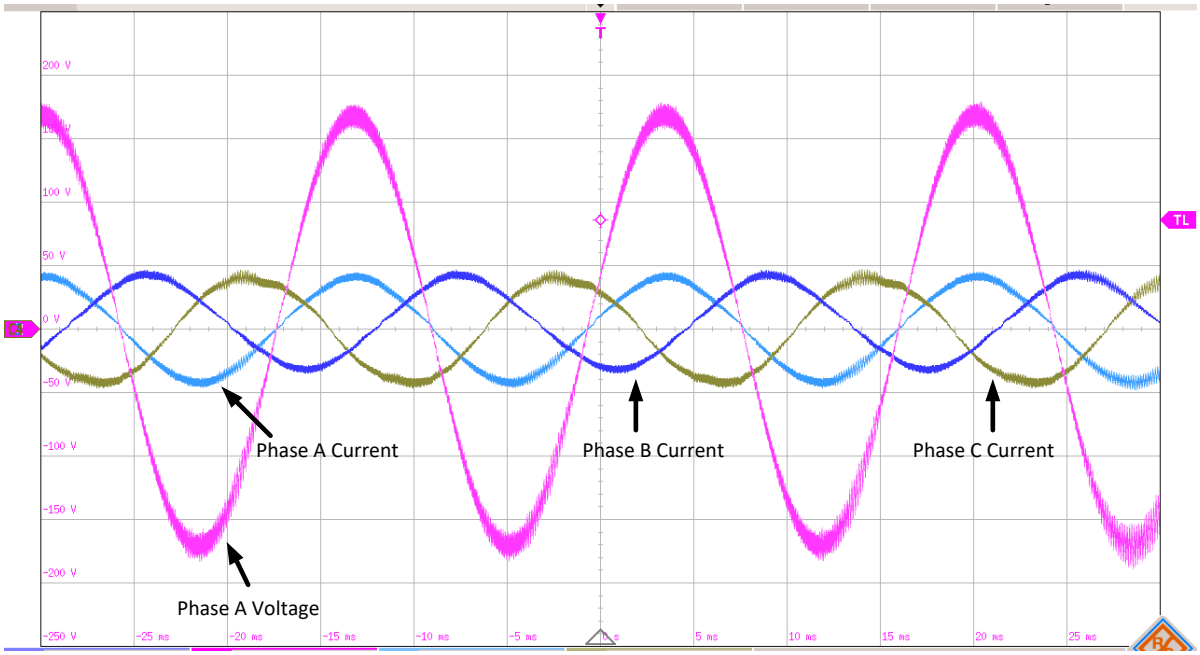

Figure 8.6: Experimental results for the three phase currents and phase A voltage

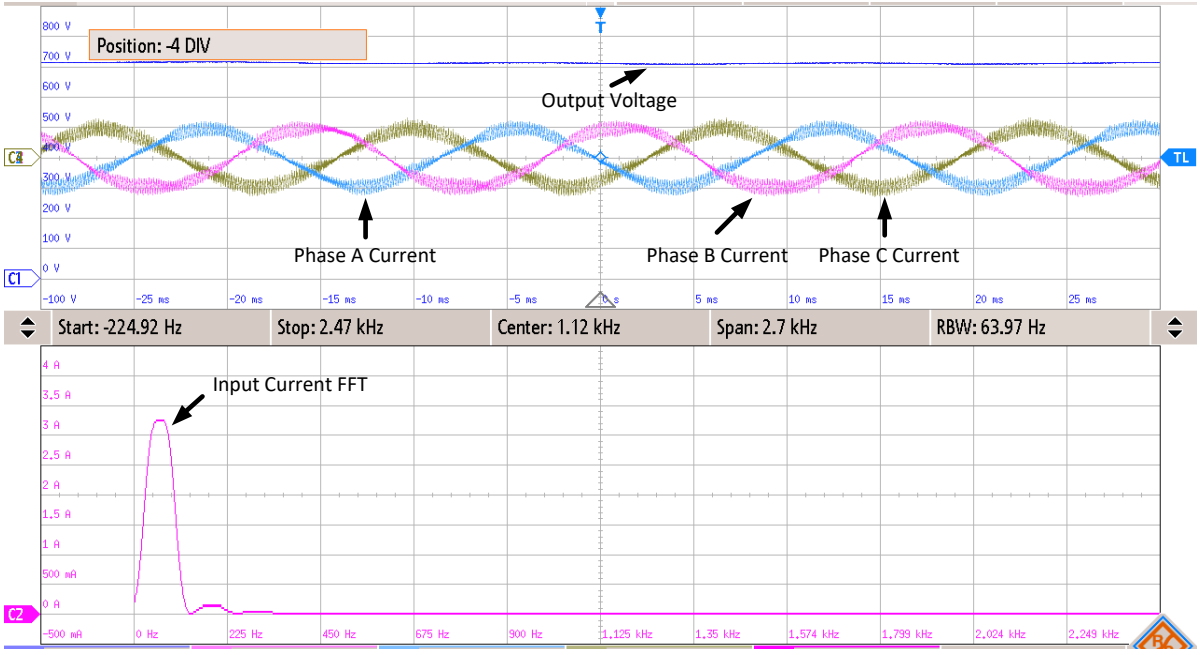

Figure 8.7: Experimental results for the three phase currents, output DC voltage and the Fast Fourier Transformation (FFT) of the input current

Figure 8.7 is divided into two parts. The upper part shows the dc-link voltage (blue) and the three phase input currents. Each division is equal to 100 V for the DC voltage while it is equal to 5 A for the input current. The lower part of the figure depicts the Fast Fourier Transformation (FFT) of the input current and illustrates the low THD attained as the fundamental component is high and the other components are negligible.

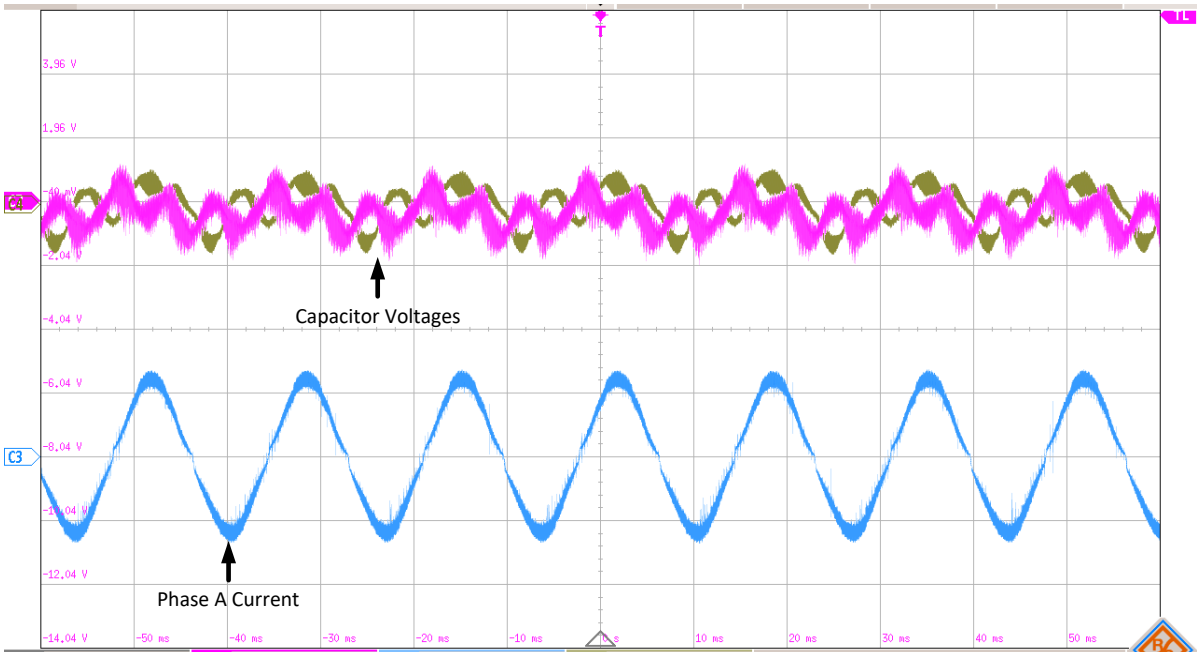

Figure 8.8: Experimental results for current in phase A (lower signal) and capacitor voltages (upper signals)

Figure 8.8 depicts the capacitor voltages (pink and gray). Additionally, phase A current is shown in blue. It is illustrated that the two capacitor voltages are overlapped, similar to Figure 6.5 in the simulation results, which shows the validity of the capacitor balancing method. The scale is 2 V/div for the capacitor voltages signals and 2 A/div for the input current signals.

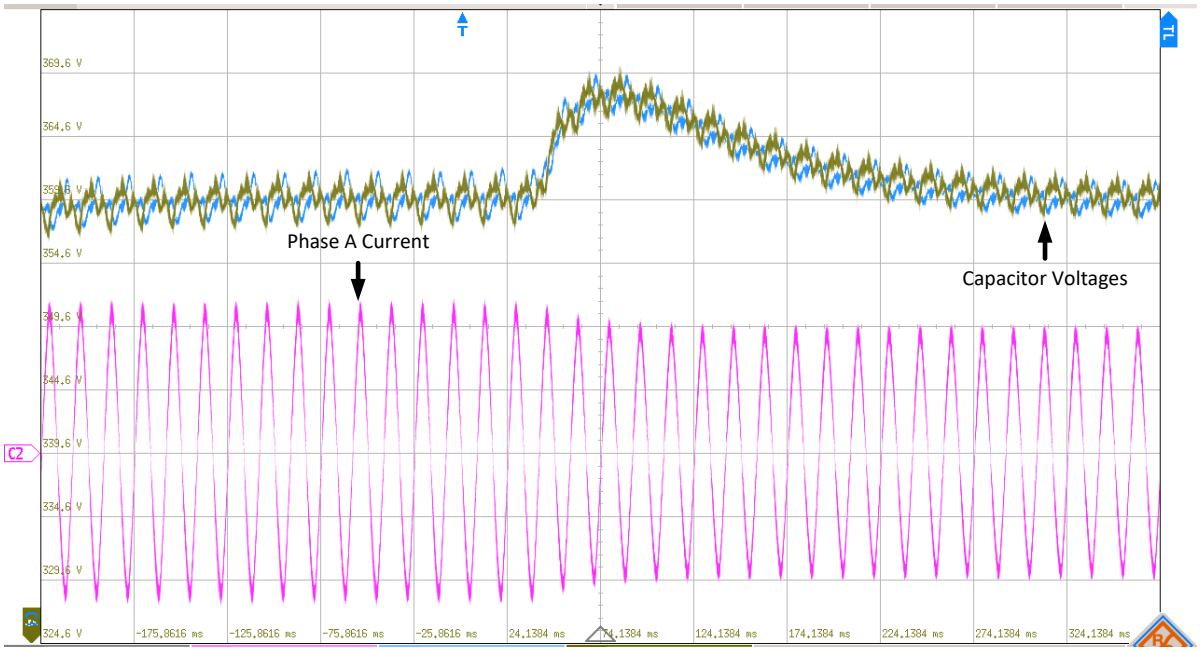

Figure 8.9: Experimental results for capacitor voltages (upper signals) and phase A current (lower signal) in the test case of a load step change

Figures 8.9 depicts the response of the capacitor voltages and the current injected in phase A when the load resistance is changed from 500 to 600 Ω (17%). The result in this figure shows a similar response as illustrated in both Figure 6.19 and Figure 6.21 in the simulation results. It is illustrated that the capacitor balancing method is robust as the capacitor voltages are balanced even during the transient response. It is shown in the figure that the rise time of the capacitor voltages is 30 ms while the settle time is 200 ms. The scale/division for the current in both figures is 2 A/div while it is 5 V/div for capacitor voltages in Figure 8.9.

Figure 8.10 depicts the experimental result of capacitor mismatch test where a 470 uF capacitor is connected in parallel to capacitor C1, which increases the total capacitance in C1. This test is performed to check the robustness of the capacitor balancing technique in the simplified SVPWM. The figure illustrates that the capacitor voltages are well-balanced even when the capacitors are mismatched. It also is illustrated that the voltage across the upper capacitance (dark green) has smaller ripple as compared to the voltage across C2 (blue). This

is reasonable as C2 has a smaller capacitance than C1. The figure also shows that a pure current is flowing in phase A (pink). The scale of this figure is 10V/div for the capacitor voltages while it is 2A/div for the current.

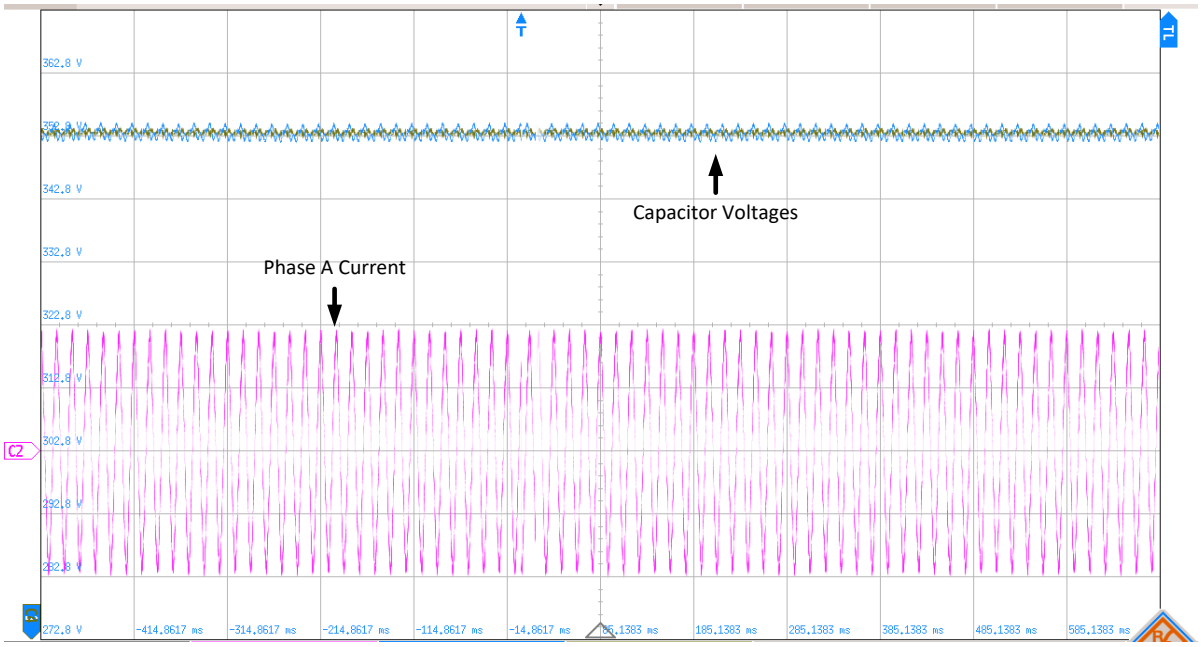

Figure 8.10: Experimental results for capacitor voltages (upper signals) and phase A current (lower signal) in the test case of the capacitor mismatch

Figure 8.11 depicts the result of a 17% load step change test (from 500 to 600 Ω) in the capacitor mismatched condition. It is illustrated that the balancing technique is able to successfully balance the capacitor voltages (dark green and blue). It is shown in the figure that the rise time of the capacitor voltages is 40 ms while the settle time is 250 ms. The input current (pink) is reduced as the load is increased to 600 Ω. The capacitor voltages in this figure has a scale of 5V/div while the scale for the current is 2A/div.

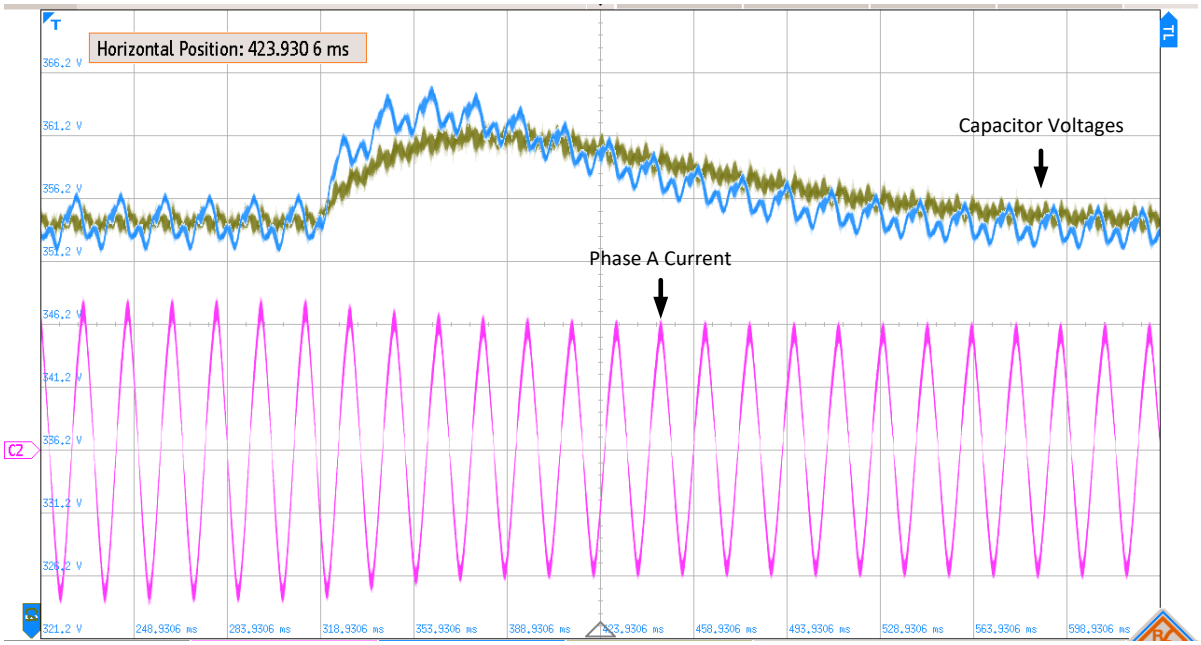

Figure 8.11: Experimental results for capacitor voltages (upper signals) and phase A current (lower signal) in the test case of the capacitor mismatch with load step change

The final test to check the robustness of the introduced modulation technique is connecting a 600 Ω fault resistor in parallel to capacitor C1 (dark green). Figure 8.12 depicts the response of the capacitor voltages when connecting the fault resistor. It is illustrated that rectifier draws sinusoidal current (pink) and the capacitors voltages (dark green and blue) are well-balanced even when one of the capacitors draws a larger amount of current. The figure illustrates that the rise time for the capacitor voltages C1 and C2 is 30 ms and 80ms respectively, while the settle time is 250 and 370 respectively. The scale for the capacitor voltages is 5V/div while it is 2A/div for the current.

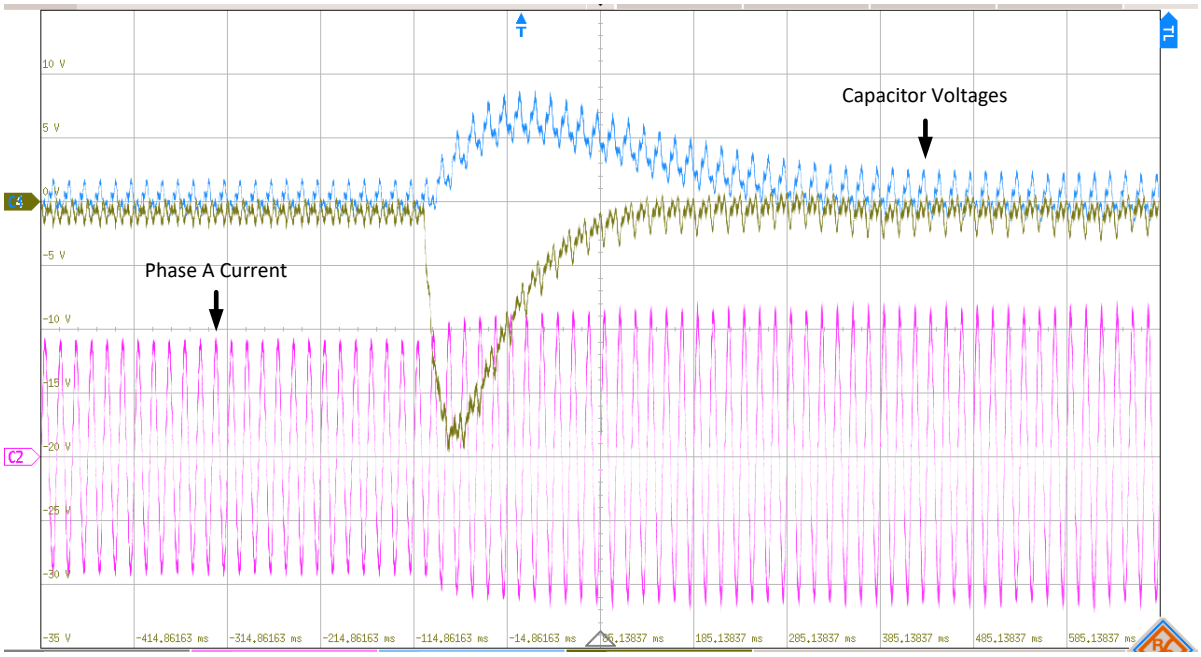

Figure 8.12: Experimental results for capacitor voltages (upper signals) and phase A current (lower signal) in the test case of the parallel fault resistor connected to capacitor C1

The results illustrated in Figures 8.4 to 8.12 verify the validity and robustness of the introduced simplified modulation technique as the unity PF and low input current THD are attained. Moreover, the capacitor voltages are well-balanced even under fault conditions and a regulated output voltage is achieved.

Chapter 9. Conclusion and Recommendations

9.1. Summary:

The remarks obtained by this study can be summarized as follows:

- The Vienna rectifier provides a significantly low THD with only three active switches.
- The Vienna rectifier is a PFC rectifier that maintains the main's voltage and current in phase (unity PF) to increase the active power.
- The PF in the Vienna rectifier is maintained almost unity even under extreme fault conditions.
- The Vienna rectifier requires a very small inductance filter which leads reduction in the rectifier's size.
- The problematic of the complexity and the computational burden of the 3-level SVPWM technique can be solved by employing the introduced simplified SVPWM technique.
- Applying SVPWM for the Vienna rectifier differs from the conventional converters since the active switches do not directly control the applied voltage level.
- Using SVPWM for the Vienna rectifier increases the capacitors balancing capability.
- The simplified SVPWM method is capable of handling extreme fault conditions, such as unbalanced capacitor voltage, capacitor mismatch, capacitor short-circuited and load step change.
- The maximum boost ratio gained by the Vienna rectifier is 6.3* V_{phase} while the minimum boost ratio is 2.4*V_{phase}
- The Vienna rectifier provides a high boost ratio, which can be a disadvantage for some applications.

- The disadvantage of high boosting ratio is overcome by adding a high efficiency, soft-switched and storage-less 4-switch buck converter to the Vienna rectifier's output.
- The integration of the 4-switch converter and the Vienna rectifier provides a highly efficient system with small filters that can be used for low voltage applications.
- The simplified SVPWM method is verified by the experimental results.
- The experimental results illustrates that the simplified SVPWM is successfully functioning even under fault conditions.

9.2. Future Work:

- Increasing the voltage levels of the Vienna rectifier to improve the THD and reduce the inductor size.
- Employing techniques to reduce the DC-link's capacitor size such as adding an axillary circuit to support the capacitors in their discharging mode.
- Improving the efficiency of the Vienna rectifier by employing soft-switching techniques for the switches.
- Investigating the application of the Vienna rectifier on wind energy application to fix the variable frequency by converting AC to DC, then DC to AC.
- A hardware implementation of the boost-buck system proposed in Chapter 7 to verify the simulation results.
- Employing method to improve the zero-crossing current distortion for the Vienna rectifier.

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APPENDICES

Appendix A: Inductance and Capacitance Design

$$L = \frac{\frac{V_{dc}}{2}}{4 * fsw * \Delta i_{ppmax}}$$

$$C = \frac{Pac}{12 * f * (V^2 - (V - \Delta V)^2)}$$

Appendix B: MATLAB/Simulink Blocks

The overall schematic of the MATLAB/Simulink implementation is shown in Figure B.1. This Figure illustrates the Vienna rectifier circuits, the control and modulation blocks.

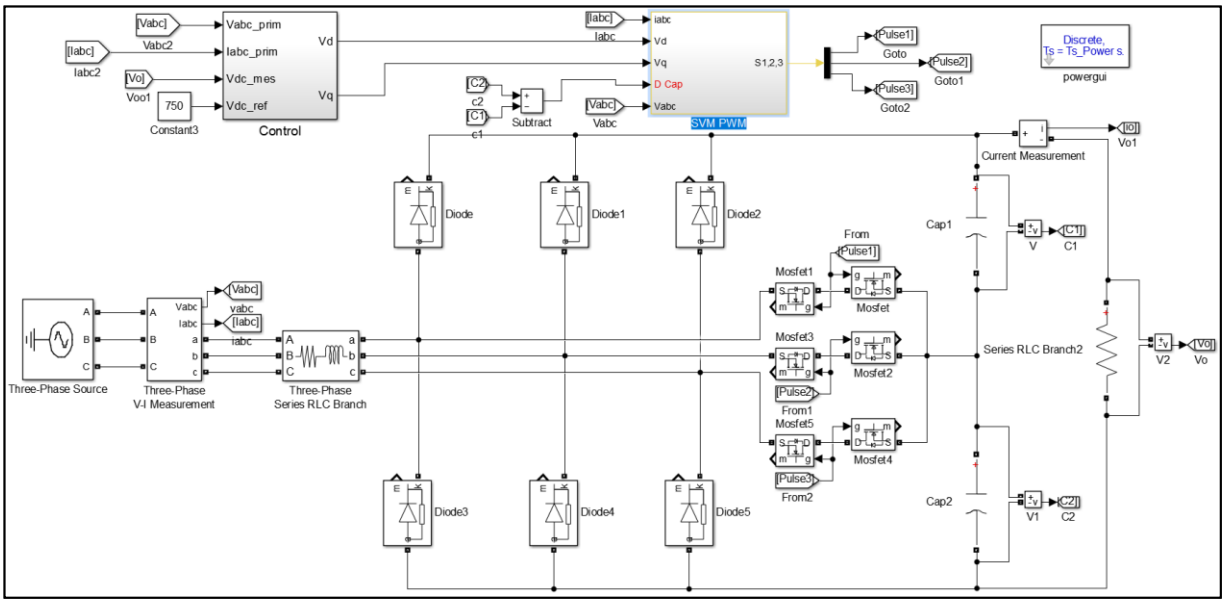

Figure 0.1: Schematic of the overall system

Figure B.2 depicts the Space Vector Pulse Width Modulation (SVPWM) block consisting of the following sub-blocks:

1. Sector Identification block.
2. Angle Normalization block.
3. Sub-vectors Calculations block
4. Shortening Sub-vectors block
5. Pulse Generation block
6. Capacitor Voltage Balancing block.

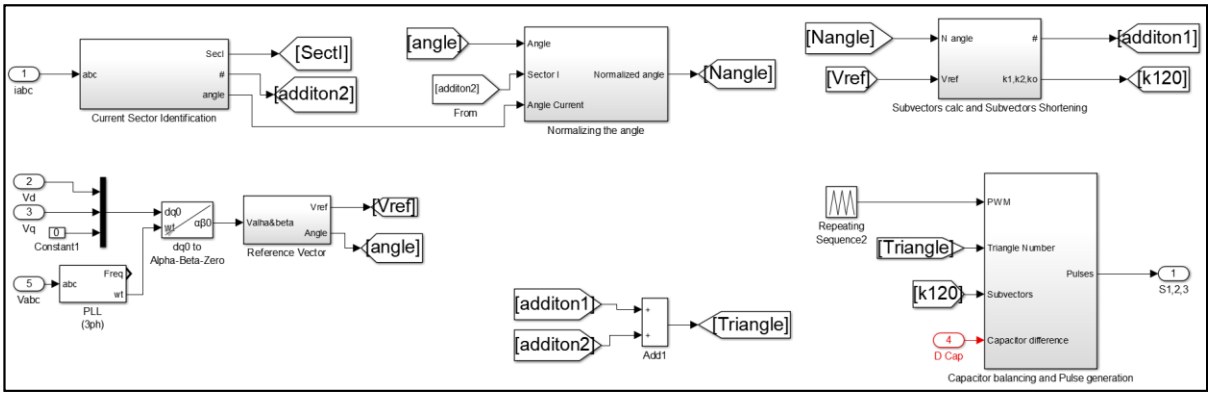

Figure 0.2: SVPWM block

Figure B.3 illustrates the details of Sector Identification block. The input of the block is the 3-phase input current. The block uses simple comparators to identify the sectors (from 1 to 6)

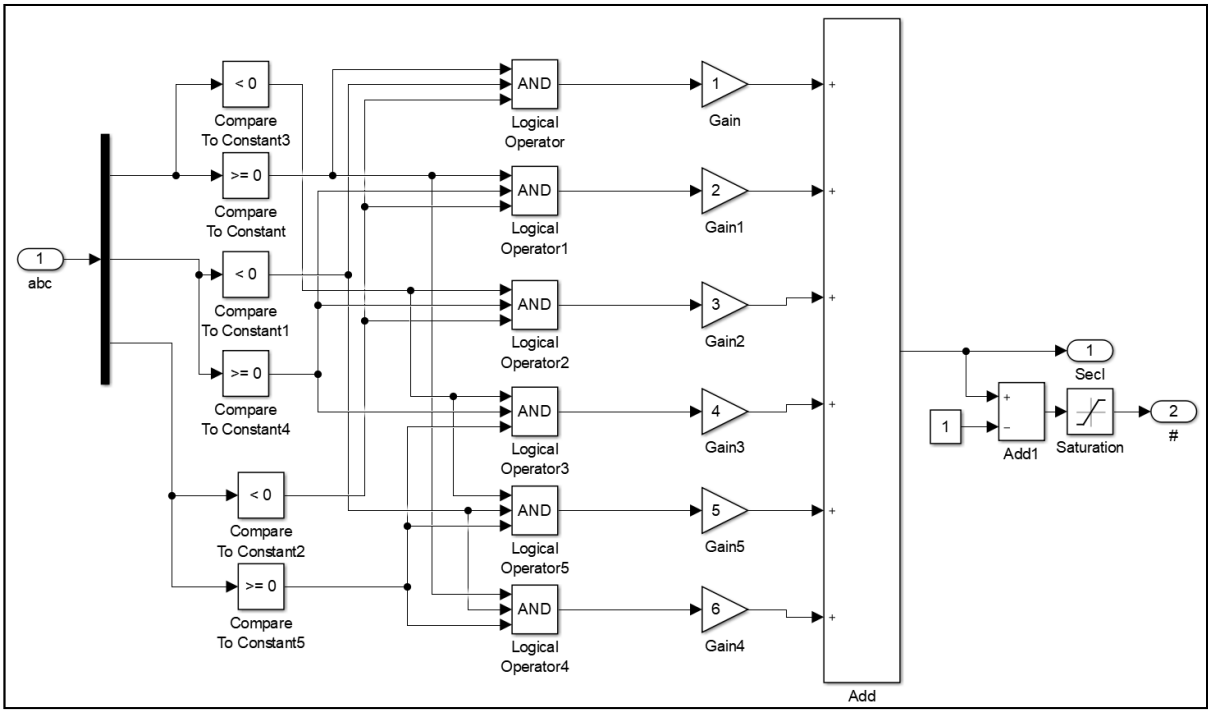

Figure 0.3: Current Sector Identification block

Figure B.4 shows the Angle Normalization block. The input of the block is an angle between + π to – π while the output is normalized to be ideally between -30 to 30 degree.

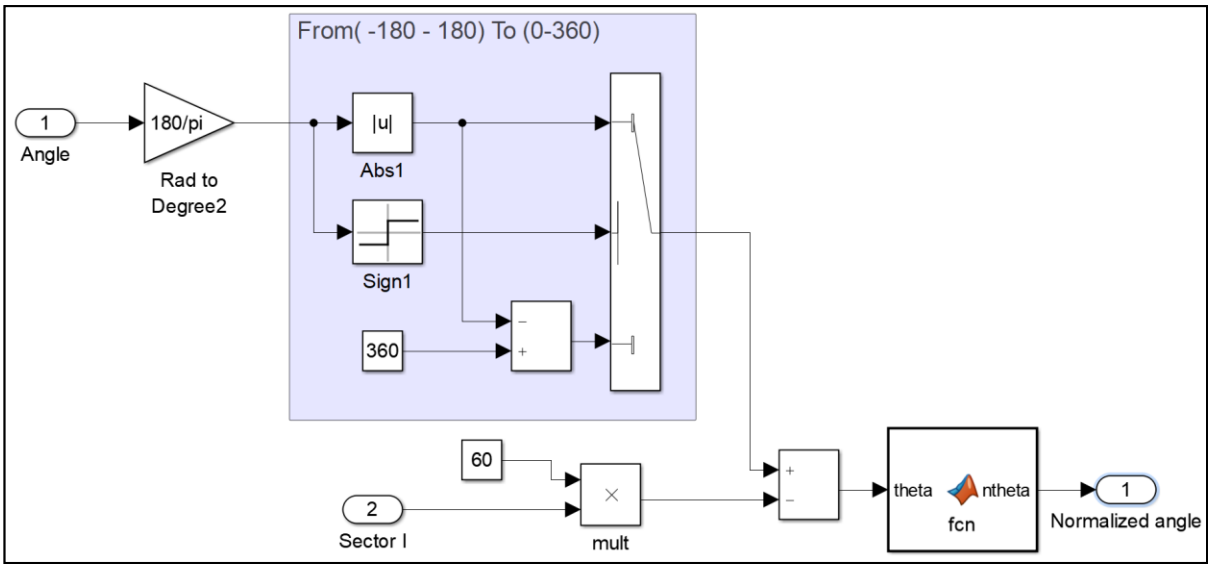

Figure 0.4: Normalizing Angle block

Figure B.5 depicts the block that contains both sub-vector calculations and sub-vector shortening. In this block, the sub-vectors are calculated, and checked whether they exceed the boundary of the hexagon or not. In case the boundary of the hexagon is exceeded, shortening will be applied.

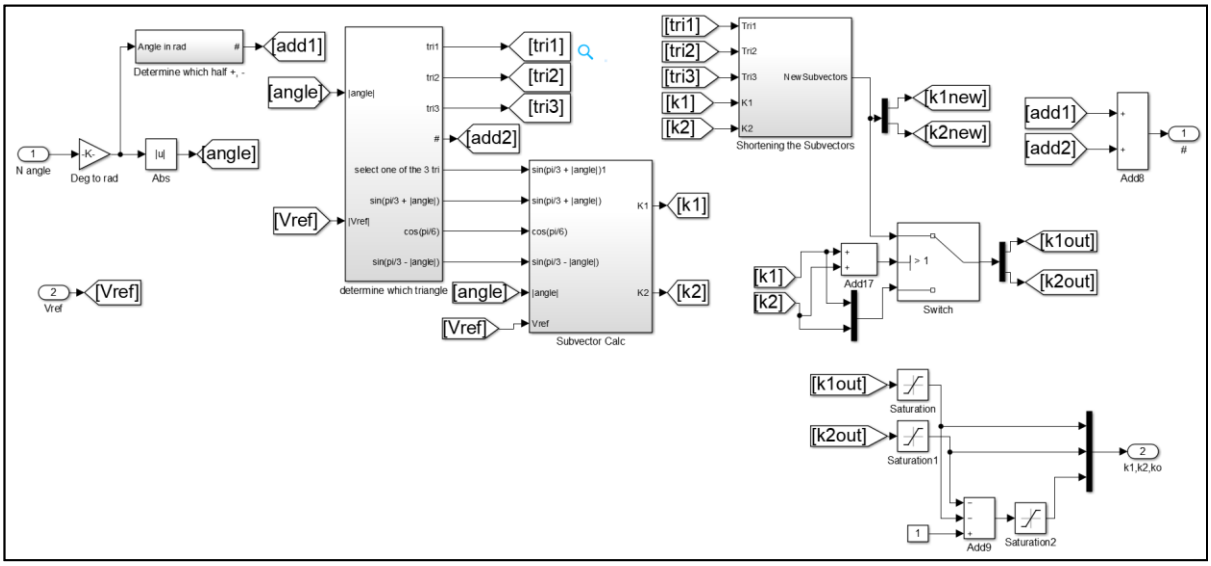

Figure 0.5: Sub-vectors Calculation and Shortening block

Figure B.6 depicts the block which performs both functions of pulse generation and capacitor voltage balancing.

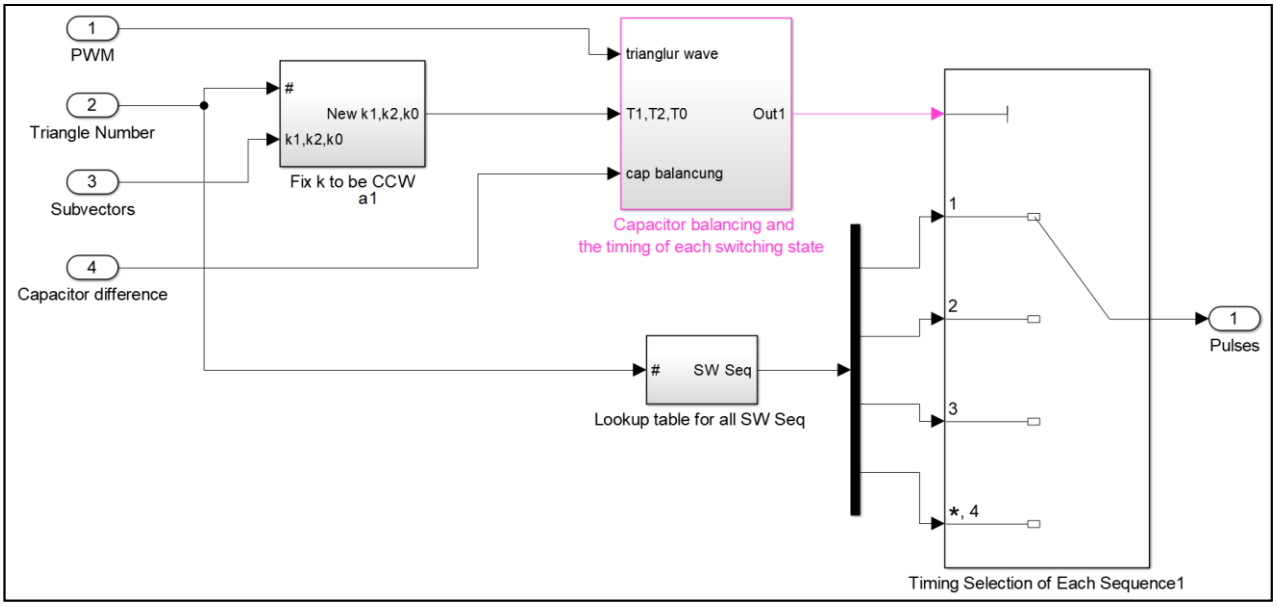

Figure 0.6: Capacitor Balancing and Pulse Generation block

Figure B.7 illustrates procedure of both capacitor balancing and switching states timing. As shown in the figure, there are four different timing that corresponds to four different switching states. These switching states are the two redundant states (Vo1 and Vo2) and the other two adjacent states (V1, V2).

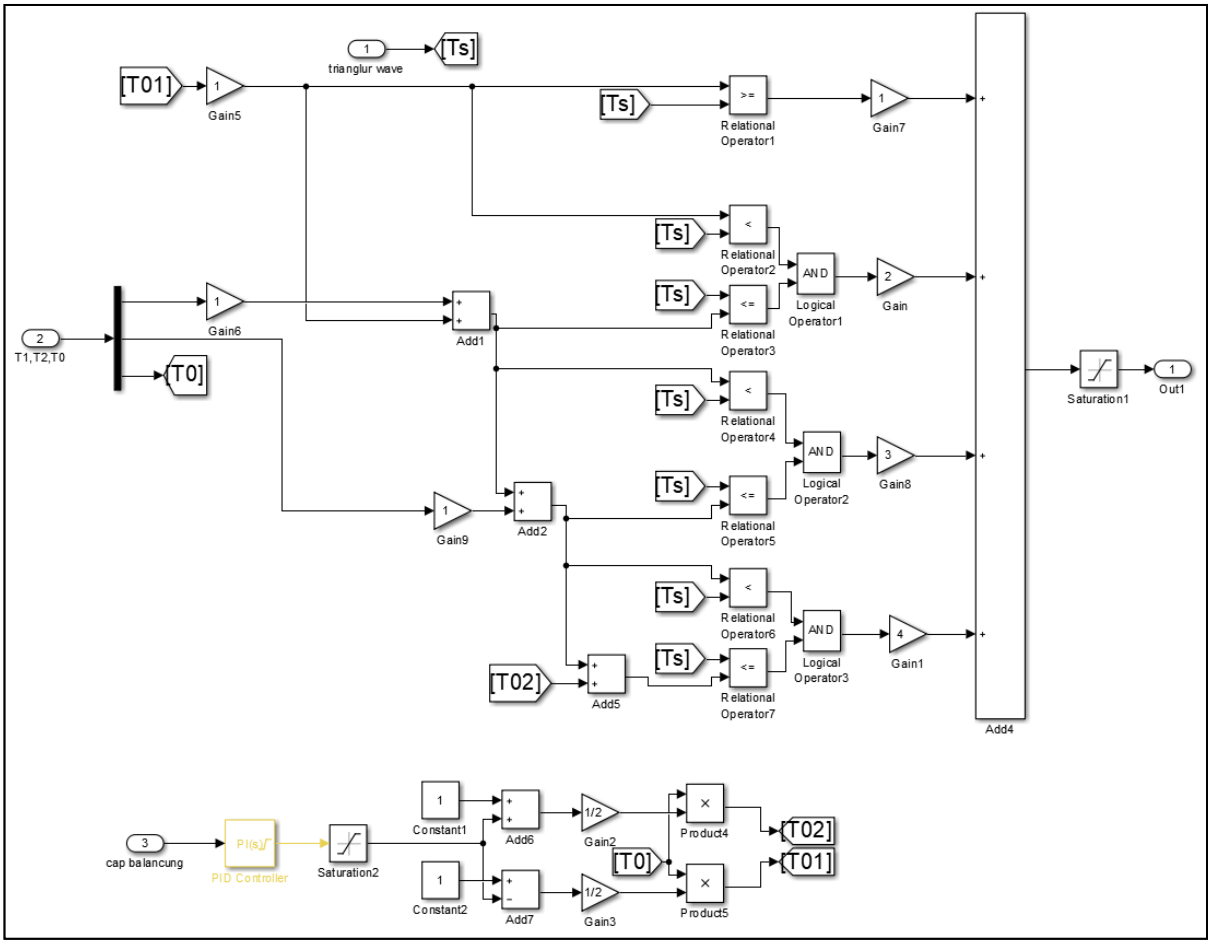

Figure 0.7: Capacitor Balancing and Switching States Timing block

In some triangles of the 3-level SV hexagon, the direction of switching sequences are rotating clockwise while it is rotating counter clockwise in other triangles. On the other hand, the timing of the switching states is generated in a clockwise manner. Therefore, a block must be implemented to ensure that the timing is assigned for the correct switching state as illustrated in Figure B.8.

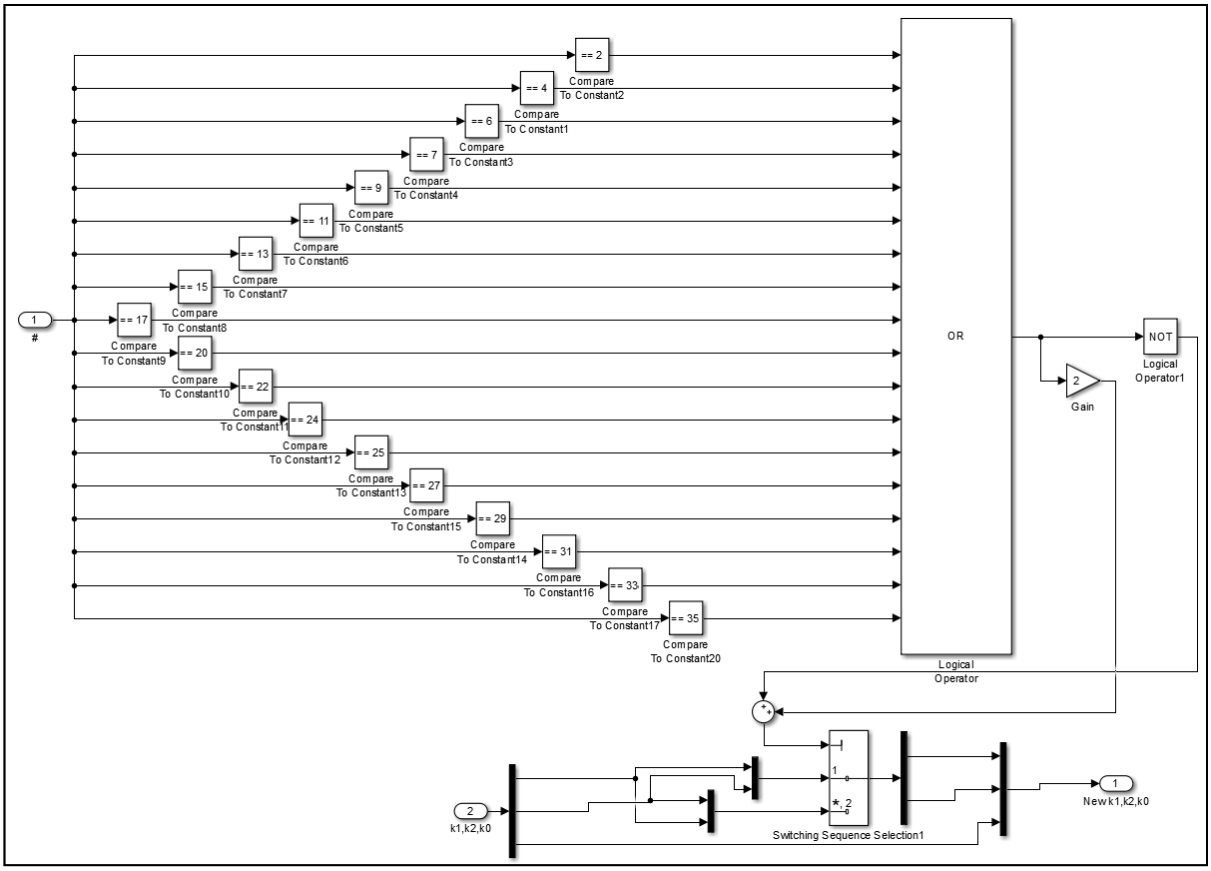

Figure 0.8: Fixing Sub-vectors Rotation block

Figure B.9 depicts the lookup table that contains the switching sequences of all 36 triangles in the 3-level space vector diagram. The input of this block is the number of the triangle while the output is the switching sequence of the selected triangle.

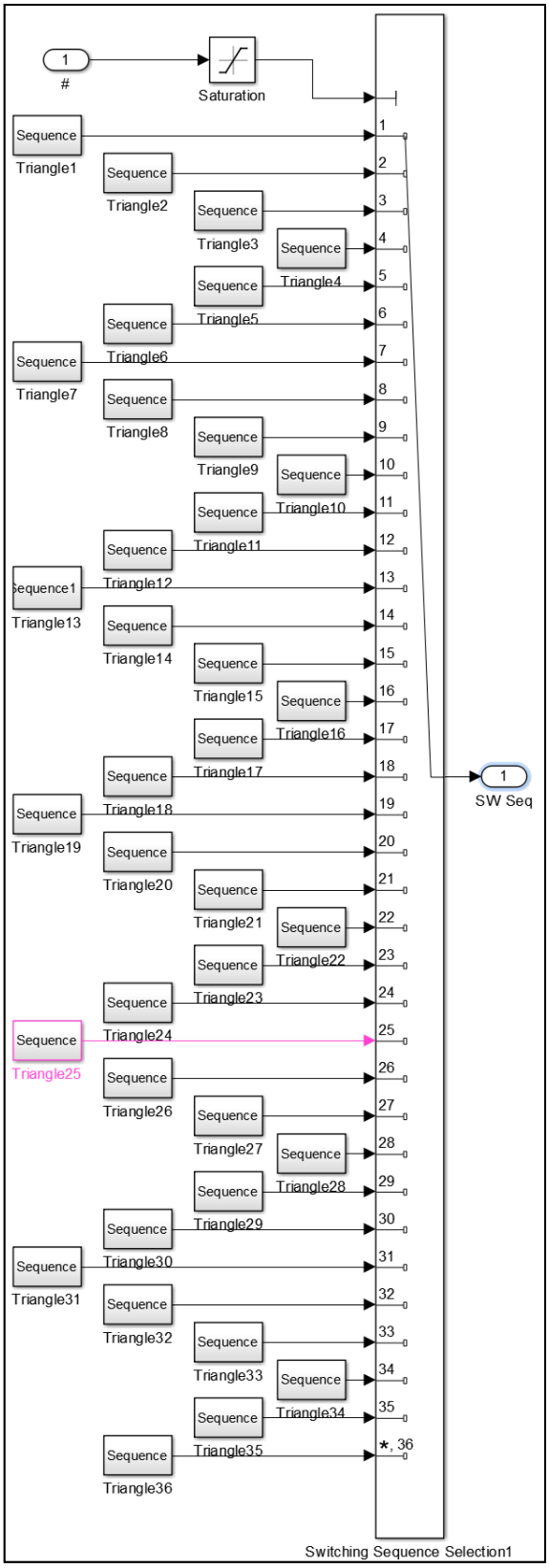

Figure 0.9: Lookup Table for all Switching Sequences block

Figure B.10 illustrates the switching sequence of triangle 1 of the 3-level SV diagram. The switching states (100) and (011) are the redundent states while (000) and (010) are the adjacent states.

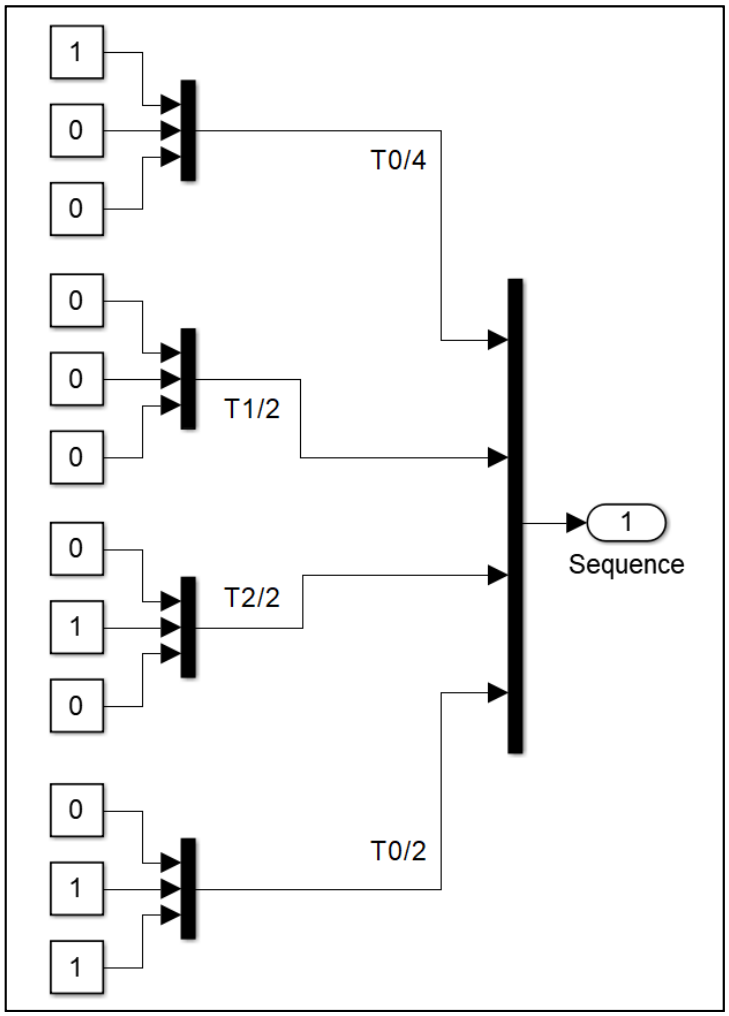

Figure 0.10: Triangle 1 block