Design and Development of Exclusive Modulation Techniques for Effective Power Regulation in Dual Two-level-inverter-fed Open-ended Winding Traction Motors

by

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A thesis submitted to the
School of Graduate and Postdoctoral Studies in partial
fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering
Department of Electrical, Computer and Software Engineering
School of Graduate and Postdoctoral Studies
Faculty of Engineering and Applied Science
University of Ontario Institute of Technology
Oshawa, Ontario, Canada
April 2019

THESIS EXAMINATION INFORMATION

Submitted by: Rishi Menon

PhD in Electrical, Computer and Software Engineering

Thesis title: **Design and Development of Exclusive Modulation Techniques for Effective Power Regulation in Dual Two-level-inverter-fed Open-ended Winding Traction Motors**

An oral defense of this thesis took place on April 17, 2019 in front of the following examining committee:

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

Abstract

An integral part of an EV propulsion system is the traction drive. The existing two-level inverter drives reportedly has several drawbacks. Multilevel inverter has been proposed as an improvement over the conventional inverter drive for EVs. Dual two-level inverter topology, fed from isolated DC sources (battery packs) can be a suitable preference for the multilevel inverter in EVs. However, in this topology, the isolated DC sources obtained from battery packs may have different charge or capacities due to their manufacturing tolerances and aging over the time. This will result in different voltage levels and state of charge (SOC) in the individual battery pack. In normal operation of the drive, power flow between isolated sources need to be regulated.

In first work, a simple carrier-based modulation (CBM) technique for sharing and controlling the power flow between isolated DC sources in a dual two-level inverter has been proposed . The proposed technique is extensively studied for different steady state and dynamic conditions. The effectiveness of the proposed technique for EVs is analyzed for different driving profiles and results are provided for dynamic SOC balancing between the isolated battery sources.

In the second work, an output current ripple analysis is provided for the dual two-level inverter for varied power sharing ratio. This work demonstrates that the ripple in motor phase current changes when the power sharing in dual two-level inverter is changed. Current error trajectory and current ripple envelope for different switching schemes are compared for equal and unequal sharing. Polar plot representations for peak to peak current ripple in linear modulation range are also illustrated for varied power sharing.

The concepts were initially simulated using Matlab/Simulink and PLECS. A 5.7 kW open-end winding induction motor was used as the load for experimental studies. The dual inverter system was build using two Semikron's stacks having half-bridge modules of SKM50GB12T4. For the speed control and PWM, a digital signal processor (TMS320F28069M) and a real-time simulator OPAL-RT (OP8665) were used.

Keywords: Current ripple; dual inverter; electric vehicle; PWM; SOC.

Declaration of Authorship

I hereby declare that this thesis consists of original work of which I have authored. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Statement of Contribution

Part of the work described in Chapter 1 has been published as:

[1] **R. Menon**, A. H. Kadam, N. A. Azeez and S. S. Williamson, "A comprehensive survey on permanent magnet synchronous motor drive systems for electric transportation applications," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 6627-6632.

Part of the work described in Chapter 2 and 3 has been published as:

[1] **R. Menon**, N. A. Azeez, A. H. Kadam, S. S. Williamson and C. Bacioiu, "An instantaneous power balancing technique for an open-end IM drive using carrier based modulation for vehicular application," *IEEE Transactions on Industrial Electronics* doi: 10.1109/TIE.2018.2886749.

[2] **R. Menon**, S. S. Williamson, and A. H. Kadam, "A fault tolerant strategy for an open-ended dual inverter traction motor drives," *IEEE Transactions on Transportation Electrification*. (under review)

[3] **R. Menon**, S. S. Williamson, N. A. Azeez and A. H. Kadam "A modulation strategy for fault tolerant operation in dual inverter drive," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore. (under review)

[4] **R. Menon**, N. A. Azeez, A. H. Kadam and S. S. Williamson, "Energy loss analysis of traction inverter drive for different PWM techniques and drive cycles," in *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Hamilton, 2018, pp. 201-205.

Part of the work described in Chapter 4 has been published as:

[1] **R. Menon**, N. A. Azeez, A. H. Kadam and S. S. Williamson, "Study and analysis of the effects of varied PWM techniques and power sharing ratios on the current ripple in open-ended, 3-level traction motor drives," *IET Electrical Systems in Transportation*. (under review)

This work is dedicated to my family…

Acknowledgements

First, I would like to thank the God Almighty for giving me the opportunity, strength and necessary patience for completing this Ph.D. program.

I would like to express my deepest gratitude to my research supervisor Prof. Sheldon S. Williamson, for his continuous support, guidance, and motivation throughout my research work. I consider myself quite privileged to work in his research group. I could learn many valuable lessons from him, which will help me in my future professional life. I would always admire him for the elderly love and wisdom he has gifted me.

I am deeply grateful to Dr. Najath Abdul Azeez, for his insightful mentoring during my research. His practical advices helped me to understand and enrich my concepts on the subject. The interesting discussions that we had over technical matters would always be cherished. I'm indebted to Dr. Lalit Patnaik for his valuable feedback and critical comments during lab meetings, which helped me to think harder about my work. My special word of thanks is to the Graduate Program Assistant, Joel Stewart for all departmental support during the research.

I express my deep sense of gratitude to late Dr. Voiko Lukanov (Founder of D&V Electronics Ltd). Although our interactions were few, but I have been highly influenced by his vision and passion for the automotive technology.

I convey my sincere thanks to the management of D&V Electronics Ltd, for supporting and providing facilities to build my hardware in their research lab. I

would like to thank in particular, Kalina, Will, Ciprian, Veliko, Pasquale, Brian for their kind support.

I would like to thank my fellow lab mates Arun, Arvind, Navbir, Siddhartha, Kunwar, Janamay, Amandeep, Vamsi, Deepak, Praneeth, Ronanki, Sang, Deepa, David, Manjot for stimulating discussions and all the fun we have had in the last few years. Arvind deserves a special mention for all his help in technical documentation as well as providing updated information around the globe.

Most importantly, none of this would have been possible without the love and motivation of my family. They have been a constant source of support and pillar of strength all these years. Dr. K. Gopakumar deserves a special acknowledgment, for being a driving force and having high hopes which always inspired me to pursue my higher studies.

Rishi Menon

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List of Abbreviations

EV	**E**lectric **V**ehicle
VSI	**V**oltage **S**ource **I**nverter
DC	**D**irect **C**urrent
AC	**A**lternating **C**urrent
PWM	**P**ulse **W**idth **M**odulation
CBM	**C**arrier **B**ased **M**odulation
SVM	**S**pace **V**ector **M**odulation
SVPWM	**S**pace **V**ector **P**ulse **W**idth **M**odulation
THI	**T**hird **H**armonic **I**njection
DPWM	**D**iscontinuous **P**ulse **W**idth **M**odulation
DCC	**D**iscontinuous **C**continual **C**lamp
DSC	**D**iscontinuous **S**split **C**lamp
FFT	**F**ast **F**ourier **T**ransform
EMI	**E**lectro **M**agnetic **I**nterference
IM	**I**nduction **M**otor
V/f	**V**oltage over **H**ertz
FOC	**F**ield **O**riented **C**ontrol
SoC	**S**tate **O**f **C**harge
DSP	**D**igital **S**ignal **P**rocessor

HIL	**H**ardware - **I**n - **L**oop
THD	**T**otal **H**armonic **D**istortion
WTHD	**W**eighted **T**otal **H**armonic **D**istortion

List of Symbols

M	Modulation index	
CC	Coulomb count	Coulomb
I_{dc}, I	Current	A
V_{dc}, V	Voltage	V
V_{ref}	Reference voltage	V
V_k	DC offset voltage	V
F_s	Switching frequency	Hz
V^d, V^q	dq axis voltage	V
I^d, I^q	dq axis current	A
V^d_{err}, V^q_{err}	dq axis error voltage	V
I^d_{err}, I^q_{err}	dq axis error current	A
k_d	decoupling sharing factor	
k_c	offset sharing factor	

Chapter 1

Introduction

Over several years auto manufacturers always faced a dilemma, how to cut fuel consumption and carbon emissions while preserving the vehicle performance that consumers have been accustomed to. A continuous decline in oil reserve is also considered to be the critical issue around the globe [1]. These issues led to increasing momentum in adoption of environmentally friendly vehicles. In the last decade, there has been a steady rise in Electric Vehicles (EVs), Hybrid Electric Vehicles (HEVs), and Plug-in Hybrid Electric Vehicles (PHEVs) in the commercial market. However, actual sales volumes are still very low. Optimistic forecasts by researchers predict that, with more advances in technology to improve the driving range and battery life, EVs will have a rapid growth in the market in coming years [2], [3]. This fact in itself opens up a radically new scope and sharp edge challenges in EV research.

A typical block diagram of EV system is shown in the of Fig. 1.1. Traction motor is the prime energy conversion component in EV propulsion system. Some

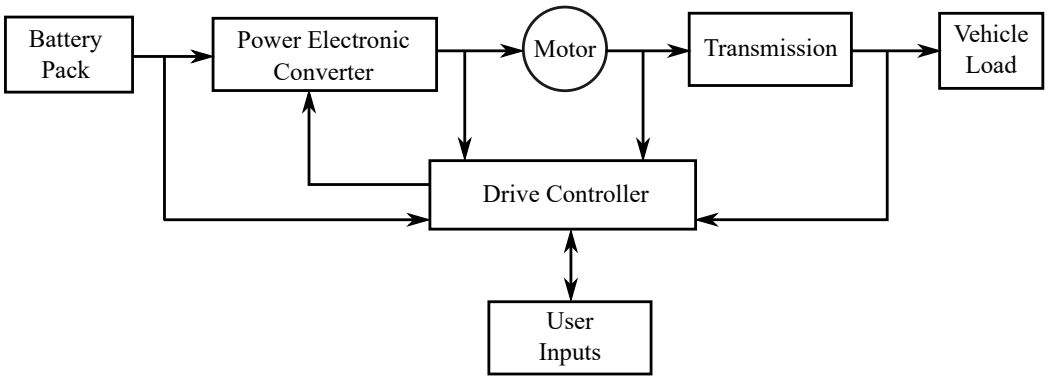


Figure 1.1: Block Diagram of an EV system

of the requirement for traction motor are: (i) High torque capability from zero to base speed, (ii) constant power capability over a speed range of typically above base speed, (iii) high efficiency over a wide range of operating conditions. Based on the above requirements, suitable electrical motors for EVs with applicability and dynamic operation has been comprehensively reviewed in [4]. Out of various types of electric motors, three-phase AC motors are more preferred than the DC motors. In AC motors, induction motors (IM) are widely used due to their rugged, reliable and economical construction. However, they are subjected to the cage losses at lower and higher speeds. Permanent magnet synchronous motor (PMSM), is an alternative to induction motor, with high power and flux density, high torque to weight ratio and lower copper losses. However, PMSM has eddy current losses, limited transient overload power and high uncontrolled generator voltage [5]. Switch reluctance machines are also attractive solution due to their simple and rugged construction. However, due to their higher torque ripple and acoustic noise, they are still under research for EV application [6].

In order to operate traction motors over wide range of speeds and load torques,

power electronic converter are required. The converter may use silicon based semiconductor devices like metal-oxide-semiconductor field-effect transistor (MOSFETS) or insulated gate bipolar transistors (IGBTs) with anti-parallel diodes to provide bidirectional power flow. The drive controller provides pulse width modulation (PWM), which triggers the devices in converter, to generate power output at required voltage and frequency. The drive controller may have several control loops, for regulating voltage, current, torque, flux, speed, position, tension, or other desirable conditions of the load. Each of these may have their limiting features purposely placed in order to protect the motor, the converter, or the source. The input commands and the limiting values to these controllers would normally come from supervisory control systems, that produce the required references for the drive demanded by the user [7]. The traction motor, power converter and drive controller together forms the whole drive system for EVs. In the next section, various power converters used for traction drives are discussed in detail.

1.1 Classification of converters for traction motor drives

Converters for high-power motor drives, can be broadly classified into three types namely cycloconverters, current source inverters (CSI) and voltage source inverters (VSI) as shown in Fig. 1.2 [8].

Cycloconverter is an AC/AC converter. It is a direct frequency converter that converts a fixed AC input to an adjustable AC output, whose voltage and frequency can be independently controlled. They are typically used for industrial

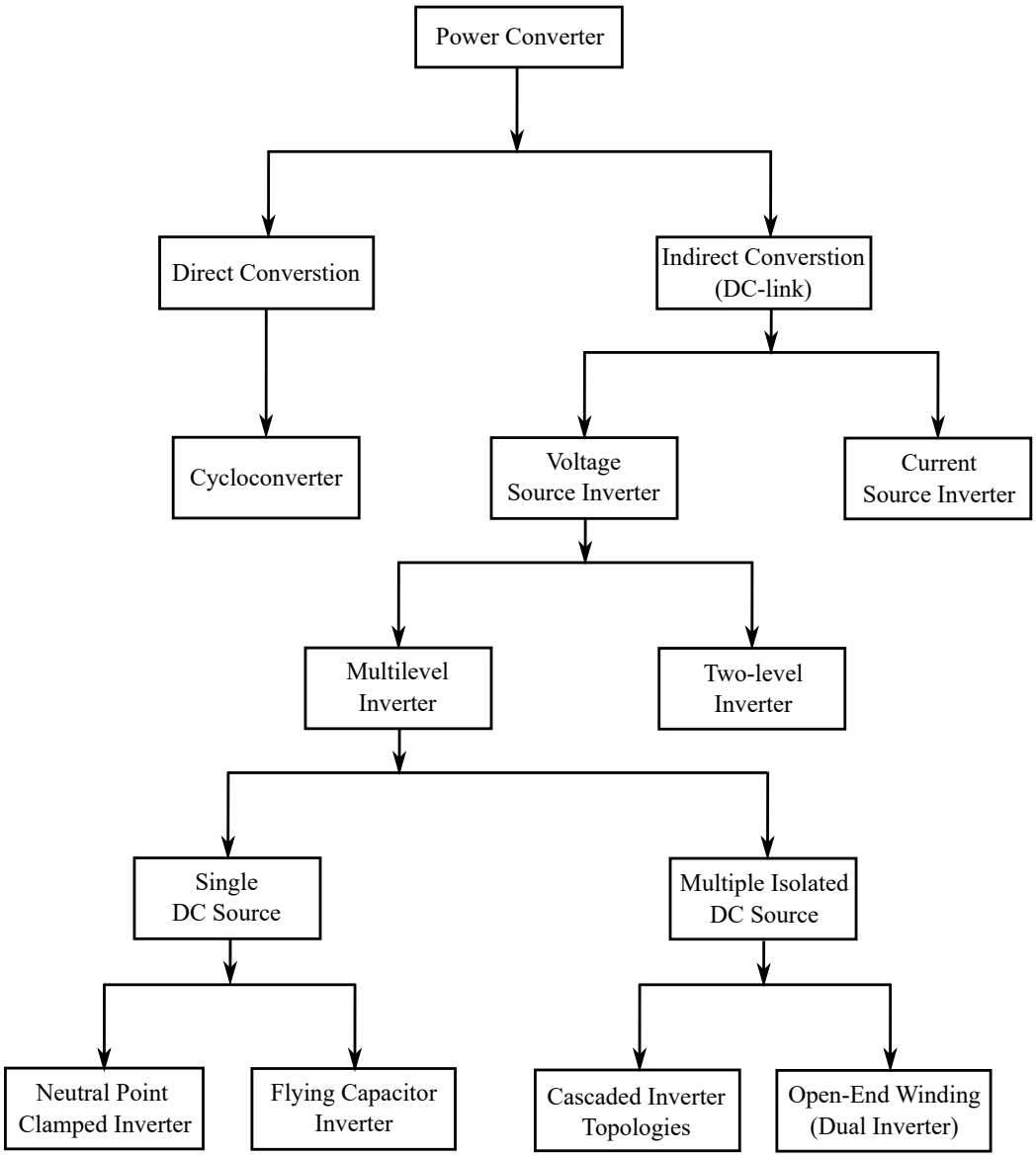


Figure 1.2: Classification of power converter for traction application

AC motor and now increasingly used for the traction motor drive emulation [9]–[11].

The current source inverter (CSI) and Voltage source inverters (VSI) are DC to AC converters, hence named as inverters. The current source inverters are fed

from a DC current source and convert it to AC current output. CSI consists of DC link inductor and inverter switches, which produces controlled AC current output [12], [13]. Its main advantage in motor drive application is the inherent protection against overloads and it is used for specific applications [14], [15]. The most preferred converter for motor drives is VSI. In this, a fixed DC voltage is converted to variable AC voltage. VSIs depict a faster dynamic response compared to CSIs, since there is no line inductor in the DC link. The next sections discuss VSI and its types in detail.

1.1.1 Voltage source inverters

The most popular choice of circuit topology for EV application among the different types of converters is the voltage source inverter [16]. For three phase motors, the fixed DC voltage is converted to three-phase AC voltage with variable magnitude and frequency. A typical VSI fed drive system for three phase AC motor is shown in Fig. 1.3. The DC-link capacitor between the source and converter is to filter out the high frequency switching ripples. The selection of DC link capacitors, bus bar design for low stray inductance etc. need careful attention for reliable operation

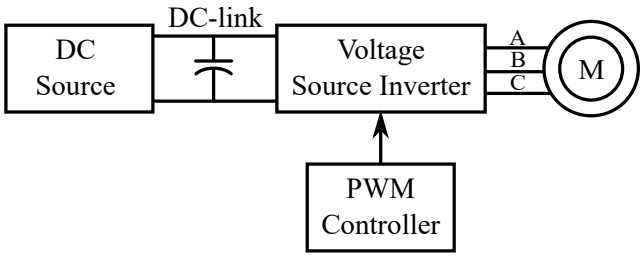


Figure 1.3: Block diagram of a VSI.

of the drive [17], [18]. With increase in power level, specific protection modules like over voltage, over current, saturation and temperature detector are included in the power circuit [19]. The voltage source inverters can be further classified into two categories, the two-level and multilevel inverter topologies. The two-level inverters are the most popular configuration for motor drives in EV. However, due to continuous demand to achieve better performance and efficiency, two-level inverters are being replaced with multilevel inverters. When compared to two-level inverters, the merits offered by multilevel converters are reduced harmonic content in output voltage and current, lower common mode voltage, reduced dv/dt, lesser voltages stress on power switches and better fault tolerance [20]–[22]. The circuit configuration and characteristics of both the topologies will be discussed in the next sections.

1.2 Two-level inverters

The two-level VSI is the simplest and first converter topology used for the three-phase traction drives [23]. The Fig. 1.4 show the general schematic for the two-level VSI. The two-level VSI consists of three half-bridges with total 6 power semiconductor switches. In this, A-phase voltage is generated by the half-bridge consisting of switches S_1 and S_2. Similarly, B-phase and C-phase voltages are generated by the other two half-bridge formed by switches S_3, S_4 and S_5, S_6 respectively. The logic states of the switches in a half bridge are opposite. The output of each half-bridge (between midpoint of half bridge and DC-link ground) is called the pole voltage (V_{AO}, V_{BO}, V_{CO}). The pole voltage of this inverter can take two values (0

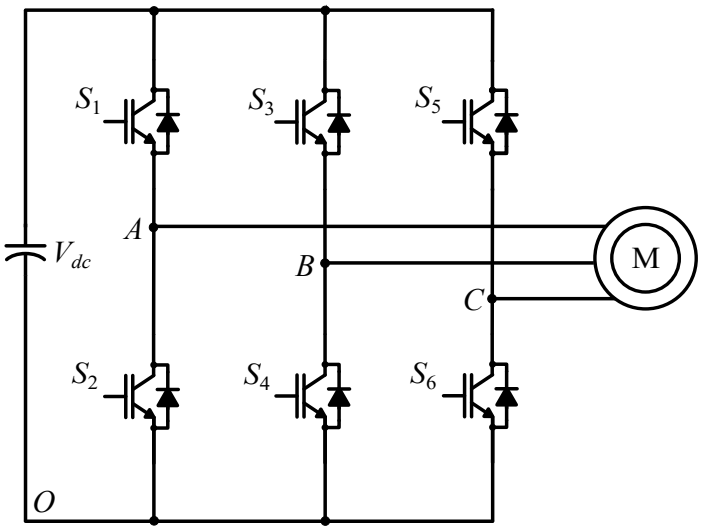


Figure 1.4: Schematic of the two-level inverter.

and V_{dc}), hence the name two-level VSI. When the top switch is ON and bottom switch is OFF, the output of half-bridge is V_{dc}.

In the complimentary switch state, the output is 0. To avoid short circuiting during transition of the states, a dead-time is inserted by turning off both switches for a very short duration [24]. The performance of the inverter is highly influenced by the PWM techniques, associated switching losses, conduction losses, output and DC-link current ripple. For inverters based on IGBT, dead-time of 1 or $2\,\mu\,\mathrm{sec}$ is generally used. MOSFET being much faster compared to IGBT, the dead-time are reduced to hundreds of nanoseconds [25]. Since the connected load of VSI is inductive, anti-parallel diodes are used to freewheel the load current during the time when both the switches of an inverter leg are in the OFF state.

In two-level inverters, when all the three pole voltages are considered together, there are eight states for the inverter and corresponding to each state, there is a

voltage space vector (reference vector) which is applied to the motor. The reference vector generated by these states can be mapped to a two-dimensional $\alpha\beta$ plane as shown in Fig. 1.5. The reference vector can be expressed as

$$\vec{V}_{ref} = |V_{ref}|\angle\theta = V_\alpha + jV_\beta \tag{1.1}$$

There are six active vectors, V_1 (100), V_2 (110), V_3 (010), V_4 (011), V_5 (001) and V_6 (101) and two zero vectors V_0 (000) and V_7 (111). In this '1' implies that the top device is ON and '0' implies that the bottom device is ON as shown in Fig. 1.6. The tips of the active vectors when joined together form a hexagon. The active vectors are separated by 60^o, making six equal triangular sectors in hexagon. Any voltage reference vector $\vec{V}_{ref}$, inside a hexagonal sector, can be generated using the available vectors of the sector [26], [27]. The per unit pole voltage corresponding to the state of inverter is shown in Table 1.1.

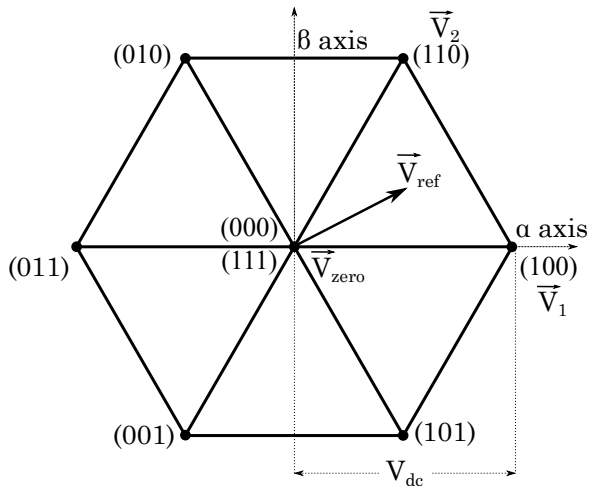


Figure 1.5: Voltage space vector diagram of the two-level inverter.

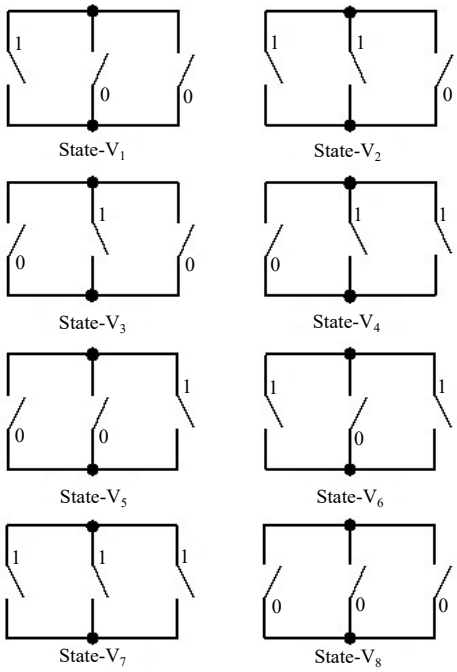


Figure 1.6: Switching states of the two-level inverter.

Table 1.1: Switching states and pole voltage of the two-level inverter.

Space vector	Inverter state (A,B,C)	Pole voltages (p.u)			Voltage space vector (p.u., V_{dc})
		V_{AO}	V_{BO}	V_{CO}	
V_0	000	0	0	0	0
V_1	100	1	0	0	$1\angle 0^o$
V_2	110	1	1	0	$1\angle 60^o$
V_3	010	0	1	0	$1\angle 120^o$
V_4	011	0	1	1	$1\angle 180^o$
V_5	001	0	0	1	$1\angle 240^o$
V_6	101	1	0	1	$1\angle 300^o$
V_7	111	1	1	1	0

Different PWM schemes can be used to generate the fundamental reference voltage. The main aim of these PWM schemes is to generate a fundamental voltage of required amplitude and frequency, as desired by the controller. The inverter switching can be achieved through either voltage and current control. In the current control strategy, a hysteresis band is used, to keep the phase current within a predetermined limit. This limit depends on a specified current reference value [28]–[30]. With this hysteresis band, it is difficult to keep switching frequency constant. Hence, this type of control scheme is used for specific speed control applications. The classical form of PWM generation is the voltage PWM control in which the switching frequency can be kept constant. The voltage based PWM generation can be divided into two schemes; continuous and discontinuous conduction. These modulation schemes can be implemented either by carrier-based modulation (CBM) or by space vector modulation (SVM) technique. The former method is straightforward, in which the required modulating wave shape is compared with the carrier to generate the switching pattern. The space vector method realization is based on the pre-calculation of the time length of the inverter state in switching cycle [31]–[33]. The switching vectors are stored in look-up table and are applied for calculated time duration to generate the reference vector (V_{ref}) in a corresponding sector. Moreover, the method also requires the information on sector of two-level hexagon which may lead to complexities and higher execution time in digital implementation [27], [32], [34]. Since SVM generates similar results as the CBM method, SVM method are avoided due to digital computation complexities [34], [35].

1.2.1 PWM for two-level inverters

The most simple and popular scheme in continuous modulation for the two-level inverter is sinusoidal PWM (SPWM)[31], [32], [36]. In this, three-phase sine waves (modulating wave) corresponding to the fundamental frequency of the output voltage are compared with a triangular carrier wave of high frequency as shown in Fig. 1.7. This comparison with carrier wave also denotes to the switching frequency of the devices. Each leg of the two-level inverter is controlled by the respective modulating wave. The magnitude of modulating and carrier wave relates to the reference voltage and carrier voltage respectively. When the reference voltage is more than the carrier voltage, the pole voltage of corresponding half-bridge will be V_{dc}. In the opposite case when the carrier voltage is larger compared to the reference, then the pole voltage is 0. The main drawback of the SPWM scheme is the

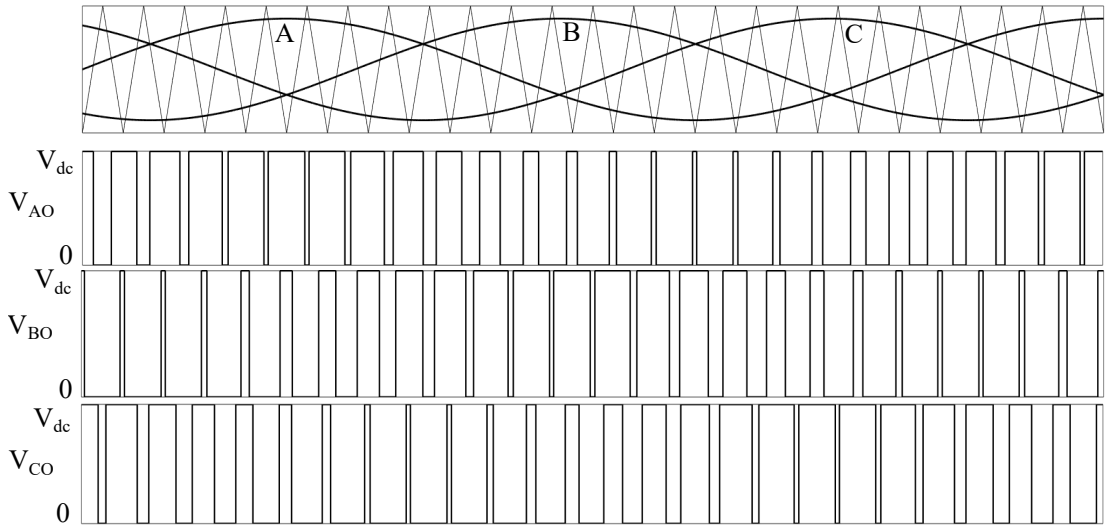


Figure 1.7: Modulating and carrier waves in SPWM for a two-level inverter (top) and pole voltages V_{AO}, V_{BO} and V_{CO} showing two levels.

limited linear modulation range. The maximum fundamental voltage amplitude obtained in SPWM is $0.5V_{dc}$ and results in inefficient utilization of the DC-bus [32], [36].

Another common continuous modulation scheme is space vector PWM (SVPWM), which is used in many applications where voltage controlled VSIs are used [31], [32], [34]–[37]. SVPWM is a modification to the SPWM in which modulating waveform are injected with triplen harmonic component as common mode voltage. Hence also know as triplen harmonic injection (THI) PWM. Since the neutral point of the motor is not connected to the inverter, the common mode voltage will not appear in the phase voltages. The new modulating waveforms, after the addition of the common mode voltages are V^*_{AN}, V^*_{BN} and V^*_{CN} as shown Fig. 1.8 [37]. These new modulating waveforms are compared with triangular carrier waveform , to generates the pole voltages in VSI. It may be noted that the peak amplitudes of these new references are less compared to the original references, and it is possible to get more output voltage while maintaining linear modulation.The major advantage of SVPWM compared to SPWM is the increase in linear modulation range

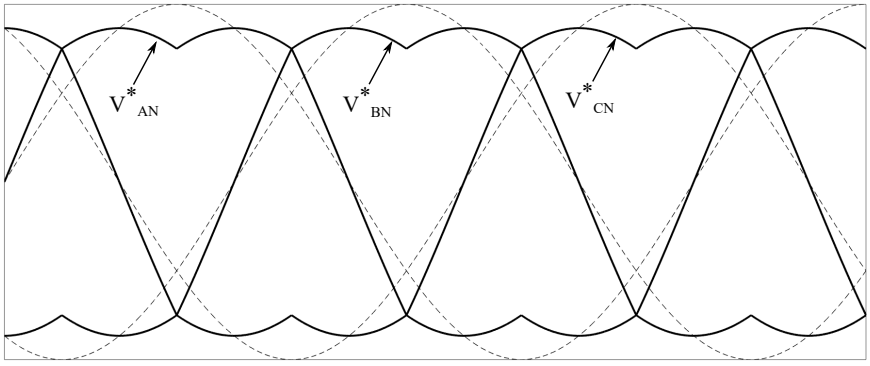


Figure 1.8: Modulating and carrier waves in SVPWM for a two-level inverter.

by 15.4% and better utilization of DC-bus voltage. In this scheme, the maximum fundamental voltage amplitude can be increased to $0.577V_{dc}$ [36].

In two-level inverters, for reduced harmonics, the switching frequency need to be increased. But higher switching frequency will increase switching losses in semiconductor devices. In order to overcome this drawbacks discontinuous modulation schemes (DPWM) are suggested in the literature [38]–[41]. In DPWM, the switching devices are clamped to the positive or negative DC bus over certain intervals, thus also called as bus clamping PWM. The main types of DPWM techniques are continual clamp and split clamp, in which the corresponding phase are clamped to DC bus for 60^o and 30^o interval respectively. This reduces the switching losses to around 33%, compared to the continuous PWM schemes [40]. The DPWM technique could be an effective solution in reducing switching losses. However, the developed torque in machine can have considerable ripples [42], [43]. In vehicular application the torque ripple may not be a concern due to high inertial load [44]. The Fig. 1.9 and 1.10 shows the modulating wave of continual clamp and split clamp schemes. It can seen from the figures that modulating waves are clamped to positive and negative DC bus for particular period in a fundamental cycle. When

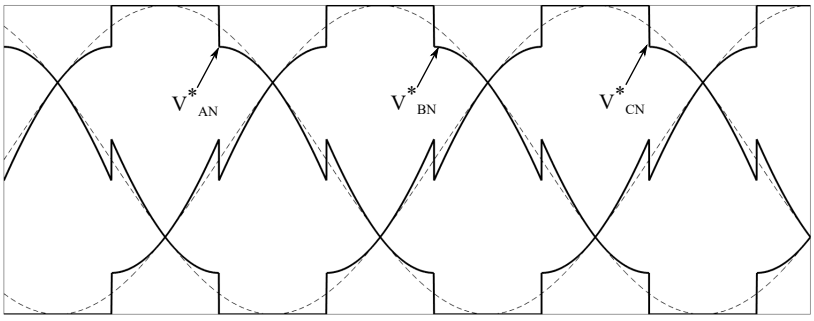


Figure 1.9: Modulating and carrier waves for discontinuous (60^o) PWM

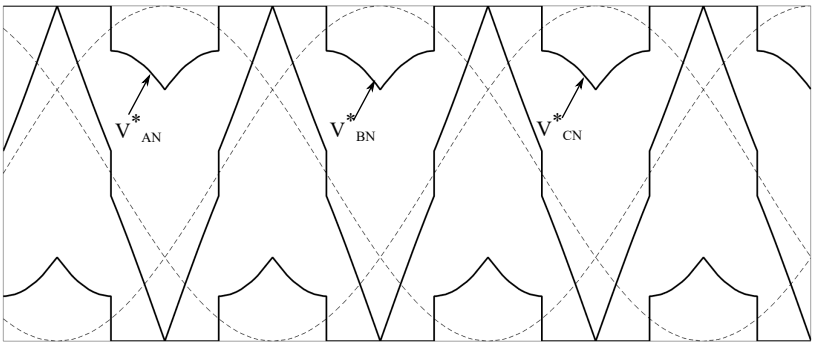


Figure 1.10: Modulating and carrier waves for discontinuous (30^o) PWM

these modulating waves are compared with high frequency carrier wave, there will be no switching in the clamped portion and the generated pole voltages will be discontinuous in pattern.

The two-level inverter has many drawbacks. One of which is the lower output voltage from the high voltage DC source (battery pack) in EV. One alternative to this drawback is to include a DC/DC boost converter between the DC source and two-level inverter, which may complicate the control strategy for both the DC/DC converter as well as the inverter. Secondly, since there are only two levels, the large dv/dt in the output waveform can cause failure of the winding wire insulation [45]. To get nearly sinusoidal current waveforms, the switching frequency of the inverter has to be increased. It will lead to higher switching losses and electromagnetic interference (EMI). If the switching frequency is kept low, it will introduce low order harmonics in phase currents and undesirable torque ripple in the motor [46]. Moreover, the two-level inverter has poor fault tolerance and the failure of any device will result in the complete shut-down of the drive. Multilevel inverter can be a suitable alternative to the two-level inverters. A higher voltage with reduced harmonic distortion and better electromagnetic compatibility can be synthesized from

lower voltage inputs in multilevel topologies. Moreover, the switching frequency of the devices can be kept low, which will reduce dv/dt, device stress, common mode voltage etc [20], [21].

1.3 Multilevel inverters

Multilevel inverters are the most preferred topology for high power application. They have more than two-levels in the individual pole voltage. The importance of multilevel converters is discussed in several publications [20]–[23], [47]–[50]. Although multilevel inverters are already proven technology, it presents a great deal of challenges and offers a wide range of possibilities for research, design and

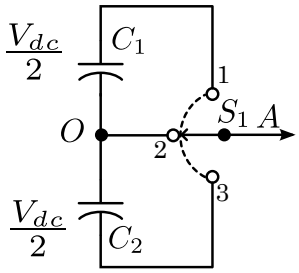


Figure 1.11: Three-level inverter with single pole triple throw switch.

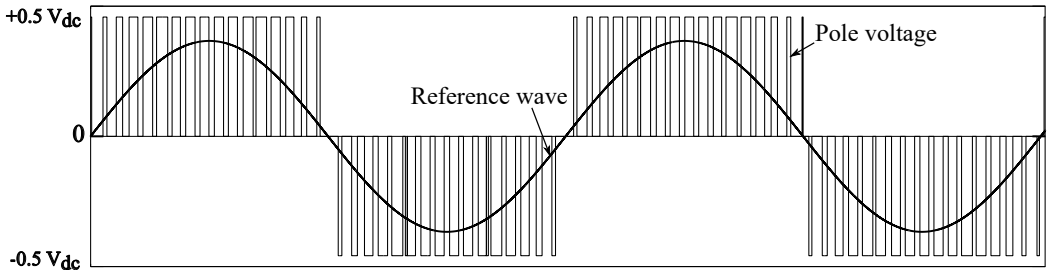


Figure 1.12: Reference wave and the resultant pole voltage for a three-level inverter.

development for automotive application. Active research is being undertaken in transportation sector to improve upon power topology, performance, efficiency, power density, modulation methods, packaging, reliability and cost of multilevel inverters. The simplest multilevel inverter is the three-level inverter. A simplified schematic of one leg of a three-level inverter using a rotary switch with three contacts is shown in Fig. 1.11. The pole voltages obtained from this inverter are $+0.5V_{dc}$, 0 and $-0.5V_{dc}$. Fig. 1.12 shows the voltage reference and the corresponding pole voltage waveform for a three-level inverter. For a general *n*-level inverter, the number of power supply capacitors will be $n-1$, and the rotary switch will be having *n* contacts. There are various circuit configurations by which the rotary switch can be implemented electronically. The three traditional circuit configuration for multilevel topology are neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped and cascaded H-bridge. These are discussed below in detail.

1.3.1 Neutral point clamped inverter

In three-level inverters, the neutral point clamped inverter are one of the most common topology. The schematic of three-level NPC inverter is shown in Fig. 1.13. It consists of 12 IGBTs with anti-parallel diodes and another independent six diodes. The blocking voltage requirements of all the IGBTs and diodes are equal to $0.5V_{dc}$. Consider the leg corresponding to the A-phase. When S_1 and S_2 are ON, the output voltage is $+0.5V_{dc}$. For $-0.5V_{dc}$, S_3 and S_4 are turned ON. To get the midpoint of the DC bus, S_2 and S_3 should be turned ON. In this case, the forward current

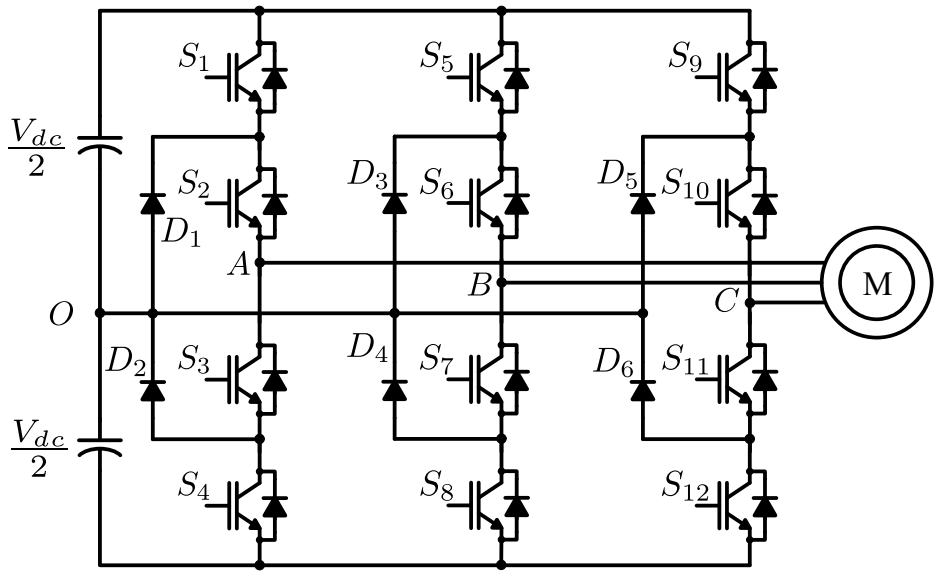


Figure 1.13: Schematic of the three-level neutral point clamped inverter.

will be passing through D_1 and S_2, and the path for reverse current will be through S_3 and D_2. Table 1.2 shows the logic states of the switches to get the required pole voltages. To get more output levels, additional capacitors and switching devices may be incorporated to this circuit configuration. As the number of level increases, reverse voltage across the clamping diodes becomes unequal. To get the same reverse drop, many diodes are to be connected in series. Another issue is the unequal voltage sharing of the capacitors at the DC-link, which can result in undesirable

Table 1.2: Switching logic of the three-level NPC inverter.

Pole voltage	State of A-phase circuit	State of the switch			
		S_1	S_2	S_3	S_4
$+0.5V_{dc}$	2	ON	ON	OFF	OFF
0	1	OFF	ON	ON	OFF
$-0.5V_{dc}$	0	OFF	OFF	ON	ON

output harmonics. Usually additional capacitor voltage-balancing techniques are required to get equal sharing of the capacitor voltages [51]–[53].

1.3.2 Flying capacitor inverter

The flying capacitor inverter is another successful multilevel inverter topology [22], [54]. The DC-bus mid point is generated by floating capacitors, which can be always balanced. Fig.1.14 shows the schematic of the three-level flying capacitor inverter. The capacitors C_1, C_2 and C_3 are the floating capacitors and the voltage across these capacitors are $0.5V_{dc}$. For the A-phase sub-circuit, switches S_1 and S_2 are turned on to get output voltage of $+0.5V_{dc}$. Similarly S_3 and S_4 is activated to get $-0.5V_{dc}$. The DC bus midpoint can be obtained on the output in two ways. One way is by turning on S_1 and S_3, and the other way is by turning on S_2 and S_4. For

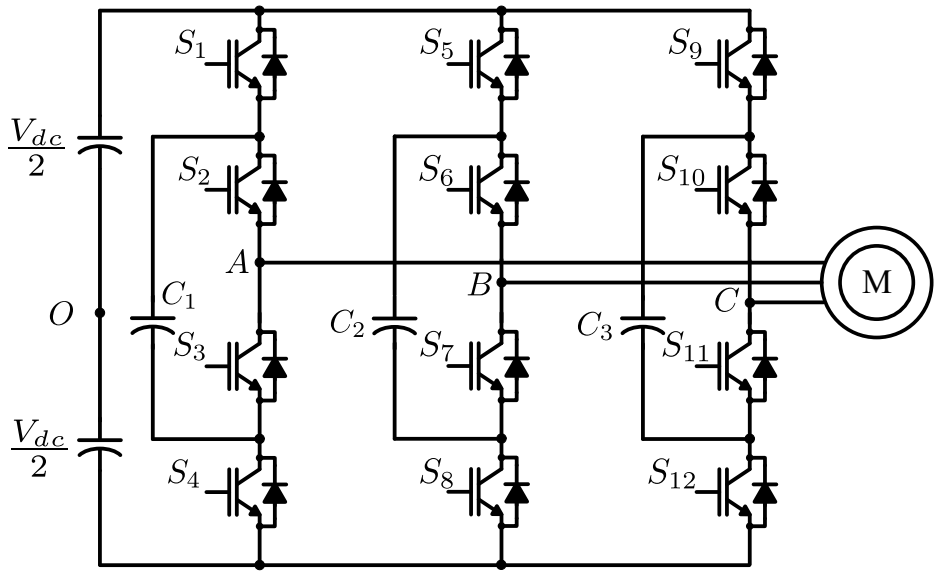


Figure 1.14: Schematic of the three-level flying capacitor inverter.

Table 1.3: Switching logic of the three-level FC inverter.

Pole voltage	State of A-phase circuit	State of the switch				Current direction through C_1	
		S_1	S_2	S_3	S_4	+ve I_A	-ve I_A
$+0.5V_{dc}$	2	ON	ON	OFF	OFF	Zero current	
0	1	ON	OFF	ON	OFF	+	-
0	1	OFF	ON	OFF	ON	-	+
$-0.5V_{dc}$	0	OFF	OFF	ON	ON	Zero current	

the same direction of output current, one connection will give charging of the capacitor and the other will give discharging. By selecting the proper connection to generate the midpoint, the capacitors can be always balanced. The disadvantages of this configuration are the requirement of extra capacitors, voltage sensors and frequent switching to maintain the capacitor voltages using the redundant states. Table 1.3 shows the states of the switches, pole voltages and the capacitor current directions. This topology also can be extended to get more levels.

1.3.3 Cascaded H-bridge inverter

This was first topology which was introduced in multilevel converters [49], [55]–[57]. Fig. 1.15 shows a three-level CHB inverter topology, having three H-bridge cells. Each cell can be powered by independent symmetrical voltage sources and can produce the corresponding pole voltages. This makes the structure more modular. The output voltage that can be obtained from each cell is $+0.5V_{dc}$, 0 and $-0.5V_{dc}$. Consider the sub-circuit for A-phase. When S_2 and S_3 is turned ON, the

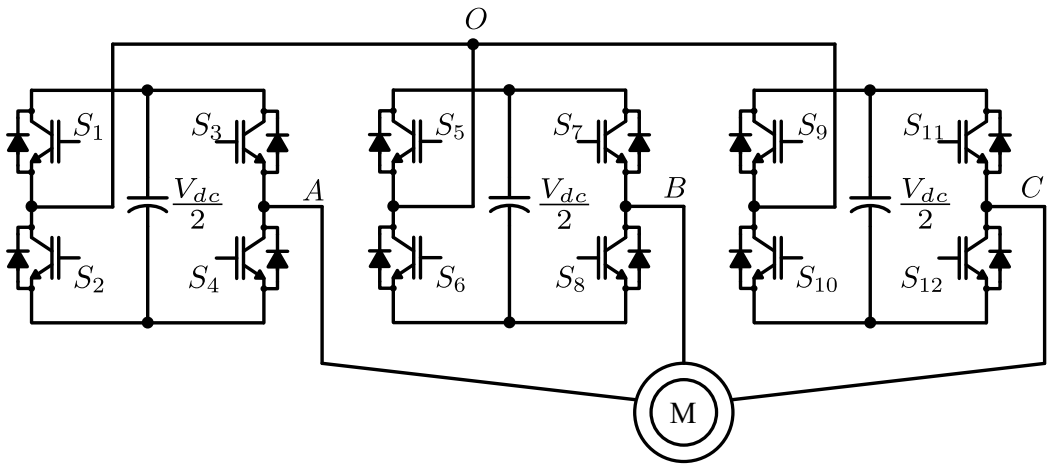


Figure 1.15: Schematic of the three-level cascaded H-bridge inverter.

output voltage is $+0.5V_{dc}$ and for $-0.5V_{dc}$, S_1 and S_4 are turned ON. Zero output can be obtained either by turning ON the bottom switches or by turning ON the top switches of the cell. Table 1.4 shows the states of switches for the corresponding pole voltages. It can be seen from the circuit configuration that the voltage stresses for all the devices will be equal. The topology is more fault tolerant compared to NPC and FC. The disadvantage of this topology is the requirement of multiple isolated power sources [58]. The topology can be easily extended to get more levels. Moreover, with asymmetric voltages, the levels can be increased compared to other

Table 1.4: Switching logic of the three-level CHB inverter.

Pole voltage	State of A-phase circuit	State of the switch			
		S_1	S_2	S_3	S_4
$+0.5V_{dc}$	2	OFF	ON	ON	OFF
0	1	OFF	ON	OFF	ON
0	1	ON	OFF	ON	OFF
$-0.5V_{dc}$	0	ON	OFF	OFF	ON

topologies with similar device count [59], [60].

1.3.4 Multilevel inverter by cascading two-level inverters

A three-level inverter topology obtained by cascading two-level inverter [22], [49], [54] is shown in Fig. 1.16. In this topology, the capacitor balancing issues are avoided by using two separate voltage sources. Also additional clamping diodes are not required and the configuration is much simpler compared to above mentioned three-level topologies. The drawback of this topology is the unequal blocking voltages for the devices. The conventional half bridges can be used to cascade one leg and in that, the top and bottom devices are always complimentary. The inverter switching logic is given in Table 1.5.

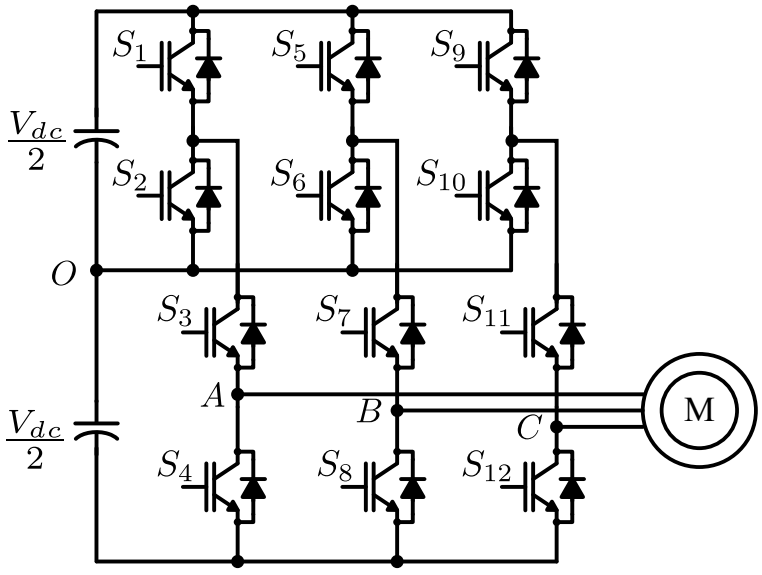


Figure 1.16: Schematic of the three-level cascaded inverter.

Table 1.5: Switching logic of the three-level cascaded inverter.

Pole voltage	State of A-phase circuit	State of the switch			
		S_1	S_2	S_3	S_4
$+0.5V_{dc}$	2	ON	OFF	ON	OFF
0	1	OFF	ON	ON	OFF
$-0.5V_{dc}$	0	OFF	ON	OFF	ON

1.3.5 Dual inverter configuration

In the case of conventional star or delta connected motors, only one end of the stator windings are accessible. It is possible to design various inverter topologies by using both ends in three phase windings of the motor (open-end winding) [61]–[65]. In this configuration, both ends of the windings are connected to separate three phase inverters. It is also know as dual two inverter. The individual inverter can be a two-level inverter or any conventional multilevel inverter [64], [66]. Fig. 1.17 shows a three-level inverter topology for an open end winding motor. It consists of Inverter 1 and Inverter 2 which are conventional two-level inverters, hence popularly know as dual two-level inverter. When compared to other three-level

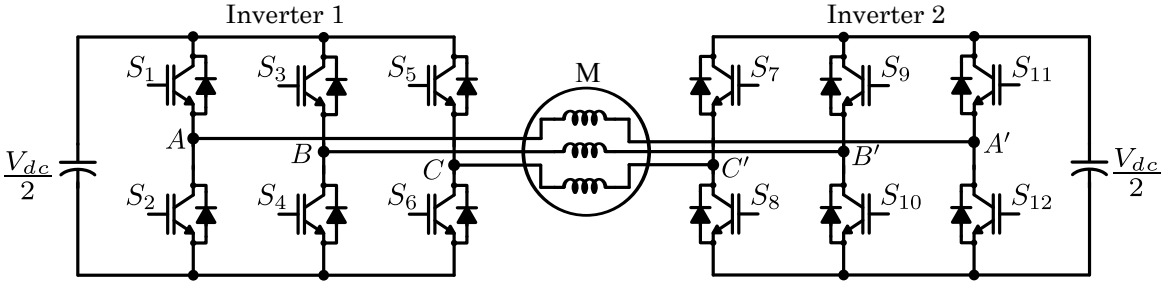


Figure 1.17: Schematic of dual two-level inverter using open-end winding motor.

topologies, the open-end winding motor fed from dual two-level inverter has following advantages:

(i) Additional diodes and capacitors are not required.

(ii) Absence of neutral point fluctuation.

(iii) Independent control of each inverter is possible.

(iv) Simple configuration with higher switching vector redundancy.

(v) Modular and economical due to availability of conventional two-level inverters and its auxiliary circuits.

The open-end winding topology can be supplied either from a single DC source. A single DC source fed dual inverter will have inherent zero sequence current due to the presence of common path. Common mode chokes can be used to suppress the common mode current. However, the large size of inductors will not be suitable for traction application. Alternatively, circulation of common mode current in dual inverter circuit can be removed using specific PWM techniques [63], [67], [68]. However, this may cause a limitation in the output voltage generated by 15% [65]. Thus the effect of zero sequence current is intrinsically eliminated when the topology is fed from isolated DC sources. It is also feasible to produce multilevel output if the topology is configured with one DC source on Inverter 1 and one floating capacitor bank on Inverter 2. When the capacitor is properly balanced and charged, it can act as harmonic filter [69]. The isolated DC supplies can be equal or unequal in voltage magnitude. With the same converter configuration, one can

produce a four-level voltage output with 2:1 ratio of voltages at the both isolated DC source. It has been reported that a four-level inversion is the optimal proportion from unequal isolated DC sources fed to dual inverter [70]. However, due to the asymmetrical DC-links, the power switches at higher DC bus side will have to tolerate double voltage [71].

The topology also has higher tolerance for half-bridge faults [72]. During a fault occurrence in any leg of either one of the two-level inverters, the system can be operated with the healthy inverter as a conventional three-phase drive. This can be implemented by creating an artificial star connection at the faulty inverter by closing either all top devices or bottom devices. This mechanism ensures a reliable operation of the traction drive at half rated power and rated speed [73].

1.3.6 Space vector hexagon and PWM for multilevel inverters

The voltage space vector diagram of the three-level inverter shown in Fig. 1.18 is an extension of the two-level structure. It can be observed that three-level inverter has $27(3^3)$ switching states, of which many states are redundant. It consists of an outer hexagon with seven inner sub-hexagons. The radius of the outer hexagon and the sub-hexagons are V_{dc} and $0.5V_{dc}$ respectively. There are 19 unique voltage space vectors, and the inner voltage space vectors can be generated in multiple ways. The redundant states can be used for capacitor balancing in topologies having capacitors. The inverter states corresponding to the voltage space vectors are marked with 0, 1 and 2 which represents the pole voltage of $-0.5V_{dc}$, 0 and $+0.5V_{dc}$ respectively [62], [63], [65], [74].

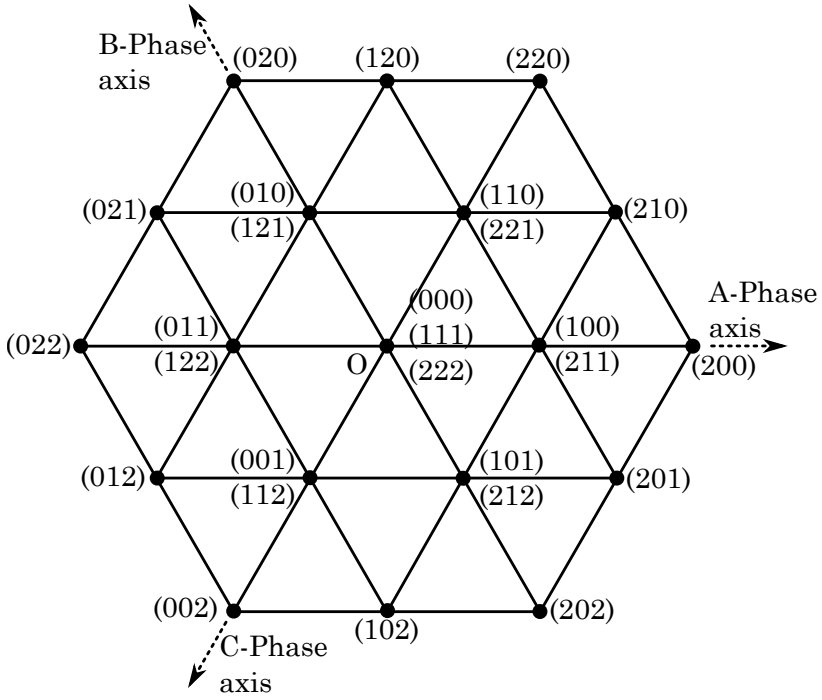


Figure 1.18: General space vector diagram of the three-level inverter.

The carrier-based modulation techniques used for the two-level inverter can be extended to generate the gating signals for the multilevel inverter [75]–[77]. The main problem in this extension is the generation of multiple level shifted carriers in standard digital implementation. There are several methods suggested in which

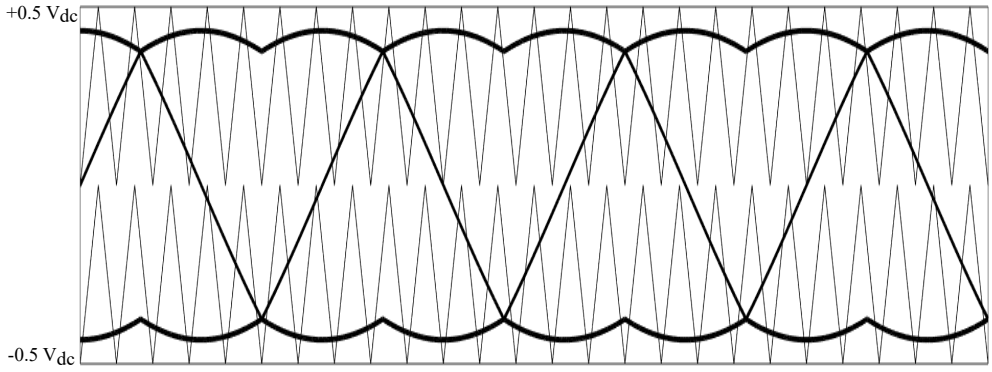


Figure 1.19: Modulating and carrier waves in SVPWM for a three-level inverter

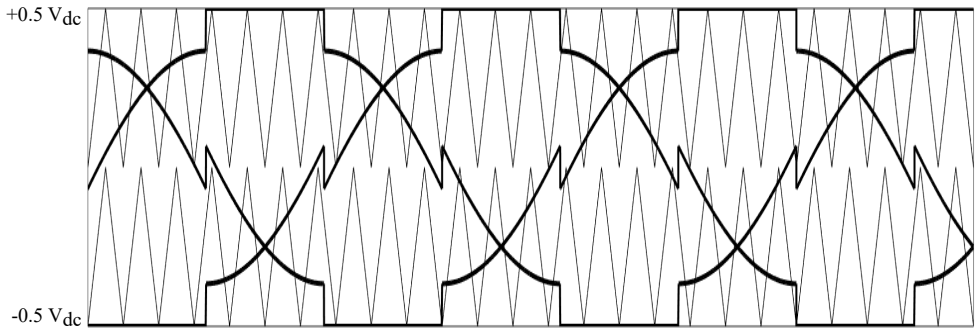


Figure 1.20: Modulating and carrier waves in DPWM (60^o) for a three-level inverter

the reference waves can be modified to compare with single carrier [78]. For a n-level inverter $n-1$ level shifted carrier are required. For three-level PWM generation, two level shifted carrier are used, each with a height of $0.5V_{dc}$. These level shifted carriers can be in phase opposition disposition (POD) or phase disposition (PD). However the latter has proven to be better in harmonics performance [27], [79]. Fig. 1.19 and Fig. 1.20 shows the SVPWM and discontinuous (60^o) PWM schemes in which reference is compared with carrier waves to generate the required pole voltages for a three-level inverter as shown in 1.12.

1.4 Controllers for VSI fed drives

The voltage source inverter fed drives provides three phase voltages of variable frequency and variable amplitude to the motor. A variable frequency is required, since the rotor speed depends on the speed of stator rotating magnetic field. A variable voltage is required for constant flux operation so as to obtain maximum torque at all speeds of operation [80]. Various types of controllers have been proposed for

VSI fed drives [80]–[82]. Induction machines control methods can be classified into scalar and vector control. In scalar control, only magnitude and frequency of voltage, current and flux linkage vectors are controlled. The scalar control methods are simple to implement and the most popular in drive application. The vector control methods not only allows the control of voltage amplitude and frequency, but also the instantaneous position of the voltage, current and flux vectors. This improves significantly the dynamic behavior of the drive. Therefore, several methods for decoupling torque and flux have been proposed. Field oriented control (FOC) and direct torque control (DTC) are the two most popular vector control methods [83]. These control methods are briefly described in the sub-sections below.

1.4.1 V/f Control

The V/f control is the simplest and low cost control scheme for IM [84]–[86]. It is based on the steady state approximation that if the V/f ratio of the IM is kept constant, the air gap flux and torque developed in the motor is constant. At low frequency the approximation is not valid, as the stator resistance cannot be ignored, and a minimum voltage is required to maintain the flux. At frequencies higher than rated value, to avoid insulation breakdown, the voltage is saturated to rated

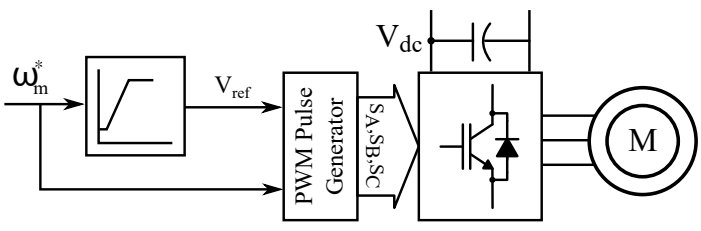


Figure 1.21: Block diagram of open loop V/f control.

voltage. The open-loop V/f controller is illustrated in Fig. 1.21 [84]. The speed control is achieved by varying the voltage in accordance with the desired motor speed. The draw back of open-loop control is that the actual speed of the motor varies according to load torque which affects the slip speed. As a result, this controller is used only in low-performance applications where precise speed control is not necessary [84], [86]. Different closed loop schemes are suggested in the literature to overcome this issue. However, either expensive or complex computation is required to estimate the slip speed [84]. The main drawbacks of V/f control are poor performance at low speeds and during dynamics. Various researchers have tried to address these concerns [87]–[91]. For precise and accurate control, the V/f is being replaced by FOC and DTC in high performance applications.

1.4.2 Field oriented control

The Field oriented control (FOC) was first proposed by K. Hasse [92] and by F. Blaschke [93] in early 1970s. The invention of FOC brought induction machines control similar to the DC machines. FOC provides decoupled control of torque and flux, which is inherently possible in the DC machines. The motor input currents are adjusted to set a specific angle between fluxes produced in the rotor and stator windings. Once the flux angle is known, an algorithm performs the transformation by changing three-phase stator currents into the orthogonal torque and flux producing components. These components are controlled in their d-q axis and an inverse transformation is used to determine the necessary three-phase currents or voltages.

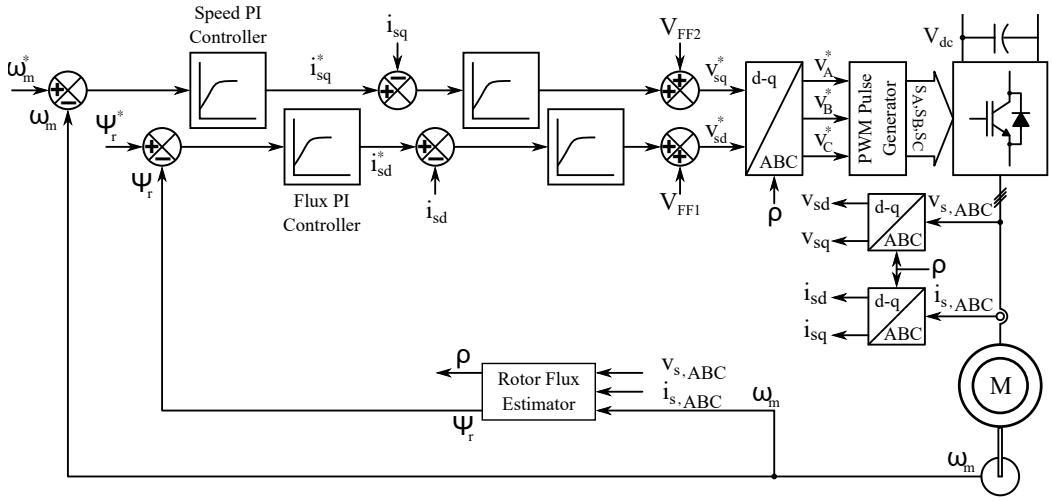


Figure 1.22: Block diagram of direct vector control.

Blaschke [93] used hall sensors mounted in the air gap to measure the machine flux, and thereby obtain the flux magnitude and flux angle for field orientation. Field orientation achieved by direct measurement of the flux is termed as direct flux orientation (DFO). Later on the control scheme for direct FOC has been modified with open loop rotor flux estimator as shown in Fig. 1.22 [94], [95]. Hasse [92], on the other hand, achieved flux orientation by imposing a slip frequency derived from the rotor dynamic equations so as to ensure field orientation as shown in Fig. 1.23. This alternative, consisting of forcing the field orientation in the machine, is known as indirect field orientation (IFO). IFO has been generally preferred than the DFO implementation, to avoid expensive hall probes and complex computation for rotor flux estimation. The operation of IFO requires correct alignment of the d-q reference frame with the rotor flux vector. This needs an accurate knowledge of the machine rotor time constant τ_r. However, τ_r will change during motor operation due to temperature and flux changes. On-line identification of the secondary time constant, for calculation of the correct slip frequency in indirect rotor

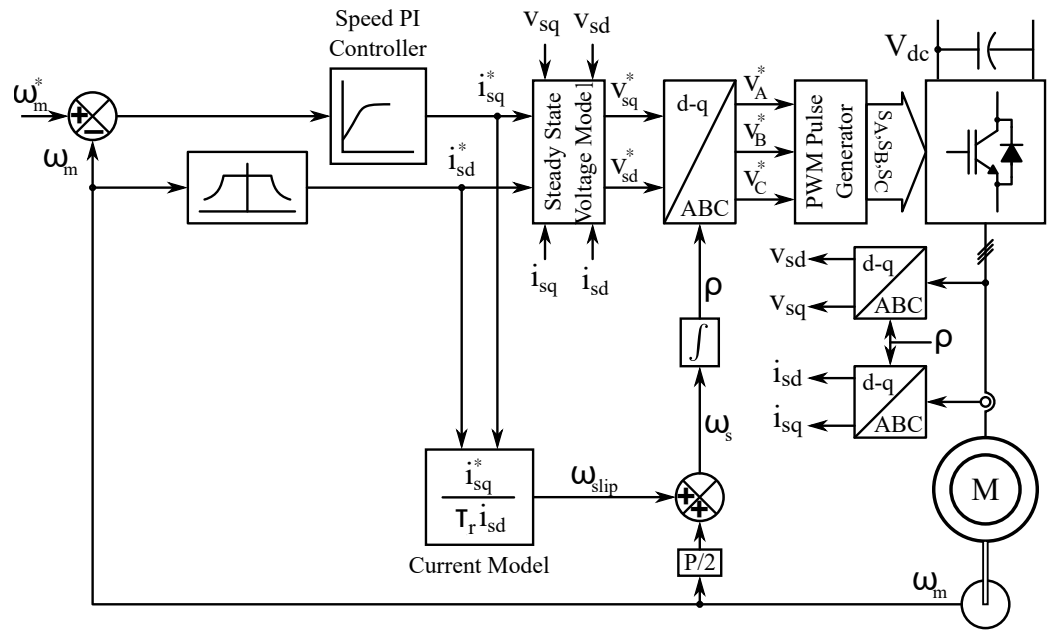


Figure 1.23: Block diagram of indirect vector control.

flux orientation, is essential and has been addressed by different researchers [96], [97], thus providing a means of adapting τ_r during the normal operation of the drive. An indirect rotor flux orientation drive with on-line tuning of τ_r can provide better torque and speed dynamics than a typical DC drive.

The use of vector controlled drives provides several advantages over DC machines in terms of robustness, size, lack of brushes, and reduced cost and maintenance. However the typical FOC based motor drive requires the use of an accurate shaft encoder for correct operation. The use of this encoder implies additional electronics, extra wiring, extra space and careful mounting, which detracts from the inherent robustness of induction motors. Moreover it adds significantly to the overall cost of the motor drive. Therefore there has been great interest among

researchers in developing high performance motor drive that does not require a speed or position transducer for its operation. Various schemes for speed estimation were proposed in literature for achieving speed sensor-less vector control of AC motors [98]–[104].

1.4.3 Direct torque control

New strategies for the torque control of induction motor was presented as direct self control (DSC) by M. Depenbrock [105], [106] and as direct torque control (DTC) by I. Takahashi and T. Noguchi [107]. The principle is based on the hysteresis control and it enables both quick torque response and efficiency operation. DTCs controls the torque and speed of the motor directly, based on the electromagnetic state of the motor. In this control, the motor decoupling and linearization via coordinate transformation used in FOC, is replaced by hysteresis controllers. The hysteresis controllers fits well with the on-off operation of the semiconductor power devices used in the VSIs. It only needs to know the stator resistance and terminal quantities (voltages and currents) in order to perform the stator flux and torque estimations. The basic method for estimating these parameters is by using the stator voltage model which does not require any other physical parameter but the stator resistance.

The basic configuration of the conventional DTC drive proposed by Takahashi is shown in Fig. 1.24 It consists of a pair of hysteresis comparator, torque and flux estimators, voltage vector selector and a VSI. DTC performs separate control of the stator flux and torque, which is also known as decouple control. The core of this

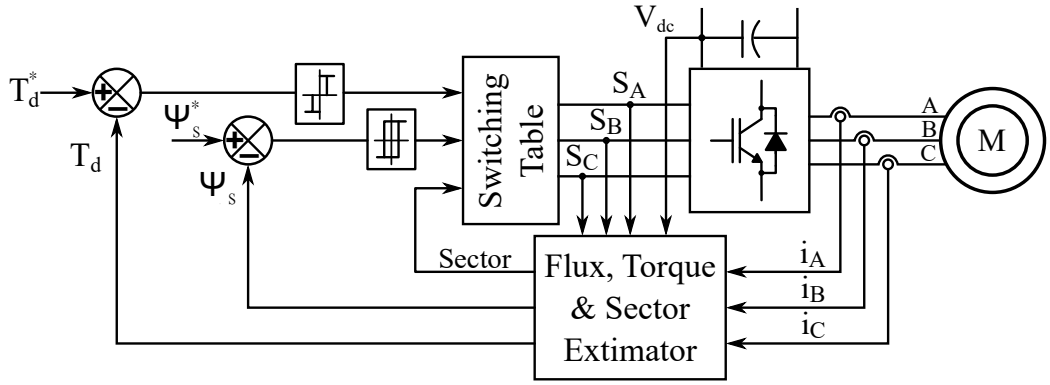


Figure 1.24: Block diagram of direct torque control.

control method is to minimize the torque and flux errors to zero by using a pair of hysteresis comparators. The hysteresis comparators determines the appropriate voltage vector and also the time duration of the selected voltage vector. It could be noted that the whole performance of the system is directly dependent on the estimation of stator flux and torque. Inaccurate estimations will result in an incorrect voltage vector selection. Moreover, with hysteresis bands, there will considerable torque and flux ripples in motor drive. To overcome these problems, extensive research and development has been carried out in DTC [108]–[113].

1.5 Objectives of Thesis

- Develop a PWM technique for effective power sharing in dual two-level inverter drive using carrier based modulation.
- Develop an algorithm for power flow control and state-of-charge balancing in isolated battery sources feeding the dual two-level inverter.

- Detailed performance analysis of the dual two-level inverter drive with power sharing control considering total harmonic distortion (THD), speed and torque ripple, drive cycle tests using hardware-in-loop.
- Illustrate a generalized block diagram representation for power sharing modulation technique with different switching schemes.
- Performance analysis of motor phase ripple current at different sharing ratio in dual inverter drive.

1.6 Scope of Thesis

One of the main desired features of any traction drive is to provide sinusoidal phase current shape during steady-state operation. Moreover, the traction drive should have lower stress on devices, minimum losses, less electromagnetic interference, better fault tolerance etc. Multilevel inverters have been suggested to meet the above-mentioned features in traction drives. Many multilevel topologies are available. However, the automotive industry is still exploring for the most suitable topology with improved features. A dual two-level inverter, generating a three-level output can be a feasible and modular topology for the vehicular application. For improving the performance and reliability of the topology, optimal PWM techniques have been studied in this thesis which can be implemented for EV drives.

Chapter 1 starts with a brief survey on converter topologies used for traction drives. Then, two-level inverters are briefly introduced with the concept of the

space vector structure (hexagon). This is followed by the pulse width modulation techniques for generating switching sequences in two-level inverters. After this, multilevel topology (three-level) and their PWM techniques and space vector structure are briefly discussed. Special mention is made on the features and benefits of the dual two-level inverter when compared to the other three-level topologies. Finally, a detailed study on various controllers for VSI is provided.

Chapter 2 describes the configuration and modeling of dual two-level inverter fed from isolated DC sources. The orientation of space vector hexagon from individual two-level space vectors is also discussed. A very simple carrier based modulation technique is proposed for sharing the instantaneous power between the isolated sources. The proposed technique is conceptually analyzed using mathematical expressions. Switching sequences are provided to explain the effect of power sharing in dual two-level inverter.

Chapter 3 provides the control and block diagram representation of the experimental implementation. The simulation results along with (Fast Fourier Transform) FFT analysis are provided to validate the proposed power sharing modulation technique. Experimental results are provided at different frequency operation to verify power sharing. Finally, the effectiveness of the proposed scheme for EV application is substantiated through SOC balancing and power sharing results in different drive cycles.

Chapter 4 investigates different power sharing PWM techniques in the dual two-level inverter. The effect of these PWM techniques on the motor current ripple is analyzed for equal and unequal power sharing ratios. The trajectory of ripple

currents and peak to peak ripple content for different PWM techniques is also explained under varied power sharing ratio. The chapter concludes with details of analytical study using simulation and experimental results which validate ripple analysis.

Chapter 5 provides an overview of the thesis work and contributions

Chapter 6 explains the scope for future work based on the current contributions.

Chapter 2

Power sharing PWM technique in dual two-level inverter drive

2.1 Introduction

Multilevel inverters have been proposed as an improvement for high power and high voltage electric traction drives. A three-level inverter can be realized by using an open-ended machine, fed from dual two-level inverter [20]–[22]. The topology has a simple configuration when compared to other three-level inverters. As discussed in the previous chapter, the structural advantages made dual two-level inverter to be extensively explored for electric transportation [114], [115]

A dual two-level inverter supplied from isolated DC sources is a modular structure. In EVs, the battery pack, comprising of multiple cells can be conveniently split into two equal sub-packs. It is essential that the isolated battery packs should discharge uniformly and maintain balanced DC voltage at the DC-link terminals.

Due to manufacturing tolerances and aging over the time, the battery packs feeding the individual inverter may differ in charge or capacities. This will cause the cells to hold different voltage levels and state of charge (SOC). If the same amount of power is drawn from both sources, the weaker battery pack may discharge at a faster rate than the other, which may affect the overall performance of the EV drive. For reliable operation, a suitable PWM technique can be implemented to regulate the power flow between isolated battery packs and balance their instantaneous SOCs [116].

In this chapter, a concept of simple carrier-based modulation (CBM) technique is proposed for power flow control in dual inverter drive fed from isolated sources. The modulation techniques is a modification to the conventional three-level PWM generation. The control technique is based on an offset mechanism of the modulating signals in the carrier region. The proposed method is analyzed using switching sequences and mathematical equations. For normal operation in linear modulation range, an expression for the power sharing limit is derived.

2.2 Dual two-level inverter configuration

A dual two-level inverter is derived from cascaded multilevel topology [61]. It feeds a three-phase open-end winding machine from both ends of stator coil using two two-level inverters. The DC sources are electrically isolated to avoid the common mode current in the circuitry as discussed in chapter 1. In this work isolated DC sources are symmetrical and are kept at equal voltage level for a three-level

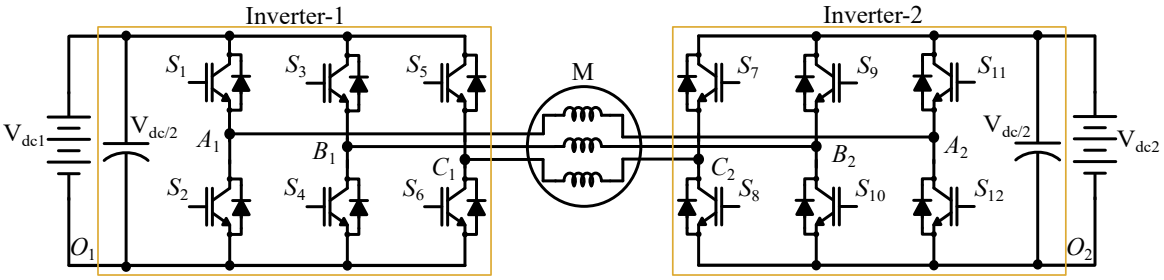


Figure 2.1: Schematic of dual two-level inverter feeding open-ended induction motor with symmetrical battery source.

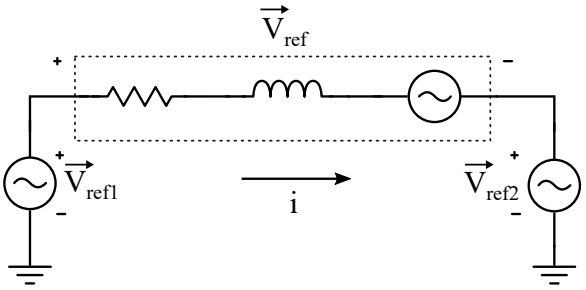


Figure 2.2: Per-phase equivalent circuit of dual two-level inverter.

operation. The dual two-level inverter fed from isolated battery sources is shown in Fig. 2.1 and its per-phase equivalent circuit is shown in Fig. 2.2.

With reference to Fig. 2.1, let fictitious point N be the neutral of the system (though the system by itself does not have a neutral point). Let the Inverter-1 apply voltages at points A_1, B_1 and C_1 and let the Inverter-2 apply voltages at its respective terminals namely A_2, B_2 and C_2. The phase voltage equation for Inverter-1 can be expressed as below:

$$\begin{aligned} V_{A_1N} &= V_{A_1O_1} - V_{NO_1} \\ V_{B_1N} &= V_{B_1O_1} - V_{NO_1} \\ V_{C_1N} &= V_{C_1O_1} - V_{NO_1} \end{aligned} \tag{2.1}$$

where $V_{N_1O_1}$ is the common mode voltage given by

$$V_{NO_1} = \frac{V_{A_1O_1} + V_{B_1O_1} + V_{C_1O_1}}{3} \tag{2.2}$$

Similarly for Inverter-2, we have

$$\begin{aligned} V_{A_2N} &= V_{A_2O_2} - V_{NO_2} \\ V_{B_2N} &= V_{B_2O_2} - V_{NO_2} \\ V_{C_2N} &= V_{C_2O_2} - V_{NO_2} \end{aligned} \tag{2.3}$$

$$V_{NO_2} = \frac{V_{A_2O_2} + V_{B_2O_2} + V_{C_2O_2}}{3} \tag{2.4}$$

By using superposition principle [62], the effective pole voltages and phase voltages (measured at each stator winding ends) of dual two-level inverter can be written as below in (2.5) and (2.6) receptively:

$$\begin{aligned} V_{Apole} &= V_{A_1O_1} - V_{A_2O_2} \\ V_{Bpole} &= V_{B_1O_1} - V_{C_2O_2} \\ V_{Cpole} &= V_{C_1O_1} - V_{C_2O_2} \end{aligned} \tag{2.5}$$

$$\begin{aligned} V_{A_1A_2} &= V_{A_1N} - V_{A_2N} \\ V_{B_1B_2} &= V_{B_1N} - V_{B_2N} \\ V_{C_1C_2} &= V_{C_1N} - V_{C_2N} \end{aligned} \tag{2.6}$$

2.3 Space vector and PWM generation in dual inverter

In dual two-level inverter, each inverter can produce two-level voltage space vectors as shown in Fig. 2.3, and the resultant space vector diagram can be found using the superposition theorem [62]. A graphical method to find the resultant voltage space vector is illustrated in Fig. 2.4. The hexagons drawn with solid and dotted lines represent the voltage space vectors produced by Inverter-1 and Inverter-2 respectively. Since these hexagons can be produced independently, the resultant

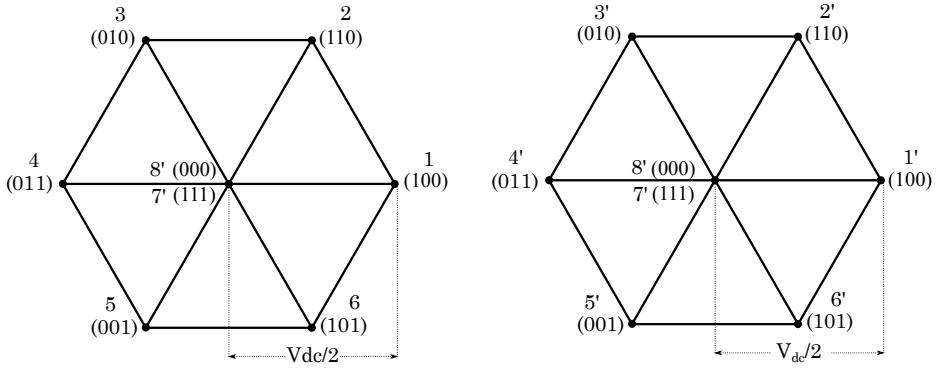


Figure 2.3: Individual space vectors of inverters in dual two-level inverter.

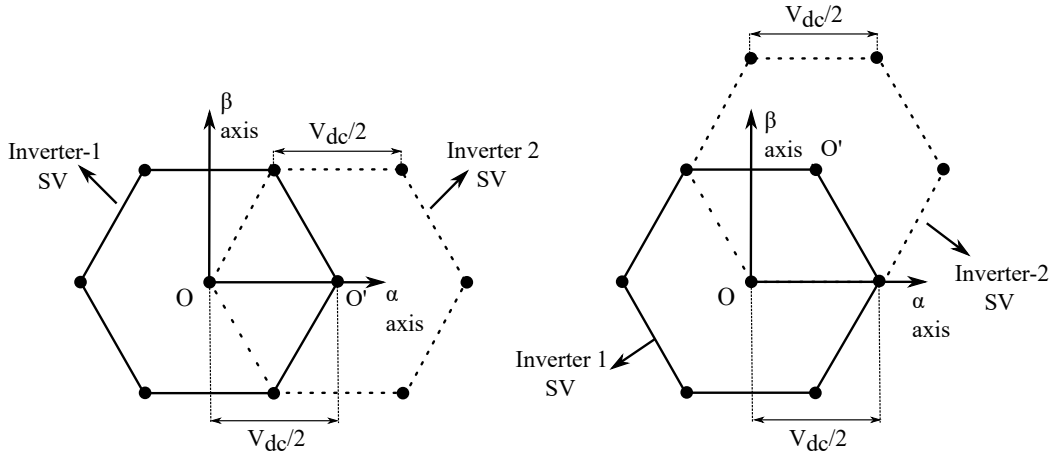


Figure 2.4: Graphical representation of superposing two-level space vectors.

voltage space vector can be found by keeping the center of the second hexagon on the vertices of the first. The figure shows the orientation of voltage space vectors produced by Inverter-2 when the states of the Inverter-1 are 100 and 110 respectively.

The required three-level space vector (SV) by superposing individual two-level SV is shown in Fig 2.5. The SV hexagon has as 6 sectoral triangles and each sector contains 4 inner equilateral triangles with side length of $V_{dc}/2$. The edges of the triangle has the corresponding switching vectors, which are formed by the combination of two-level SV structures [65]. The sector triangle has a median length of $\sqrt{3}/2V_{dc}$, which denotes the maximum radius of the circle that can be inscribed in SV hexagon by the rotating V_{ref}. This can be expressed as below:

$$\vec{V}_{ref} = V_{A_1A_2} + V_{B_1B_2}e^{j120^o} + V_{C_1C_2}e^{j240^o} \tag{2.7}$$

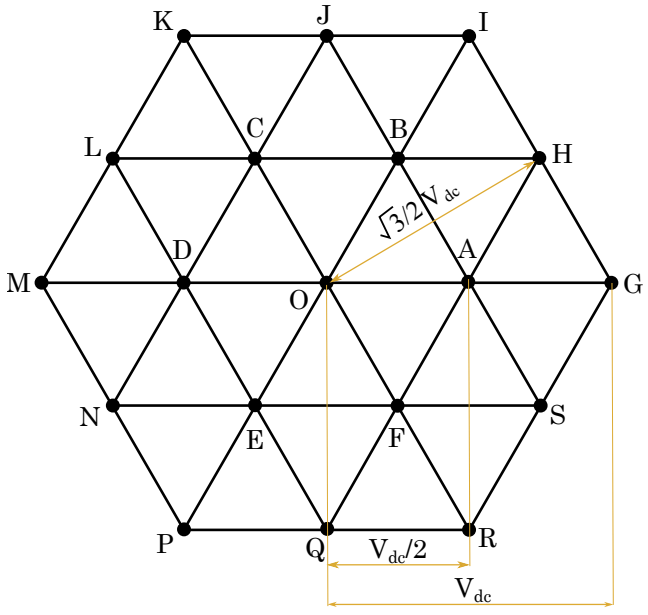


Figure 2.5: Space vector for dual two-level inverter.

There have been various modulation techniques suggested in the literature for the efficient multilevel operation of dual inverter drive [71], [117]–[121]. The modulation in dual inverter can be synthesized either by space vector modulation (SVM) or CBM technique. The latter is proven to be the simplest and feasible method for digital implementation [79]. The two level carrier-based modulation [76], has been extended to multilevel inverters with the level shifted carriers in phase disposition. This carrier arrangement gives the better harmonic results [79]. The carriers are placed in contiguous band and the total height of the carrier band denotes the available DC-link voltage (V_{dc}) in dual two-level inverter. For a three-level operation, the height of each phase disposed carrier will be $V_{dc}/2$. The modulating waves, when compared with high frequency level shifted carriers, the required gate pulses are generated for the top devices of Inverter-1 and Inverter-2, whereas bottom devices will be switched in complimentary to the top devices of each half-bridge leg. Moreover the comparison logic of the modulating waves with lower carrier is inverted to that of the upper carrier [71], [120].

2.4 Proposed power sharing concept in dual inverter

In EVs, a uniform discharge of the isolated battery packs feeding the dual two-level inverter, is an interesting topic to be surveyed. For this, the power from the isolated DC sources can be regulated by shifting the switching between the two inverters. The power sharing capability of this topology was first reported in [72], [116]. A space vector approach for dual two-level inverter, similar to conventional

three-phase inverter is described in [117]. The control effectively switches each inverter alternatively in a sub-cycle of a switching period. However, this method requires sector identification for switching pattern. Power sharing with optimal DC bus utilization, can be achieved by independent modulation and control of the two inverters using collinear vectors [119]. Due to the switching sequence complexities in digital domain, a modified space vector method is proposed in [122] to attain power sharing control within each switching cycle. However, the complex realization of SVM with effective switching time calculation still exists.

Power sharing using CBM can be more simple and easily implemented. In CBM, the upper carrier generates the switching sequences for Inverter-1, whereas lower carrier generates the sequences for Inverter-2, when both compared to the same triplen harmonic injected (THI) modulating waves. The area for logical comparison in carrier region varies with the modulation index (M) as graphically represented in Fig. 2.6. For clear visualization the carriers in the figures are illustrated at reduced frequency. It may be noted that instantaneous modulating waves has

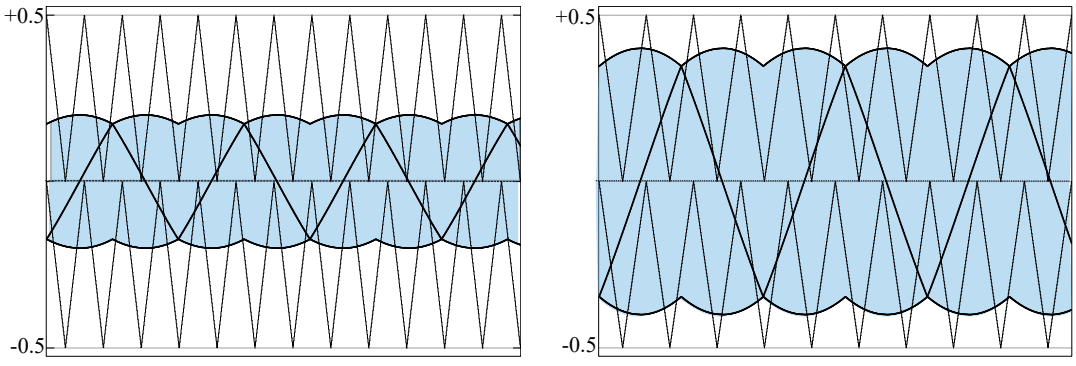


Figure 2.6: Modulating and level shifted carrier waves comparison for three-level PWM. (a) lower M, (b) higher M.

the zero crossing at the center of the carrier band i.e. the modulating waves are uniformly placed in both carriers. Therefore, CBM inherently provides an equal power sharing in an average sense in dual two-level inverter, if the isolated DC sources are maintained at equal SOC. The shaded (blue) segment in Fig. 2.6(a) and 2.6(b) represents the actual region for logical comparison to generate PWM switching in each inverter at different M. If $M < 1$ there are considerable (unshaded) portions still available in both carriers, which may also be utilized for PWM switching. This provides an additional degree of freedom to shift the modulating waves within the carrier limits [123].

A calculated DC offset voltage (V_k) with respect to M, can gradually push the modulating wave in the upper carrier or lower carrier as shown in Fig. 2.7. A positive V_k will shift the zero crossing of the modulating waves in the upper carrier and a negative V_k will shift the zero crossing in the lower carrier. When M is small, it can be clearly seen that the modulating waves can be conveniently placed in any one carrier. The darker shade (purple) in Fig. 2.7(a) and 2.7(a) represents that the entire switching shifted to one of the two-level inverter. This leads to the possibility of power flow from any one inverter in dual two-level inverter. When M is high as shown in Fig. 2.7(c) and 2.7(d), the modulating waves can be unequally displaced in each carriers based on the offset values applied and the switching will be more in the inverters associated with the darker shaded (purple) segment in carrier region. Therefore, the power flow between the inverters can be conveniently manipulated with the offsetting.

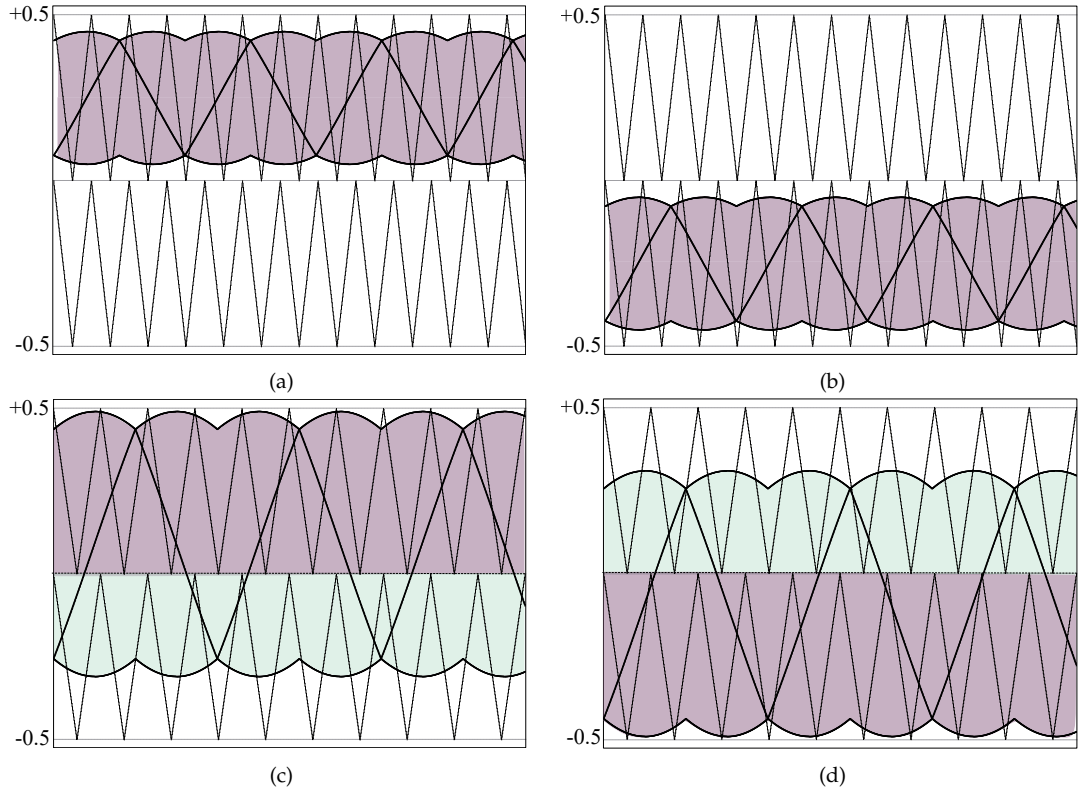


Figure 2.7: Modulating waves moved in the upper and lower carriers for different M. (a) lower M with positive V_k, (b) lower M with negative V_k, (c) higher M with positive V_k, (d) higher M with negative V_k.

The power sharing in dual inverter due to the applied offset, can be analyzed using the Fourier series of output voltage. For evaluation, the sinusoidal reference of phase-A_1A_2 can be considered as shown in Fig.2.8. When an offset is applied, the darker shaded (purple) portion of the fundamental output voltage will be produced by one of the inverter where as the lighter shaded (green) portion is produced by the other inverter. In the figure, the original horizontal reference of the phase voltage is represented in dotted line and the new position of the horizontal reference due to the applied offset V_k is shown in solid line. α is the position of new zero crossing in the output voltage. To simplify the analysis, the origin of the

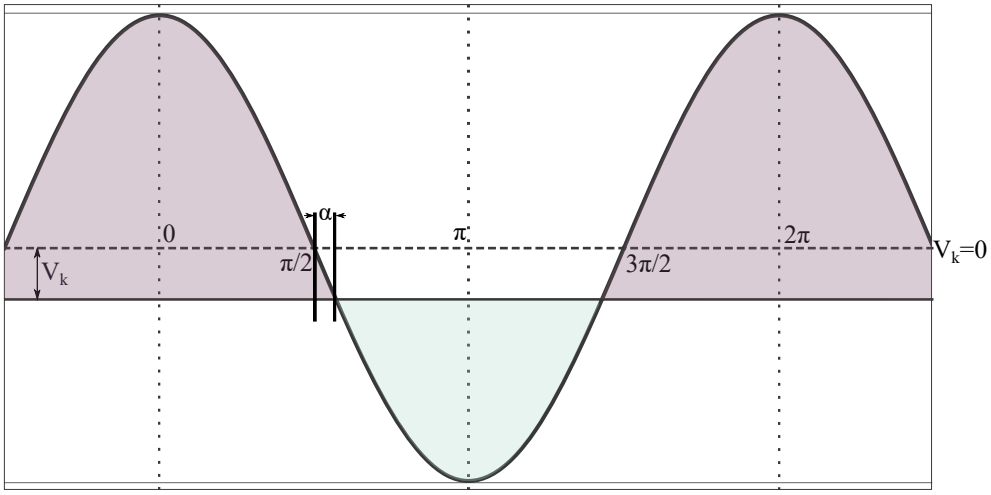


Figure 2.8: Fundamental component of the output voltage in phase-A_1A_2 of dual two-level inverter.

fundamental wave is chosen to get a cosine function. The relation of the output voltage wave with V_k can be expressed as below:

$$v_o(t) = \frac{M}{2}\cos\omega t + k \tag{2.8}$$

where M is the modulation index and k is the normalized value of offset voltage V_k. The voltage waveform seen by each inverter has fundamental and it's odd harmonics. For the power sharing in EV system, the instantaneous SOCs of the battery packs are considered. Since the SOC changes based on the average DC-link current which in turn depends only on the fundamental voltage, only the fundamental component of the output voltage need to be considered. Due to the symmetry of the waveform, the fundamental component seen by Inverter-1 can be written as below:

$$V_{a_1} = \frac{2}{\pi}\left[\int_0^{\frac{\pi}{2}+\alpha}(\frac{M}{2}\cos\omega t + k)\cos\omega t dt\right] \tag{2.9}$$

Solving (2.9),

$$V_{a_1} = \frac{2}{\pi}\left[\frac{M}{2}\int_0^{\frac{\pi}{2}+\alpha}\cos^2\omega t dt + k\int_0^{\frac{\pi}{2}+\alpha}\cos\omega t dt\right] \tag{2.10}$$

On applying the limits and simplification,

$$V_{a_1} = \frac{2}{\pi}\left[\frac{M}{2}\left(\left(\frac{\pi}{4}+\frac{\alpha}{2}\right)-\left(\frac{sin2\alpha}{4}\right)\right)+kcos\alpha\right] \tag{2.11}$$

Since variation in k is very small, (2.11) can be simplified by small angle approximation to get fundamental voltage expressed as below:

$$V_{a_1} = \frac{M}{4} + 2\frac{k}{\pi} \tag{2.12}$$

The fundamental value obtained can be substituted in the input and output power relation and DC-link current can be written as below:

$$I_{dc} = \frac{3V_{a_1}I_o}{V_{dc}}\cos\phi \tag{2.13}$$

where V_{dc} and I_{dc} are dc side voltage and current respectively and I_o is the output phase current. From (2.13), the current and the power from each DC source can be determined. It can be noted from (2.12) and (2.13) that, the input power of each inverter can be varied as a function of offset voltage irrespective of the operating power factor.

2.4.1 Derivation of Offset limits for proposed technique

From the discussion in the above section, it can be concluded that the power can be shared as desired in the dual two-level inverter by application of a common offset voltage (V_k) to the instantaneous modulating wave. The value of V_k could be positive or negative. However, for an effective multilevel waveform and to avoid six step operation, the offset should be limited to retain the modulating wave with in the carrier region. This can be ensured by calculating the V_k as a function of M. From Fig. 2.5, it can be noted that the maximum voltage vector which can be applied is $\sqrt{3}/2V_{dc}$. Hence the modulation M can be expressed as in (2.14):

$$M = \frac{2}{\sqrt{3}} \frac{V_m}{V_{dc}} \tag{2.14}$$

where V_m is the magnitude of the reference voltage vector and V_{dc} is total DC-link voltage in dual two-level inverter. The limit of the offset applied can be obtained as in (2.15):

$$V_{kl} = \pm \frac{(1-M)}{2}; \qquad 0 \leq M \leq 1 \tag{2.15}$$

From (2.15) following inferences can be made:

(i) The maximum value of offset which can be theoretically applied is ± 0.5

(ii) For a $M < 0.5$, the modulating waves can be conveniently shifted to one of the carriers and the inverter related to that carrier will deliver the entire power to the load motor. This can be suitable for implementation in fault conditions, where the modulating wave can be shifted to the carrier corresponding to

the healthy inverter. The other inverter will have zero vector state, which naturally provides a star connection at the other terminals of the motor. Thus the drive can be operated at half speed and power. For $M = 0.5$, the zero crossing of the modulating waves can be placed exactly at the center of any carrier. This is the maximum M for which power can be delivered from one of the inverter.

(iii) $0.5 < M < 1$, both inverters will be feeding the load motor. However, the inverter related to the carrier with larger fraction of modulating waves will be delivering more power to the load motor.

(iv) For $M = 1$, no power sharing will be possible, as the offset will be zero. This would be a very rare scenario in EVs, for a city drive cycle.

2.4.2 Switching Sequence for proposed technique

The switching sequence with offset mechanism can be analyzed by the space vector approach, for which first sectoral triangle, OGI is examined. The required voltage vector is assumed to be at center of each sub-triangle (OAB, AHB, AGH, BHI) as illustrated in middle trace of Fig. 2.9. The top and bottom traces shows the gate switching for the two inverters along with position of modulating waves in a switching cycle when each offsets are applied. The height of each carrier is 0.5 and total switching cycle time is T_s. The gate signals for Inverter-1 and Inverter-2 are represented by g_{A1}, g_{B1}, g_{C1} and g_{A2}, g_{B2}, g_{C2} receptively.

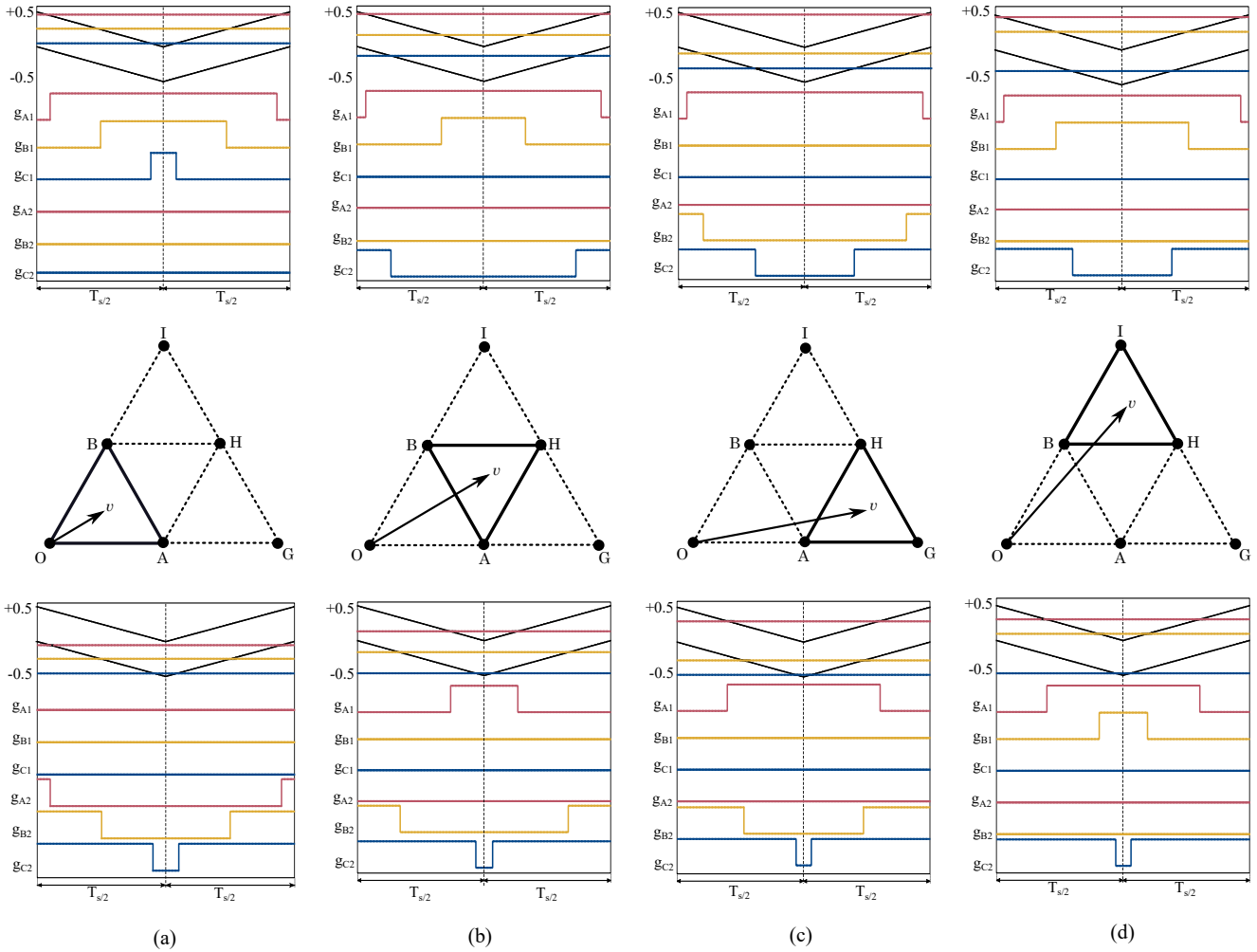


Figure 2.9: Switching pattern for voltage vector in positive and negative offset for first sectoral triangle OGI. (top) Switching pattern for positive V_k, (center) different voltage vector position in sectoral triangle and (bottom) switching pattern for negative V_k. (a) Inner sub-triangle. (b) Middle sub-triangle. (c) and (d) Outer sub-triangles.

When M is small, the required voltage vector v lies in the inner sub-triangle OAB. For both positive and negative offsets, v can be generated by switching vectors of any one inverter, keeping the other one clamped to its zero vector. In the Fig. 2.9(a), it can be noted that the switching pattern is symmetrical for either offset cases, with switching in only one inverter. When the vector is in middle sub-triangle, the switching pattern will be asymmetrical for both offsets. However, there are no overlapping between the active vectors as mentioned in [122]. The sequence of switching in both offsets will be same, when the reference vector is in the outer sub-triangles, AGH and BHI as illustrated in Fig. 2.9(c) and Fig. 2.9(d). However, the time duration of the active vectors and the zero vector will change with applied positive and negative offsets. Overall, it can be noted that the commutation in a switching cycle is minimum for each sub-triangles. The switching sequence shown in Fig. 2.9 is shown in tabular form in 2.1.

Table 2.1: Switching states for applied offset in first sector.

	Switching vectors	
Sub triangle	Upper offset	Lower offset
OAB	88′, 18′, 28′, 78′	87′, 84′, 85′, 88′
AHB	85′, 15′, 18′, 28′	84′, 85′, 15′, 18′
AGH	84′, 14′, 15′, 18′	84′, 14′, 15′ , 18′
BHI	85′, 15′, 25′, 28′	85′, 15′, 25′, 28′

2.5 Conclusion

This chapter proposes a very simple carrier based modulation technique for power sharing between the isolated DC sources, in a dual two-level inverter. The individual level shifted carriers compared to the modulating waves corresponds to the switching in each inverter. The modulating waves will be equally displaced in each carrier when they are placed at the center of carrier band, providing an equal sharing between the inverters. In linear modulation range, an offset can be applied to shift the modulating waves within the carrier region. This will cause a change in switching in each inverter based on the position of the modulating wave. The value of applied offset depends on the instantaneous modulation index M. When $M < 0.5$, the modulating waves can be placed in any one carrier and the inverter corresponding to the respective carrier can be made to deliver the entire power to the load. This will cause other inverter to be naturally clamped to its zero vectors, which could be an attractive solution for fault tolerant application without the use of any external circuit. When $M > 0.5$, the carrier which has the larger portion modulating waves will provide more switching in the corresponding inverter, causing more power flow to the load than the other inverter. The applied offset will not affect the normal operation of the drive as the nearest three switching vectors are always applied as seen from the switching sequences. The proposed modulation technique is a viable alternative for power sharing without a space vector approach and with reduced digital implementation complexities. The next chapter extends the simulation study and experimental analysis of the proposed power sharing modulation.

Chapter 3

Simulation and experimental results of power sharing modulation

3.1 Introduction

A conventional CBM technique can be modified with offset mechanism to provide power sharing in dual two-level inverter drive as discussed in Chapter 2. The proposed power sharing method can be feasibly implemented, without digital and circuit complexities in the dual inverter fed EV drive.

In this chapter a detailed simulation and experimental validation are provided for the proposed power sharing modulation technique. Block diagram representations illustrate the implementation of the proposed PWM techniques in dual inverter drive for EV. From the results, it is evident that the proposed technique can effectively regulate the power drawn between the two two-level inverters while maintaining the multilevel operation of the drive. The modulation technique can

balance the instantaneous state of charge (SOC) of independent battery packs and dynamically control the power flow from the two inverters. This will enhance reliability, robustness, and improve the battery life in an EV system. An open-end induction motor of 5.6 kW is used as the three phase load for dual inverter drive. The control algorithm is implemented on Texas Instruments DSP controller. For analyzing the performance of the proposed power sharing technique for different driving schedules, a hardware-in-loop (HIL) system was also developed using OPAL-RT simulator.

3.2 Experimental block diagram

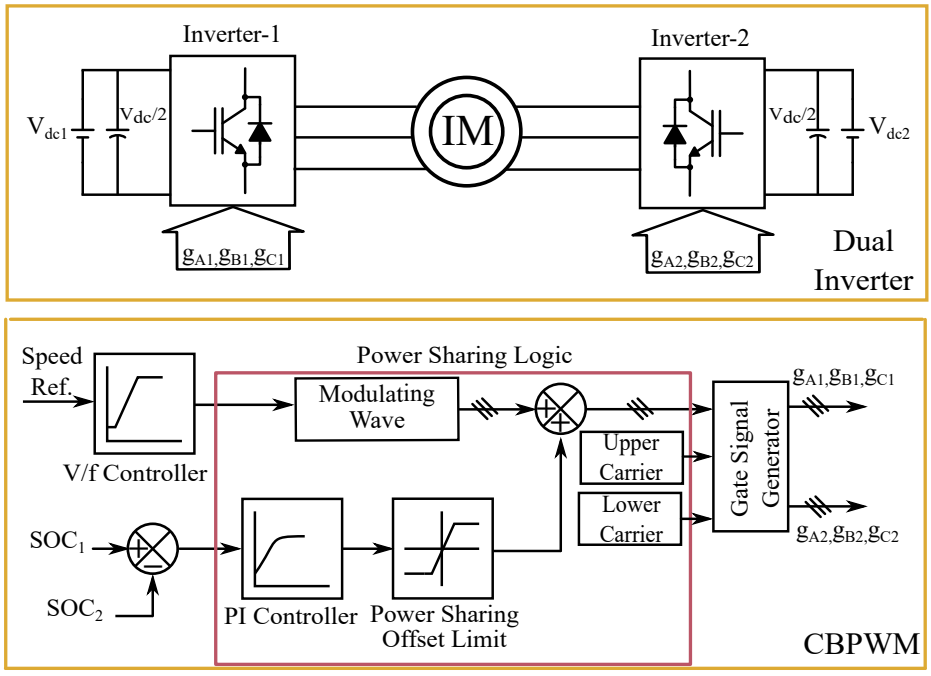
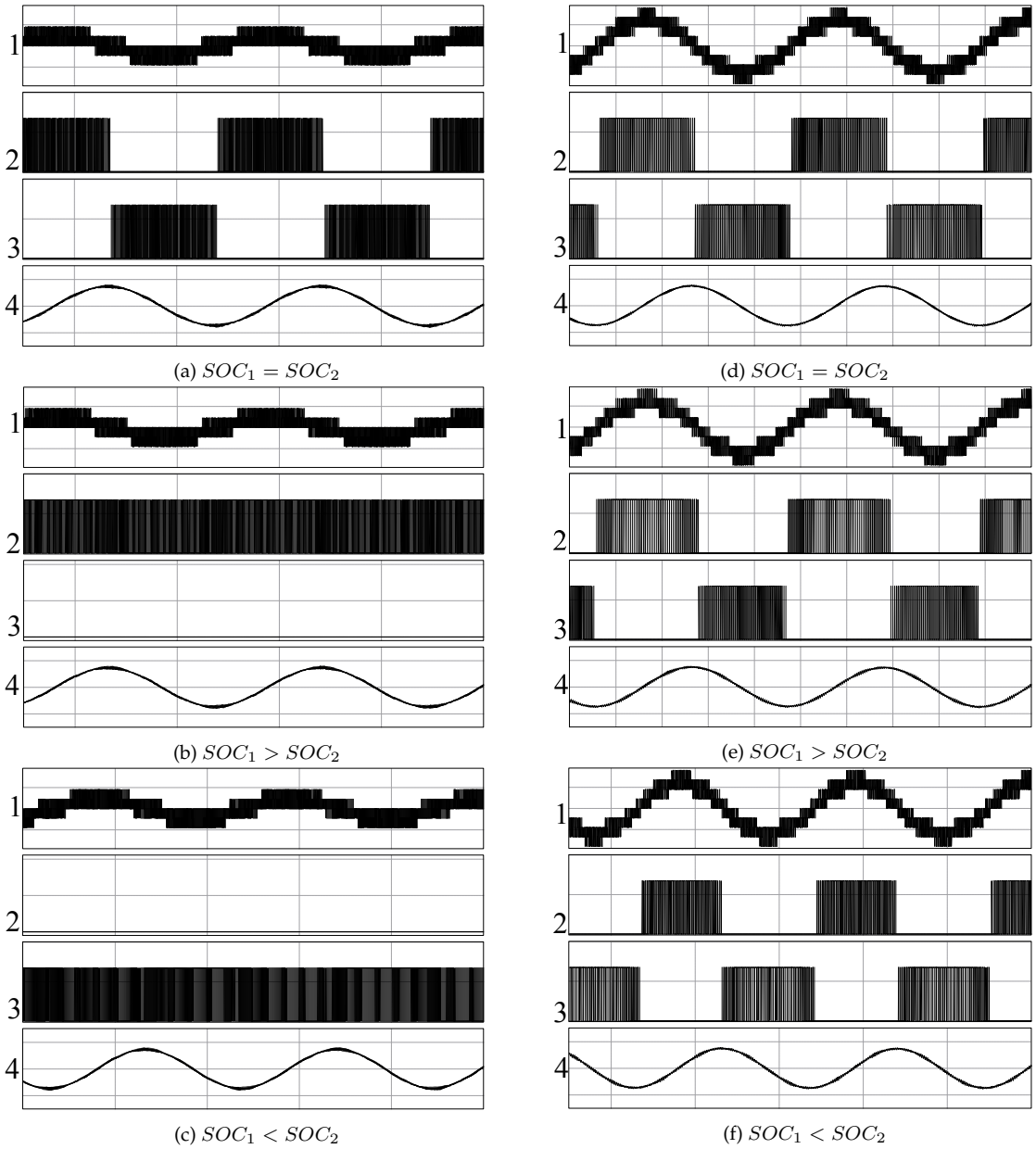


Figure 3.1: Block diagram for the proposed power sharing scheme in a dual two-level inverter drive.

The block diagram in Fig. 3.1 shows the implementation of power regulation in a dual two-level inverter drive. The value of V_k is calculated by a simple PI controller, input to which is taken as the difference of two battery SOCs. For experimental validation, SOCs are taken as the difference of two DC-link voltages. Since the SOCs of the batteries change at a slower rate, a controller with higher time constant will be sufficient to apply a slowly varying offset to the modulating waves. For any SOC error, controller will provide an offset value, which will unequally split the fundamental produced by two inverters. The limit of the PI controller is fixed by equation (2.15) in Chapter 2. The fundamental frequency of the system is 60 Hz and the carrier frequency is fixed at 3 kHz. The voltage level at DC-links of dual two-level inverter, for both simulation and hardware implementation is kept at 135 V.

3.3 Simulation results

The proposed modulation scheme is simulated in PLECS and MATLAB/simulink on an open-end induction motor using V/f control and the steady state results for different frequencies are obtained. The simulation results are shown in Fig. 3.2 for different frequencies. Fig. 3.2(a) to 3.2(c) shows the operation of dual two-level inverter at 24 Hz for different SOCs in battery pack. At lower frequency, when $M < 0.5$, the waveforms corresponds to a two-level inverter operation. For same SOC i.e. $SOC_1 = SOC_2$, there will be no offset. However, for unequal conditions, when $SOC_1 > SOC_2$ or vice versa, the required positive or negative offset value is applied by the controller to shift the modulating wave either in upper or lower



(a) $SOC_1 = SOC_2$ (d) $SOC_1 = SOC_2$

(b) $SOC_1 > SOC_2$ (e) $SOC_1 > SOC_2$

(c) $SOC_1 < SOC_2$ (f) $SOC_1 < SOC_2$

Figure 3.2: Simulation results of proposed sharing technique.
(a), (b) and (c) operation at 24 Hz (X-axis; 20 ms/div).
(d), (e) and (f) operation at 48 Hz (X-axis; 10 ms/div).
(a), (b), (c), (d), (e) and (f): (1) phase voltage (100 V/div), (2) pole voltage ($V_{A_1O_1}$) (100 V/div), (3) pole voltage ($V_{A_2O_2}$) (100 V/div), (4) phase current (1 A/div).

carrier region. From the waveforms of 24 Hz operation, it can be observed that the phase voltage and phase current are not changed and any one inverter can feed the load motor. Similarly, Fig. 3.2(d) to 3.2(f) shows the operation of the system at 48 Hz frequency. It can be seen that in equal and unequal condition of SOC_1 and SOC_2, the modulation scheme can produce a proper multilevel voltage waveform, keeping the phase current unchanged in each offset condition. This explicitly shows that the implementation of V_k has not modified the operation of dual two-level inverter.

The normalized harmonic spectrum (Fast Fourier Transform (FFT)) of the phase voltage is shown in Fig. 3.3 for the frequencies studied in simulation. The harmonic spectrum has been calculated to the maximum frequency of 3 kHz. Fig. 3.3(a) to 3.3(c) and Fig. 3.3(d) to 3.3(f) shows the voltage harmonic spectrum for 24 Hz and 48 Hz respectively. It can be seen that there is not much variation in harmonic spectrum for the different offset applied and all the harmonic components are around the switching frequency of the dual inverter. The percentage of weighted total harmonic distortion (WTHD) for different frequencies is summarized in Table 3.1. The WTHD for either of the offsets is the same. Moreover, the WTHD difference

Table 3.1: Weighted THD of phase voltage

	WTHD (%)		
Frequency (Hz)	No Offset	Positive Offset	Negative Offset
12	0.18	0.29	0.29
24	0.19	0.23	0.23
36	0.15	0.19	0.19
48	0.1	0.25	0.25
54	0.13	0.20	0.20

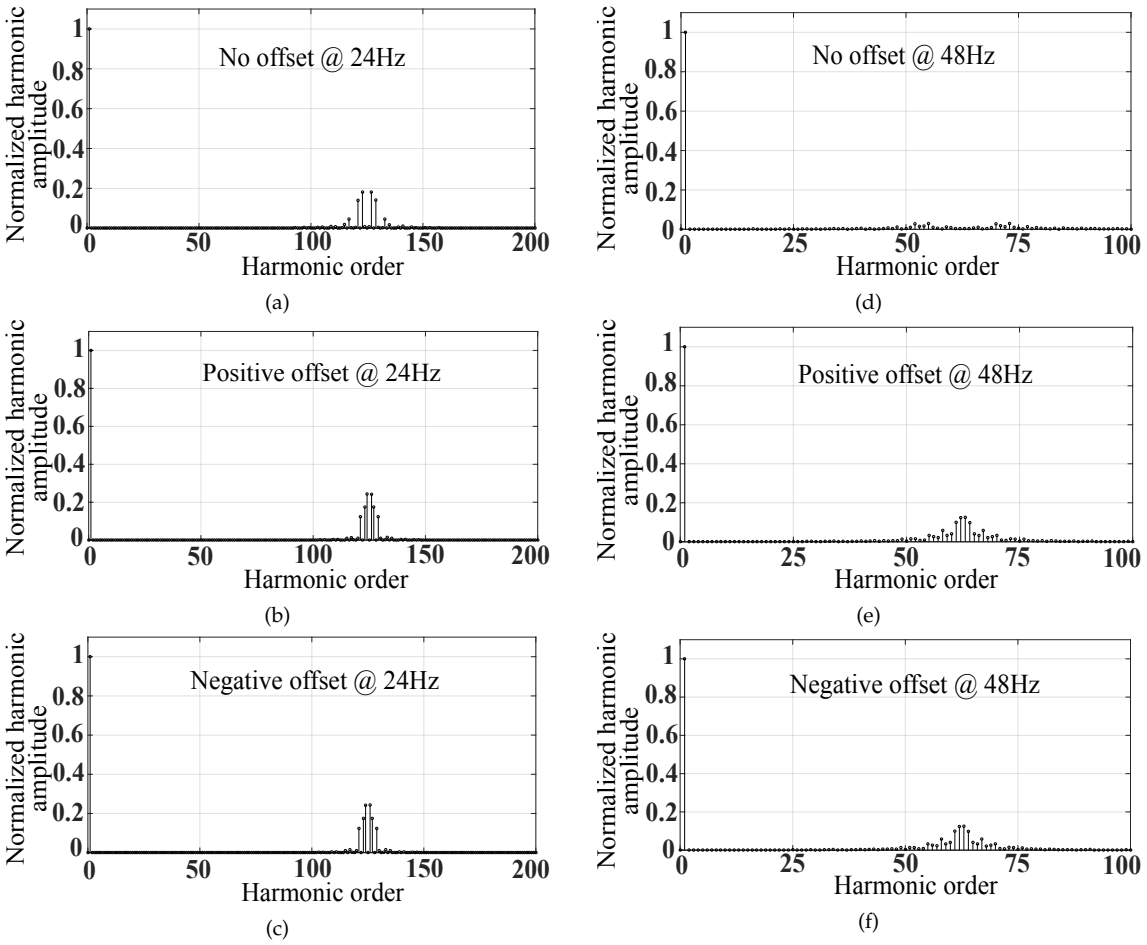


Figure 3.3: FFT of phase voltage with and without offset V_k. (a), (b) and (c) FFT spectrum at 24 Hz. (d), (e) and (f) FFT spectrum at 48 Hz.

between with and without offset case is negligible. Hence there will be no adverse effect in the system performance if the offsets are applied.

The effectiveness of the PWM due to the offsets can be evaluated from the switching losses in the dual two-level inverter. The Fig. 3.4 shows the switching loss for various fundamental frequencies in different offsets. The characteristics of IGBT switch (SKM50GB12T4) is modeled in PLECS and the average switching loss is computed for with and without offset conditions. It is evident from the graph

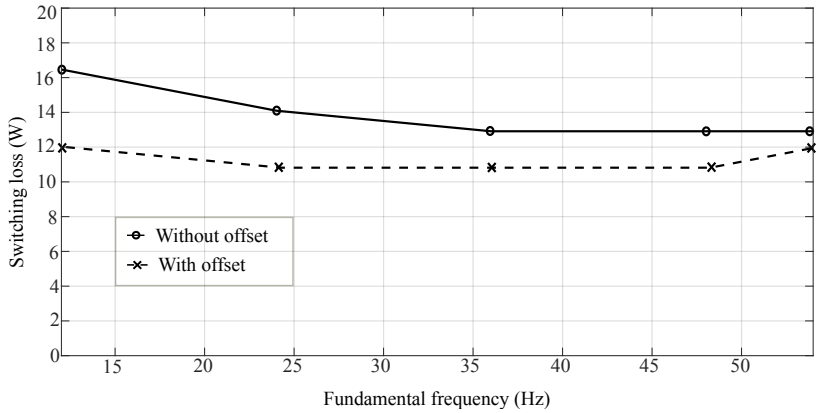
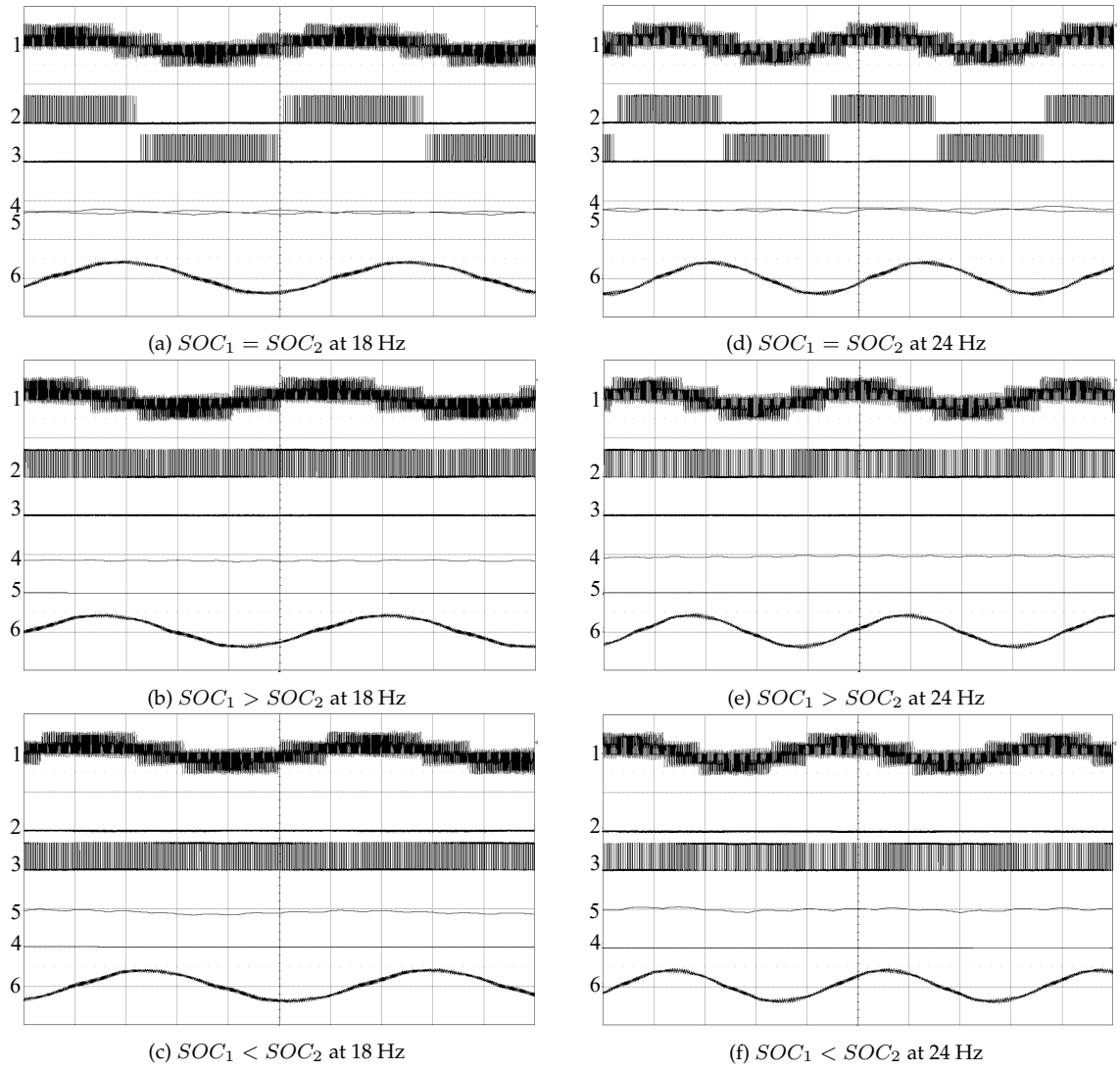


Figure 3.4: Switching loss comparison, with and without offset.

that overall switching loss will be lower when the offsets are applied, as the switching has been reduced in one of the inverter. At rated speed, the losses will become equal, as the offsets cannot be applied.

3.4 Experimental results

In hardware experiment, the dual inverter system is build using conventional two-level inverter stacks, connected to a 5.6 kW open-end induction motor. The proposed modulation technique is digitally implemented on TMS320F28069M, DSP controller kit with 90 MHz clock frequency. The motor is driven at no load and the waveforms are taken at different steady state and dynamic conditions. The power flow in the system is validated through the average DC currents, I_{dc1} and I_{dc2} and the pole voltages $V_{A_1O_1}$ and $V_{A_2O_2}$ of Inverter-1 and Inverter-2 respectively. Fig. 3.5(a) to 3.5(c) shows the performance of the drive at 18 Hz. Fig. 3.5(d) to 3.5(f) shows the performance of the drive at 24 Hz. When the SOCs are same, equal



(a) $SOC_1 = SOC_2$ at 18 Hz

(d) $SOC_1 = SOC_2$ at 24 Hz

(b) $SOC_1 > SOC_2$ at 18 Hz

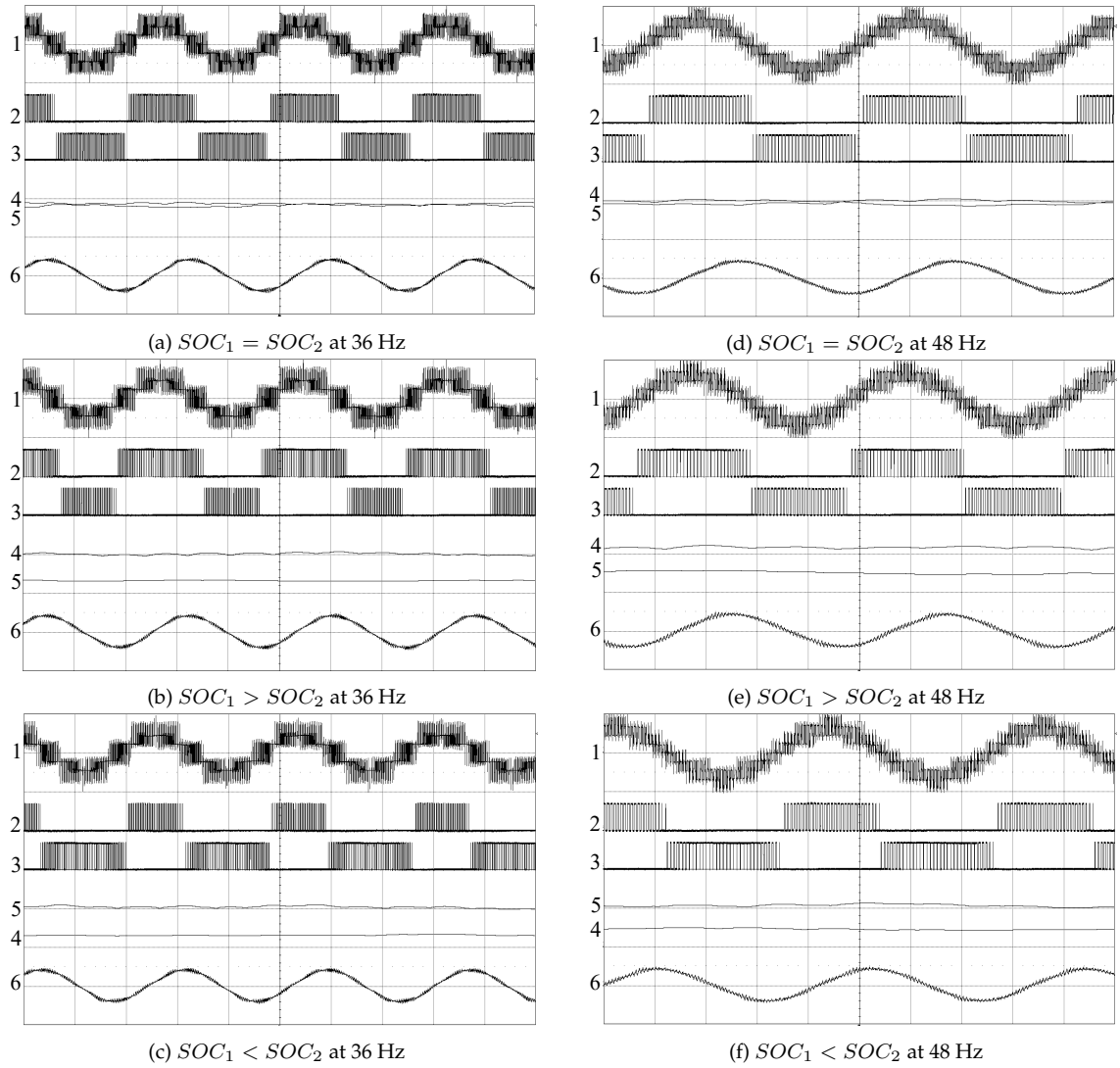
(e) $SOC_1 > SOC_2$ at 24 Hz

(c) $SOC_1 < SOC_2$ at 18 Hz

(f) $SOC_1 < SOC_2$ at 24 Hz

Figure 3.5: Experimental results of proposed sharing technique at lower M.
(a), (b) and (c) operation at 18 Hz (X-axis; 10 ms/div).
(d), (e) and (f) operation at 24 Hz (X-axis; 10 ms/div).
(a), (b), (c), (d), (e) and (f): (1) phase voltage (200 V/div), (2) pole voltage ($V_{A_1O_1}$) (200 V/div), (3) pole voltage ($V_{A_2O_2}$) (200 V/div), (4) DC current (I_{dc1}) (1 A/div), (5) DC current (I_{dc2}) (1 A/div), (6) phase current (5 A/div).

DC current will be drawn from the isolated sources. Hence the power to the load will be shared by both the inverters evenly. For $SOC_1 > SOC_2$, a positive V_k is applied by the controller and the pole voltage will be generated by Inverter-1 alone as



(a) $SOC_1 = SOC_2$ at 36 Hz

(d) $SOC_1 = SOC_2$ at 48 Hz

(b) $SOC_1 > SOC_2$ at 36 Hz

(e) $SOC_1 > SOC_2$ at 48 Hz

(c) $SOC_1 < SOC_2$ at 36 Hz

(f) $SOC_1 < SOC_2$ at 48 Hz

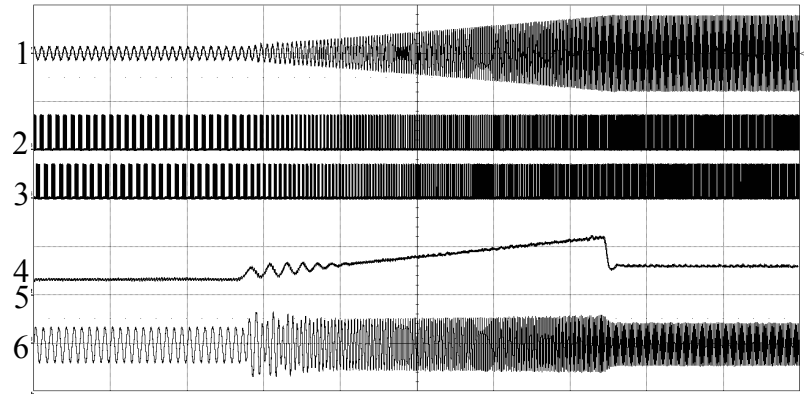
Figure 3.6: Experimental results of proposed sharing technique at higher M.
(a), (b) and (c) operation at 36 Hz (X-axis; 10 ms/div).
(d), (e) and (f) operation at 48 Hz (X-axis; 5 ms/div).
(a), (b), (c), (d), (e) and (f): (1) phase voltage (200 V/div), (2) pole voltage ($V_{A_1O_1}$) (200 V/div), (3) pole voltage ($V_{A_2O_2}$) (200 V/div), (4) DC current (I_{dc1}) (1 A/div), (5) DC current (I_{dc2}) (1 A/div), (6) phase current (5 A/div).

shown in Fig. 3.5(b) and Fig. 3.5(e). In the figures, I_{dc2} and $V_{A_2O_2}$ are zero, therefore no power is drawn from Inverter-2 rather from Inverter-1 and the dual two-level inverter works as conventional three-phase inverter. The reverse will happen when

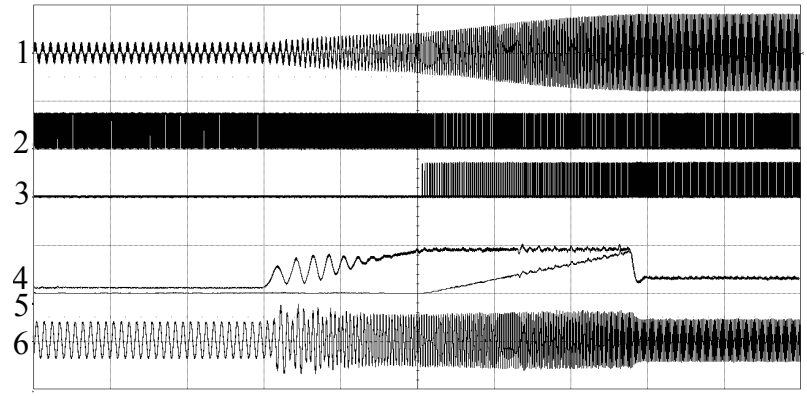
$SOC_1 < SOC_2$ as shown in Fig. 3.5(c) and Fig. 3.5(f). It can be noted that there is no dissimilarity in phase voltage and the phase current in all cases.

Fig. 3.6 shows the performance of the drive for multilevel operation. Fig. 3.6(a) to 3.6(c) shows the operation for 36 Hz and Fig. 3.6(d) to 3.6(f) shows the operation for 48 Hz. Again, for equal SOC, the motor load is equally fed from both inverters. For $SOC_1 > SOC_2$, more I_{dc1} will be drawn than I_{dc2}, and Inverter-1 pole voltage switching will be comparatively more than the other, causing Inverter-1 to feed more power to the motor load. The opposite will happen when $SOC_1 < SOC_2$ as shown in 3.6(c) 3.6(f). It may be noted that the multilevel operation remains the same, without altering the phase current.

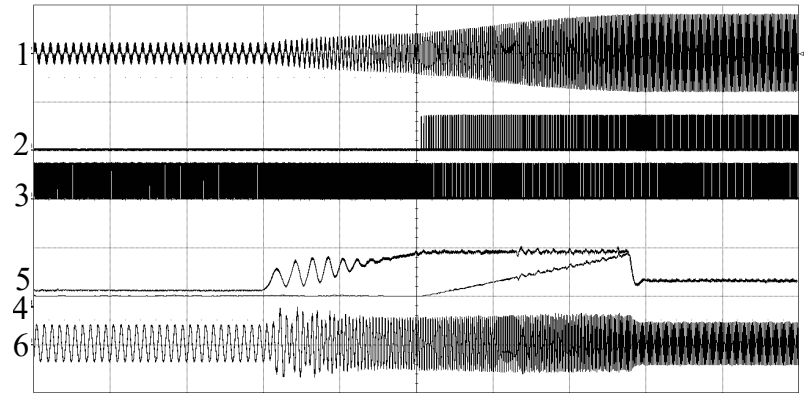
Fig. 3.7(a) to 3.7(c) shows the acceleration profile of the motor, with speed range from 10 to 60 Hz, keeping equal and unequal SOCs. It may be noted that, in equal SOCs, both inverters will take equal amount of DC current from the sources during the acceleration. However for $SOC_1 > SOC_2$ and $SOC_1 < SOC_2$, one of the inverter draws more current at lower speeds. The current is gradually taken from the other inverter as the speed increases, hence facilitating the smooth acceleration of the drive.



(a) $SOC_1 = SOC_2$



(b) $SOC_1 > SOC_2$



(c) $SOC_1 < SOC_2$

Figure 3.7: Acceleration results from 10 Hz to 60 Hz.
(a), (b) and (c) operation at full acceleration (X-axis; 1 s/div).
(1) phase voltage (200 V/div), (2) pole voltage ($V_{A_1O_1}$) (200 V/div), (3) pole voltage ($V_{A_2O_2}$) (200 V/div), (4) DC current (I_{dc1}) (2 A/div), (5) DC current (I_{dc2}) (2 A/div), (6) phase current (5 A/div).

3.5 Hardware-in-loop implementation

The suitability of the proposed power sharing scheme in standard drive cycles is examined using HIL with OP4510 real-time simulator as shown in Fig. 3.8. The dual two-level inverter, two battery packs and a medium sized electric vehicle are modeled in RT-LAB and the embedded system is implemented in DSP kit. A conventional field oriented controller is implemented to change the speed of the motor for the driving schedule. The parameters of motor and medium-sized vehicle is shown in Appendix B. The experiments are performed with and without the power sharing logic in different driving profiles like FTP-72 (UDDS-505 sec), ECE-15 cycle (UDC-195 Sec), 10-3 Mode cycle Japan (405 Sec) [124]. The results are obtained by post processing in MATLAB.

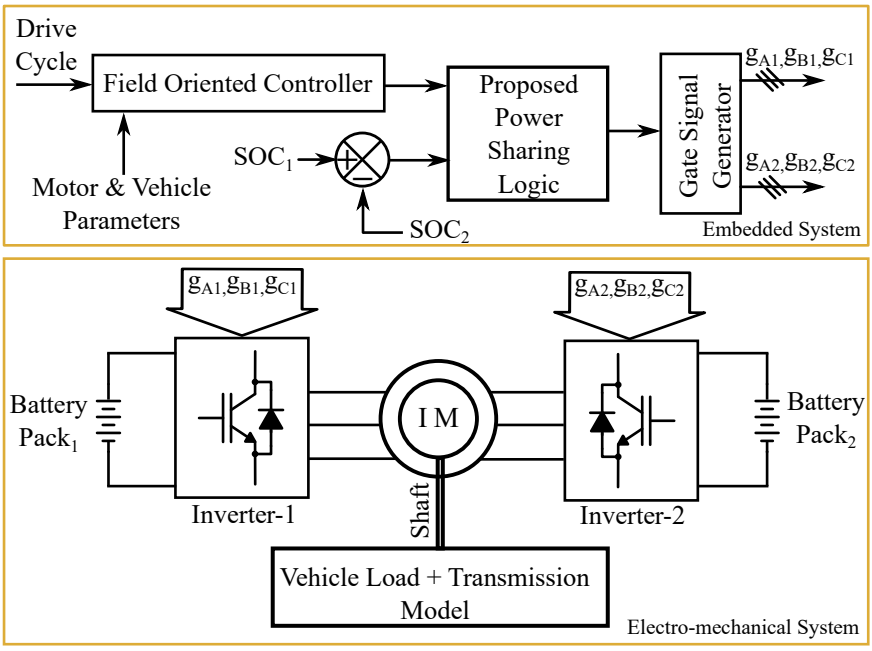
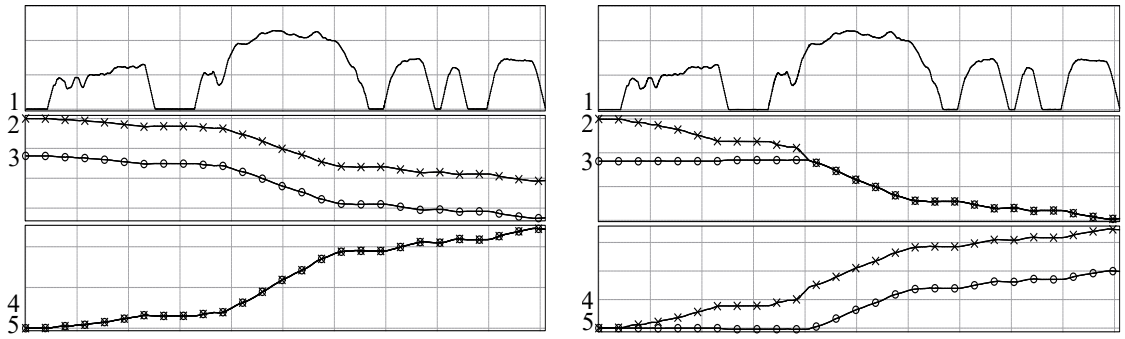


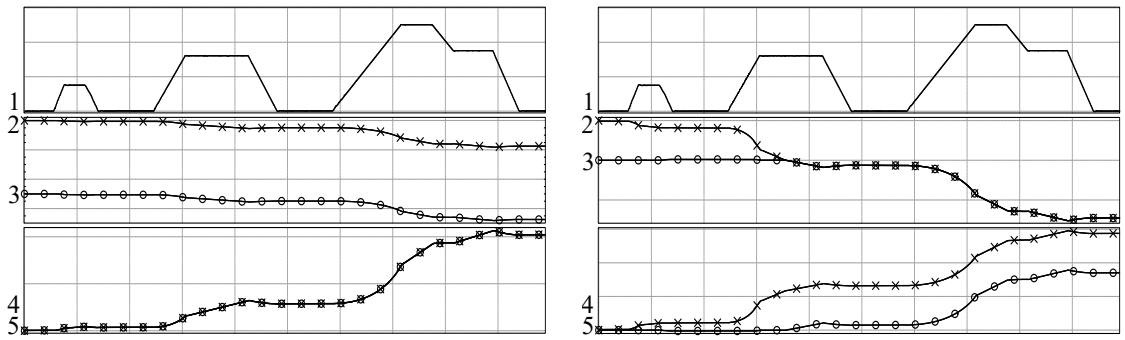
Figure 3.8: Block diagram for the proposed power sharing scheme using HIL.

Fig. 3.9 to Fig. 3.11 shows the results for unequal SOCs and Fig. 3.12 to Fig. 3.14 shows results for unequal battery capacity (Ampere hour or Ah rating) for various driving profiles. In figures SOC and coulomb count of battery pack$_1$ (SOC_1, CC_1) is represented by $'\times'$ and that of battery pack$_2$ by $'\circ'$. In Fig. 3.9 to Fig. 3.11, it can be observed that, without power sharing logic, when the battery packs have different SOCs ($SOC_1 > SOC_2$), both packs are getting discharged simultaneously in each driving cycle. Moreover, equal amount of power is taken from both DC sources as



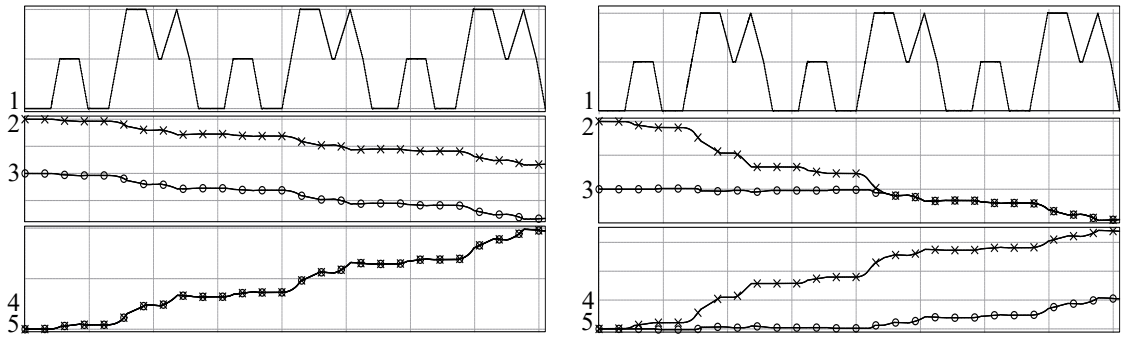
(a) Unequal SOC without power sharing for FTP-72. (b) Unequal SOC with power sharing for FTP-72.

Figure 3.9: FTP-72 driving cycle results for unequal SOC. (a) and (b) (X-axis 50 s/div):(1) vehicle speed (40 km/h/div), (2) SOC_1 (2%/div), (3) SOC_2 (2%/div), (4) CC_1 (2000 C/div), (5) CC_2 (2000 C/div).



(a) Unequal SOC without power sharing for ECE-15. (b) Unequal SOC with power sharing for ECE-15.

Figure 3.10: ECE-15 driving cycle results for unequal SOC. (a) and (b) (X-axis 20 s/div): (1) vehicle speed (20 kmh/div), (2) SOC_1 (1%/div), (3) SOC_2 (1%/div), (4) CC_1 (1000 C/div), (5) CC_2 (1000 C/div).

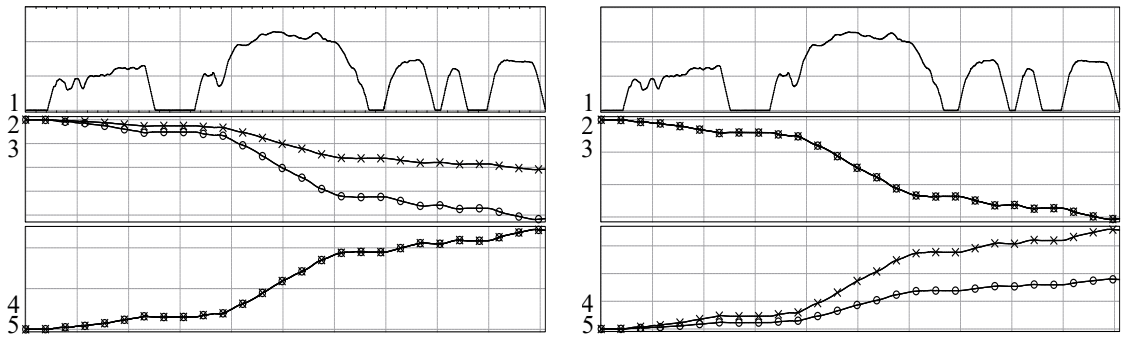


(a) Unequal SOC without power sharing for 10-3 Mode Japan.

(b) Unequal SOC with power sharing for 10-3 Mode Japan.

Figure 3.11: 10-3 Mode Japan driving cycle results for unequal SOC. (a) and (b) (X-axis 50 s/div): (1) vehicle speed (20 kmh/div), (2) SOC_1 (2%/div), (3) SOC_2 (2%/div), (4) CC_1 (2000 C/div), (5) CC_2 (2000 C/div).

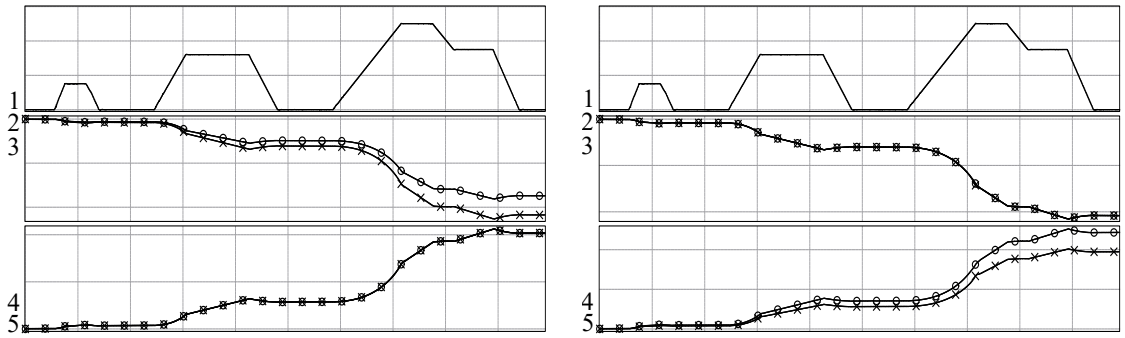
evident from the coulomb count graph. This may cause battery pack$_2$ to discharge at faster rate than the pack$_1$. When the sharing logic is applied, SOC_2 is almost constant for initial part of the cycle, while SOC_1 is getting reduced. This shows that more power has been fed from the battery pack$_1$ due to higher SOC in it. Due to this the coulomb count, CC_1 will be more than the CC_1 in all cycles. Later, the SOCs are getting balanced and the two packs are discharged uniformly.



(a) Unequal capacity without power sharing for FTP-72.

(b) Unequal capacity with power sharing for FTP-72.

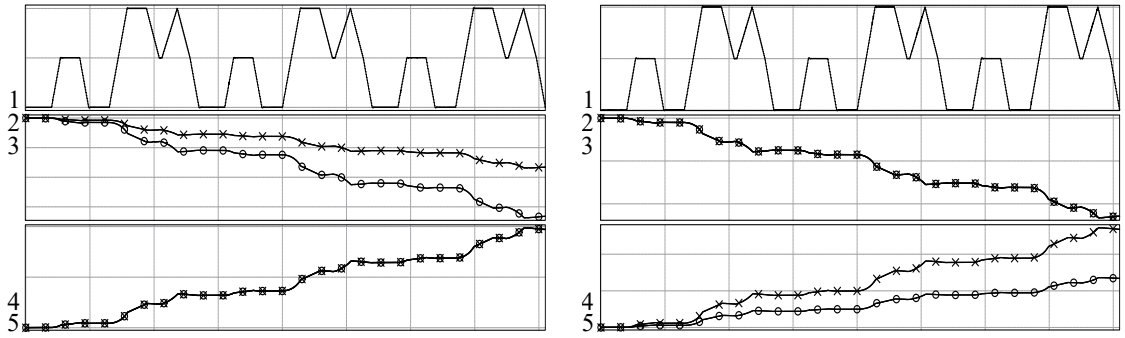
Figure 3.12: FTP-72 driving cycle results for unequal capacity. (a) and (b) (X-axis 50 s/div):(1) vehicle speed (40 km/h/div), (2) SOC_1 (2%/div), (3) SOC_2 (2%/div), (4) CC_1 (2000 C/div), (5) CC_2 (2000 C/div).



(a) Unequal capacity without power sharing for ECE-15.

(b) Unequal capacity with power sharing for ECE-15.

Figure 3.13: ECE-15 driving cycle results for unequal capacity. (a) and (b) (X-axis 20 s/div): (1) vehicle speed (20 kmh/div), (2) SOC_1 (1%/div), (3) SOC_2 (1%/div), (4) CC_1 (1000 C/div), (5) CC_2 (1000 C/div).



(a) Unequal capacity without power sharing for 10-3 Mode Japan.

(b) Unequal capacity with power sharing for 10-3 Mode Japan.

Figure 3.14: 10-3 Mode Japan driving cycle results for unequal capacity. (a) and (b) (X-axis 50 s/div): (1) vehicle speed (20 kmh/div), (2) SOC_1 (2%/div), (3) SOC_2 (2%/div), (4) CC_1 (2000 C/div), (5) CC_2 (2000 C/div).

In Fig. 3.12 to Fig. 3.14, the same system is analyzed with the battery packs having sightly different Ah capacities. It can be seen that, without sharing logic, amount of power fed from both packs is same and the SOCs are not equal. However, when the sharing technique is applied, the SOCs are balanced for complete cycle in each driving profile and CC_1 is higher than the other. This demonstrates that the source with higher capacity is providing more power to the load motor.

3.6 Conclusion

In this chapter the proposed power sharing PWM technique for a dual two-level inverter is extensively validated by simulating in PLECS and MATLAB. The steady state performances of the proposed technique are experimentally verified in hardware, using V/f drive. A simple PI controller with higher time constant is used to obtain the offset value. The difference in SOCs is used as the input to the controller and the limit is fixed by the modulation index M. From the results it can be observed that applied offset provides power regulation without affecting the normal operation of the drive both in lower and higher modulation indexes. When $M < 0.5$, any one inverter in dual inverter can be made to deliver the entire power to the load motor. This would be beneficial for a fault tolerant operation in EV drive. When $M > 0.5$, more can be fed from the inverter in which the DC source has higher SOC or power capacity. The effectiveness of the proposed modulation technique for vehicular application is envisaged through driving schedule test using FOC drive. The results shows that the modulation technique is capable of dynamic SOC balancing when the charge and capacities are different at the isolated DC sources. This would be beneficial for mass transit application where one DC source can be fed from higher capacity energy storage element.

The next chapter discuss the analysis of current ripple in motor when the power sharing is different in the dual two-level inverter fed from isolated DC sources.

Chapter 4

Current ripple analysis for different power sharing ratio in dual inverter

4.1 Introduction

A dual two-level inverter feeding an open-ended motor, is a feasible solution for traction application. The topology supplied from isolated DC sources has power sharing and independent modulation capability as discussed in the previous chapter. This sharing capability could be suitably used in vehicular application for a reliable and fault tolerant operation. Different PWM techniques are suggested in literature to control the power flow from each inverter and provide an effective multilevel operation [115].

The PWM techniques play a vital role in the overall performance of the inverter drive. Therefore evaluation of these techniques will be crucial to study the quality

of output waveforms produced by the inverter [125]. In VSI, voltage is the parameter which is being controlled, and non-sinusoidal output voltage will result in current distortions. Due to associated losses, output power etc, it is important to analyze the current which is detrimental for drive performance [36], [74]. A frequency domain method can be used to determine the harmonic distortions in the motor phase current waveform. However, calculating individual frequency component could be complex [126]. Alternatively, a time domain method can be used, in which the waveform quality can be conveniently scrutinized by predicting the ripple content in motor current [125], [127]. Moreover, the knowledge of ripple content can be used to estimate the torque ripple due to switching as well as the peak current. The latter is used for designing the protection circuitries in the drive systems [128], [129]. Several methods have been suggested in the publications to estimate and reduce the effect of output current ripple for conventional three phase inverters [130]–[132], which were extended for multiphase [133], [134] and multilevel inverters [135]–[138].

Due to structural similarity with the conventional three phase inverter, the current ripple in dual two-level inverter topology has also been extensively investigated. A theoretical approach has been reported in [139], to determine the root mean squared current ripple for different PWM variants. It was suggested that the ripple in dual two-level inverter can be reduced with discontinuous PWM technique. A concept of pivot voltage vector and its switching duty cycle can be used to estimate the instantaneous current ripple in three-level inverter, as presented in [140]. A similar method has been used for dual two-level inverter to evaluate its peak current ripple for centered PWM techniques [141]. In the above literatures,

the authors emphasized on the ripple analysis for equal power sharing ratio, i.e. when both inverters share the load power equally. However, the effect of the modulation schemes on the current ripple with varying power sharing ratio has not been presented yet.

This chapter presents an analytical study on output current ripple for power regulation based on CBM techniques. The ripple analysis is based on the error voltage vector, which is applied by different PWM techniques for varied power sharing ratios. The analysis is performed for continuous and discontinuous switching schemes in a linear modulation range. The current ripple trajectory and peak to peak ripple current are plotted in a complex plane. A detailed derivation of estimating peak to peak current ripple in dual two-level inverter is also provided. It has been shown that the current ripple changes when the power sharing ratio is changed. The results, to validate the analysis has been obtained using MATLAB/Simulink and real time simulator. Based on the discussion, an optimal PWM technique under different sharing condition has been identified.

4.2 PWM techniques for power sharing in dual two-level inverter

The dual two-level inverter fed from isolated DC sources, has higher switching redundancies as shown in Fig. 4.1. Different switching combinations can be used to provide efficient operation in dual two-level inverter drive. The power sharing in

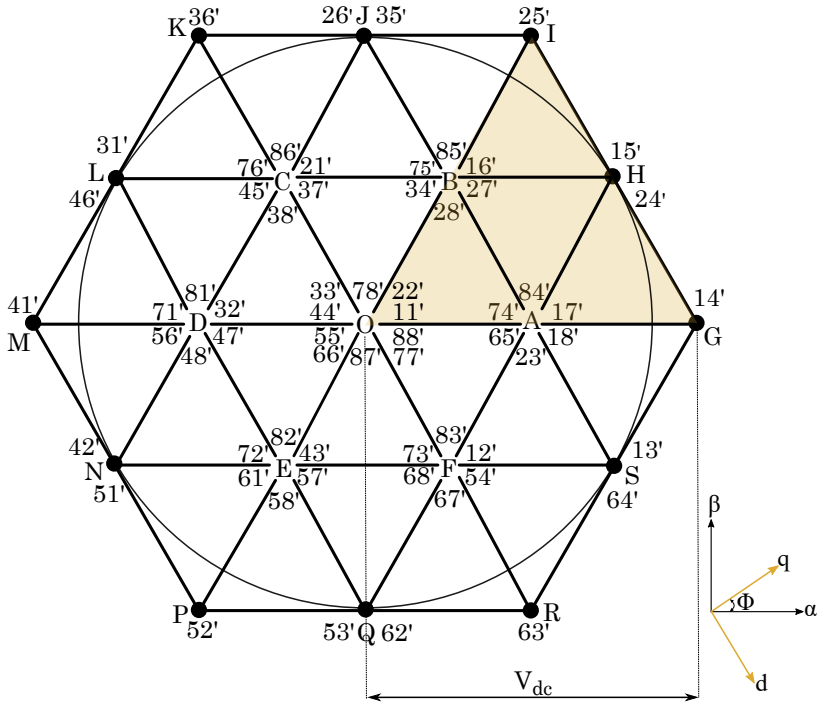


Figure 4.1: Space vector diagram with combined switching vectors of two two-level inverters.

this topology can be realized by two methods; offset power sharing and decoupled power sharing. These two methods are studied in detail in the sections below.

4.2.1 Offset power sharing

The offset power sharing is a modification of the conventional PWM generation in dual two-level inverter as discussed in Chapter 2. The block representation of this technique is shown in Fig. 4.2. The three-phase components of the reference vector are converted to the modulating waves, which are compared to two level-shifted carrier waves. This method inherently provides a per cycle average power sharing, as the modulating waves are displaced equally in each carrier region as

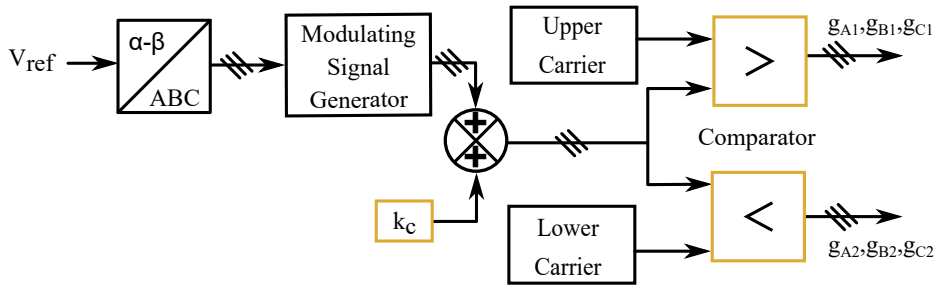
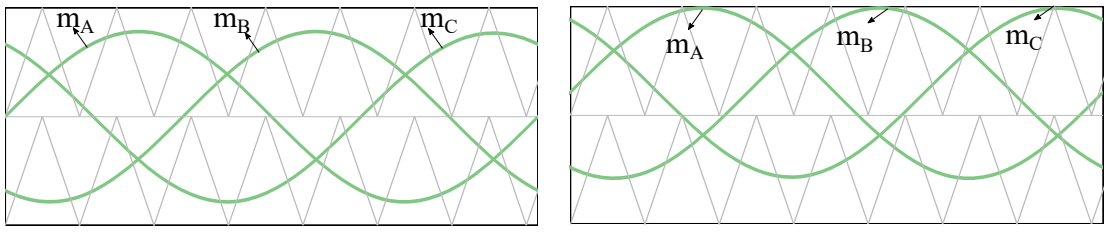


Figure 4.2: Block representation of offset power sharing.

shown in 4.3(a). If the modulation index is less than 1, the power regulation can be achieved by shifting the active vectors from center to either of the carriers by adding a common DC offset. The limit of DC offset, k_c, can be expressed as in (4.1) in Chapter 2:

$$k_c = \frac{1-M}{2}; \qquad 0 \leq M \leq 1 \tag{4.1}$$

When the value of k_c is 0, no offset will applied and the modulating waves will be at the center of the carrier region, providing an equal power sharing between both inverters. For a positive value of k_c, the offset will shift the modulating wave to the upper carrier zone as show in Fig. 4.3(b) and more power will be fed by Inverter-1 to the load. The opposite will happen when the value of k_c is negative. For better understanding, sinusoidal modulating waves are compared with carriers at



(a) (b)

Figure 4.3: Modulating waves at $M = 0.8$ compared with carriers for different k_c. (a) For $k_c = 0$ and (b) For $k_c = +ve$

reduced frequency.

4.2.2 Decoupled power sharing

The decoupled power sharing is realized by splitting the reference vector in to two phase opposed vectors [121], [142] as shown in Fig. 4.4. The reference vector can be split by a factor k_d, which denotes the power sharing ratio in the dual two-level inverter. For operation in the linear range, the limit of k_d can be expressed in the terms of modulation index M as in (4.2) [122]:

$$k_d = \frac{1-M}{2M}; \qquad 0 \leq M \leq 1 \tag{4.2}$$

and the decoupled reference vectors V_{ref_1} and V_{ref_2} for the two inverters can be written as:

$$\begin{aligned} V_{ref_1} &= k_d V_{ref} \\ V_{ref_2} &= (k_d - 1) V_{ref} \end{aligned} \tag{4.3}$$

where V_{ref} is the reference vector of the dual two-level inverter. As shown in the block diagram, the orthogonal components of the individual reference vectors,

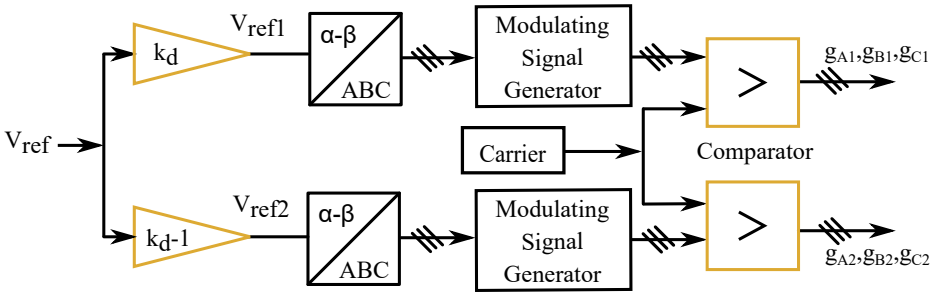


Figure 4.4: Block representation of decoupled modulation.

converted to three-phase components, are applied to the modulating signal generator. The output of modulating signal generator can be continuous or discontinuous signals with instantaneous amplitude proportional to the multiplication factor k_d. The modulating signals are then compared to the carrier wave with same comparison logic to generate two sets of gate signals for the individual two-level inverters. This is unlike the offset method, in which the comparison logic for the carrier wave are opposite. Since the modulating signal generator are independent, this sharing method can also be used to apply two different types of PWM to the individual inverter, providing a hybrid modulation.

Fig. 4.5 illustrates the decoupled power sharing method. When the value of k_d is 0.5, the reference is divided into two equal parts as shown in Fig. 4.5(a), resulting in equal load sharing in the dual two-level inverter [143]. For $k_d > 0.5$, the reference is divided unequally as shown in Fig. 4.5(b), resulting in Inverter-1

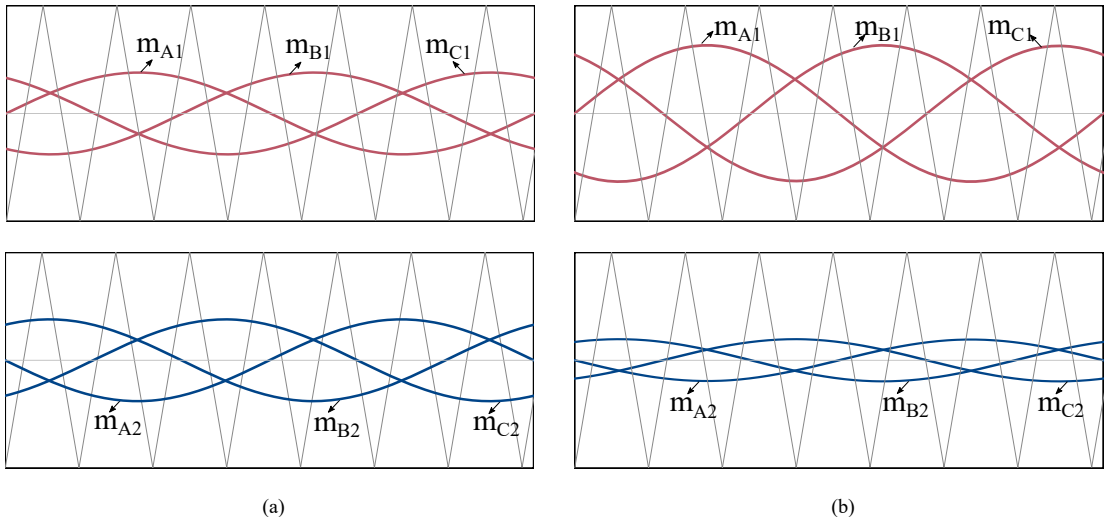


Figure 4.5: Modulating waves at $M = 0.8$ compared with carrier for different k_d.(a) For $k_d = 0.5$ and (b) For $k_d > 0.5$

delivering more power to the load. The opposite will happen when $k_d < 0.5$.

From both sharing methods discussed above, it may be noted that the sharing factors k_c and k_d can be applied based on the desired power sharing requirement between the two-level inverters. In case of battery powered vehicles, the difference of instantaneous SOCs of the isolated battery packs decides the value of regulating factors.

4.3 Switching sequences of different power sharing techniques

In CBM technique, the instantaneous three phase references are converted to modulating waves by placing of effective time period (or common mode voltage) in a switching cycle [27], [142]. In this study, the decoupled power sharing is applied, standard split clamp (30^0), continual clamp (60^0) and triplen harmonic injected (THI) PWM schemes for each inverter [75], [144]. If offset power sharing method is applied with clamping PWM schemes, it will result in maximum power being drawn from one of the sources even at lower load power. Since control of power sharing is desired in electric vehicular application, only THI scheme is considered for offset power sharing method.

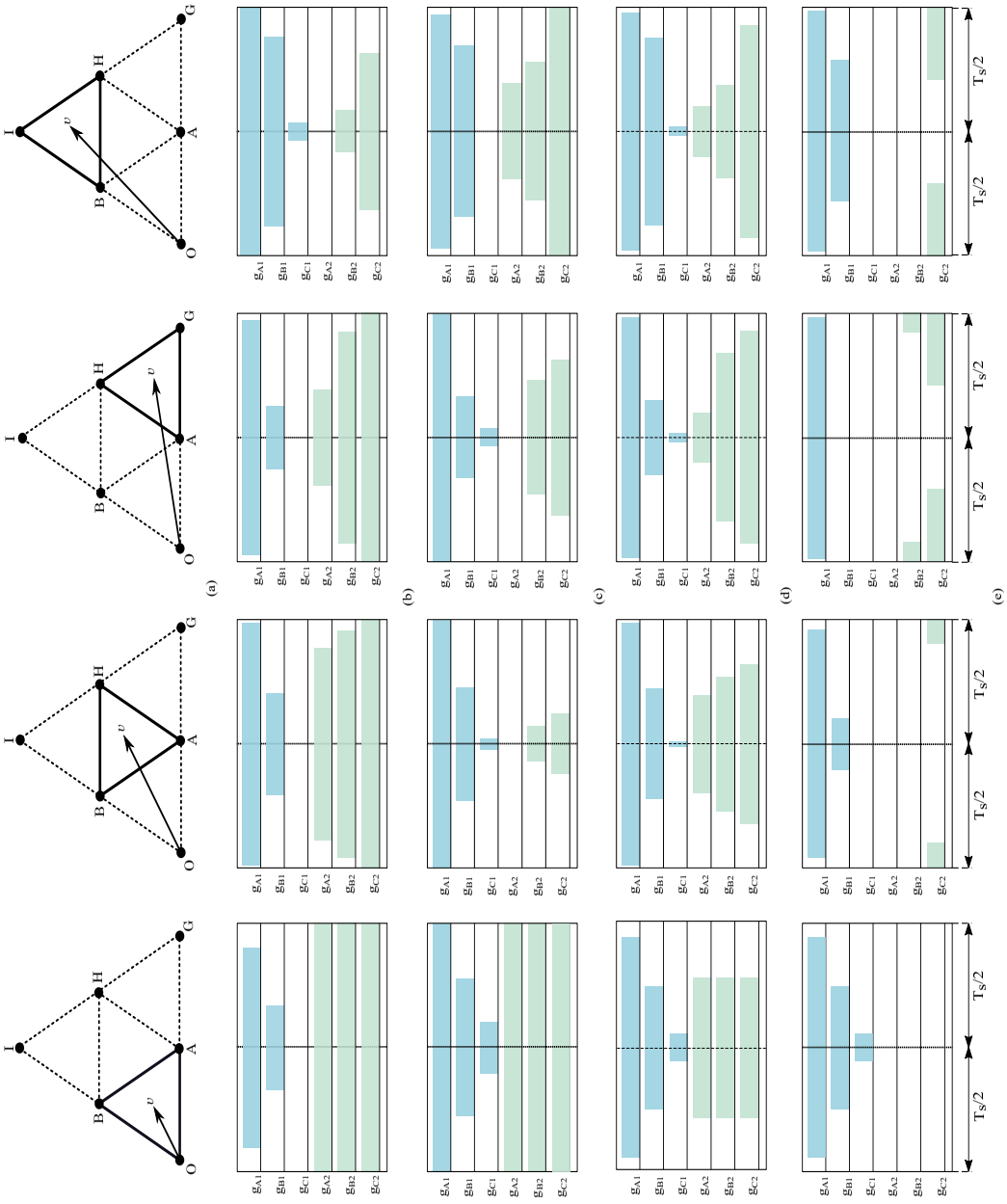


Figure 4.6: Switching pattern for different voltage vector position in first sectoral triangle *OGI* for different PWM schemes. (a) Sub-triangles, (b) DSC, (c) DCC, (d) DTHI and (e) OTHI.

Space vector approach is considered to study the switching sequence. For analysis, first sectoral triangle OGI from Fig. 4.1 is examined and the reference vector at center of each sub-triangle (OAB, AHB, AGH, BHI) are considered as shown in Fig. 4.6(a). Fig. 4.6(b) to 4.6(e) shows the corresponding gating sequence in the dual two-level inverter when power sharing is done using decoupled split clamp (DSC), decoupled continual clamp (DCC), decoupled THI (DTHI) and offset THI (OTHI) PWM schemes. The total switching cycle time period is T_s and the gate signals for Inverter-1 and Inverter-2 are represented by g_{A1}, g_{B1}, g_{C1} and g_{A2}, g_{B2}, g_{C2} receptively. These set of waveforms are for unequal power sharing in which Inverter-1 is delivering maximum possible share of the load power. Similar waveforms can be drawn for other power sharing condition.

In the inner sub-triangle OAB, the modulation index is small. It can be seen from the first column of Fig. 4.6(b) to 4.6(e) that in all schemes, the active vectors are generated by Inverter-1 alone, keeping the Inverter-2 clamped to its zero vector state. In DTHI scheme, Inverter-2 is switched from one zero vector state to other. This shows that the entire power has been shifted to Inverter-1. When the vector is in the middle sub-triangle AHB and outer sub-triangles AGH and BHI , the overall switching in the dual two-level inverter has increased for the decoupled power sharing schemes. In OTHI scheme, for the applied value of k_c, it can be observed that, total switching in the dual two-level inverter is minimum compared to other methods. It is also worth noting that, nearest three vectors are always applied in OTHI. This is not the case in decoupled power sharing and the switching vectors used do not form an equilateral triangle. The effect of these switching sequences on the motor phase current is discussed in the next section.

4.4 Ripple analysis of PWM techniques

It is feasible to compare different PWM techniques based on the overall quality of motor current waveform rather than the individual harmonic components produced by them [125], [126]. In VSI each switching state corresponds to a voltage vector. There will be always a difference between the required vector and applied vector. This results in an error voltage between reference and the instantaneous output voltage, which causes the output ripple current[138]. In other words it can be stated that the current ripple depends on the switching sequence of active and zero vectors applied by PWM techniques.

For current ripple analysis, the inductive load can be taken as a leakage inductance circuit as shown in 4.7, and the cumulative sum of error voltage in a switching cycle will give the magnitude of current error [20] as shown below:

$$I_{err} = \int \frac{V_{err}}{\sigma L_s} \tag{4.4}$$

where σL_s is the stator leakage inductance, V_{err} and I_{err} are the voltage and current errors receptively.

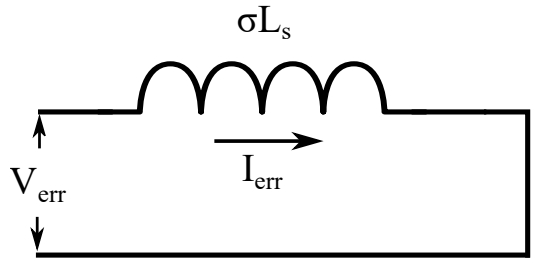


Figure 4.7: Simplified inductive circuit

4.5 Current ripple in dual two-level inverter

In general, the reference vector can be resolved into the orthogonal stationary components shown in (4.5)

$$V_{ref} = V_{ref}^{\alpha} + jV_{ref}^{\beta} \tag{4.5}$$

The two sets of three phase pole voltages due to the application of gate pulses are transformed to the α, β components as given in (4.6)

$$\begin{aligned} V_{app1}^{\alpha} &= \frac{V_{dc}}{2}\left(g_{A1} - \frac{1}{2}(g_{B1} + g_{C1})\right) \\ V_{app1}^{\beta} &= \frac{V_{dc}}{2}\left(\frac{\sqrt{3}}{2}(g_{B1} - g_{C1})\right) \\ V_{app2}^{\alpha} &= \frac{V_{dc}}{2}\left(g_{A2} - \frac{1}{2}(g_{B2} + g_{C2})\right) \\ V_{app2}^{\beta} &= \frac{V_{dc}}{2}\left(\frac{\sqrt{3}}{2}(g_{B2} - g_{C2})\right) \end{aligned} \tag{4.6}$$

On applying the superposition principal to the real and imaginary components in the above equations, the applied orthogonal components of the dual two-level inverter becomes:

$$\begin{aligned} V_{app}^{\alpha} &= V_{app1}^{\alpha} - V_{app2}^{\alpha} \\ V_{app}^{\beta} &= V_{app1}^{\beta} - V_{app2}^{\beta} \end{aligned} \tag{4.7}$$

From (4.5) and (4.7) the equations for the error voltage can be written as in (8):

$$\begin{aligned} V_{err}^{\alpha} &= V_{app}^{\alpha} - V_{ref}^{\alpha} \\ V_{err}^{\beta} &= V_{app}^{\beta} - V_{ref}^{\beta} \end{aligned} \tag{4.8}$$

The error voltages can be resolved to the orthogonal revolving reference frame components, V_{err}^{d} and V_{err}^{q}, using standard Park's transformation. On integrating the error voltages in a switching cycle, the current errors are given as in (4.9):

$$\begin{aligned} I_{err}^{d} &= \int V_{err}^{d} \\ I_{err}^{q} &= \int V_{err}^{q} \end{aligned} \tag{4.9}$$

In the equations above I_{err}^{d} and I_{err}^{q} corresponds to the flux and the torque ripple in the motor respectively [126], which are independent of each other. The difference of the maximum and minimum values of I_{err}^{d} and I_{err}^{q} gives the expression of peak to peak current ripple as given in (4.10)

$$\begin{aligned} I_{pp}^{d} &= max(I_{err}^{d}) - min(I_{err}^{d}) \\ I_{pp}^{q} &= max(I_{err}^{q}) - min(I_{err}^{q}) \end{aligned} \tag{4.10}$$

4.6 Current Ripple Trajectory for dual two-level inverter

The error currents derived in (4.9) can be plotted in a two dimensional plane as illustrated in Fig. 4.8 and Fig. 4.9. The current error trajectory for equal and unequal power sharing are represented. All the plots are normalized with respect to the leakage inductance. It can be seen that the "double-triangular" shape of the dq current ripple changes for the different PWM schemes. In Fig. 4.8(a) to 4.8(d) the ripple trajectories for both sharing conditions corresponding to low values of

M are shown. It can be seen that, DTHI scheme is having highest q-axis ripple and lowest d-axis ripple projection when the sharing is equal. In the unequal case, OTHI scheme is having the lowest ripple in both axes. Though the magnitude of ripple for DTHI and OTHI schemes are different, the current error trajectory in both schemes are similar for unequal sharing.

Fig. 4.9(a) to 4.9(d) shows the ripple trajectory of current error for higher value of M. It can be noted that the d-axis ripple for DCC scheme is the lowest for equal share ratio. However, the shape of the trajectory changed to multiple triangles for unequal sharing. In DTHI and DSC, the ripple locus area for equal and unequal sharing condition are higher and the ripple shape has changed to "rectangular". In OTHI scheme, the "double-triangular" shape is maintained in either of the sharing condition with minimum ripple.

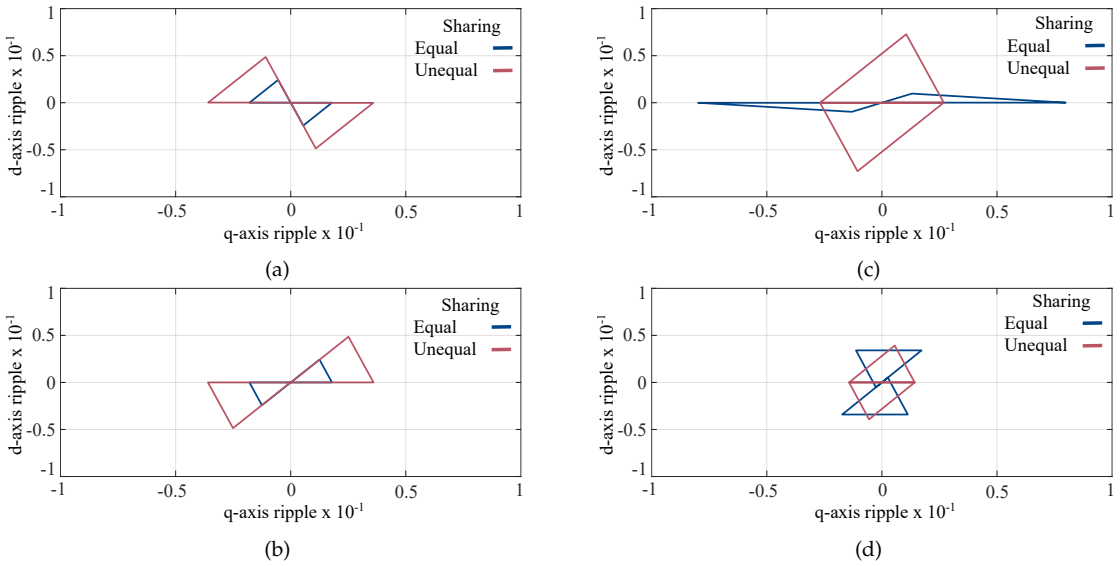


Figure 4.8: dq current error plots for equal and unequal sharing at $M = 0.4$ and $\theta = 25^0$. (a) DSC, (b) DCC, (c) DTHI and (d) OTHI.

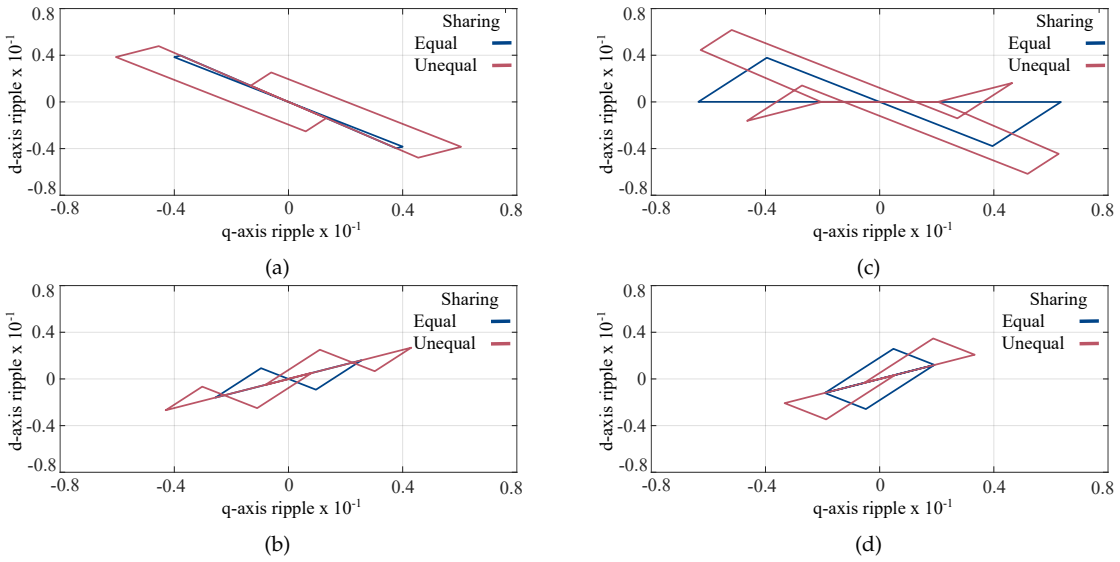


Figure 4.9: dq current error plots for equal and unequal sharing at $M = 0.8$ and $\theta = 45^0$. (a) DSC, (b) DCC, (c) DTHI and (d) OTHI.

From the above discussion it is clear that the current error trajectory not only changes with the modulation index but also with the power sharing ratio. The mathematical expression for ripple content can be easily derived for equal power sharing. However, this will be complex for unequal power sharing. It will be easier to calculate the ripple analytically using MATLAB or similar software. The peak to peak ripple obtained from the MATLAB analysis and experimental results are discussed in the next section. For the analysis, the carrier frequency of each PWM scheme has been appropriately scaled to maintain the same effective switching frequency.

4.7 Peak to peak current ripple comparison

4.7.1 Polar plot representation

The polar plots of minimum peak to peak current ripple for different decoupled power sharing schemes, are displayed in Fig. 4.10. Due to different limits of sharing factor, the offset power sharing technique is not included in this comparison and it will be considered later in this section. For better understanding, the minimum ripple content in both d-axis and q-axis are plotted separately and the sharing factor k_d in decoupled power sharing schemes are changed from 0.5 to 1. The radius of the plot is fixed by M and k_d as defined by (4.2). In the figures, color shades represents the PWM schemes having least ripple, at that M and angle. If two or more PWM schemes have the least ripple, they are also represented by different color shades.

Fig. 4.10(a), shows the plot for equal sharing ratio (i.e. $k_d = 0.5$) and radius of the plot will be 1. In q-axis, for $M > 0.5$, DCC has the minimum ripple, whereas DSC has least ripple for lower M. In d-axis, for $M > 0.5$, DCC is better at most of the angles. The DTHI scheme has minimum ripple for a small portion at every 60^0 interval in the plot. When $k_d = 0.6$ as shown in 4.10(b), the results are similar to the previous case, except that the plot area is reduced due to the limit set by k_d. The d-axis ripple shown in Fig. 4.10(c) for $k_d = 0.8$ is approximately the same for both DSC and DCC schemes. However, in the q-axis plot, DSC is better for a larger portion. When the power is completely shifted to one side (i.e. $k_d = 1$), q-axis ripple for

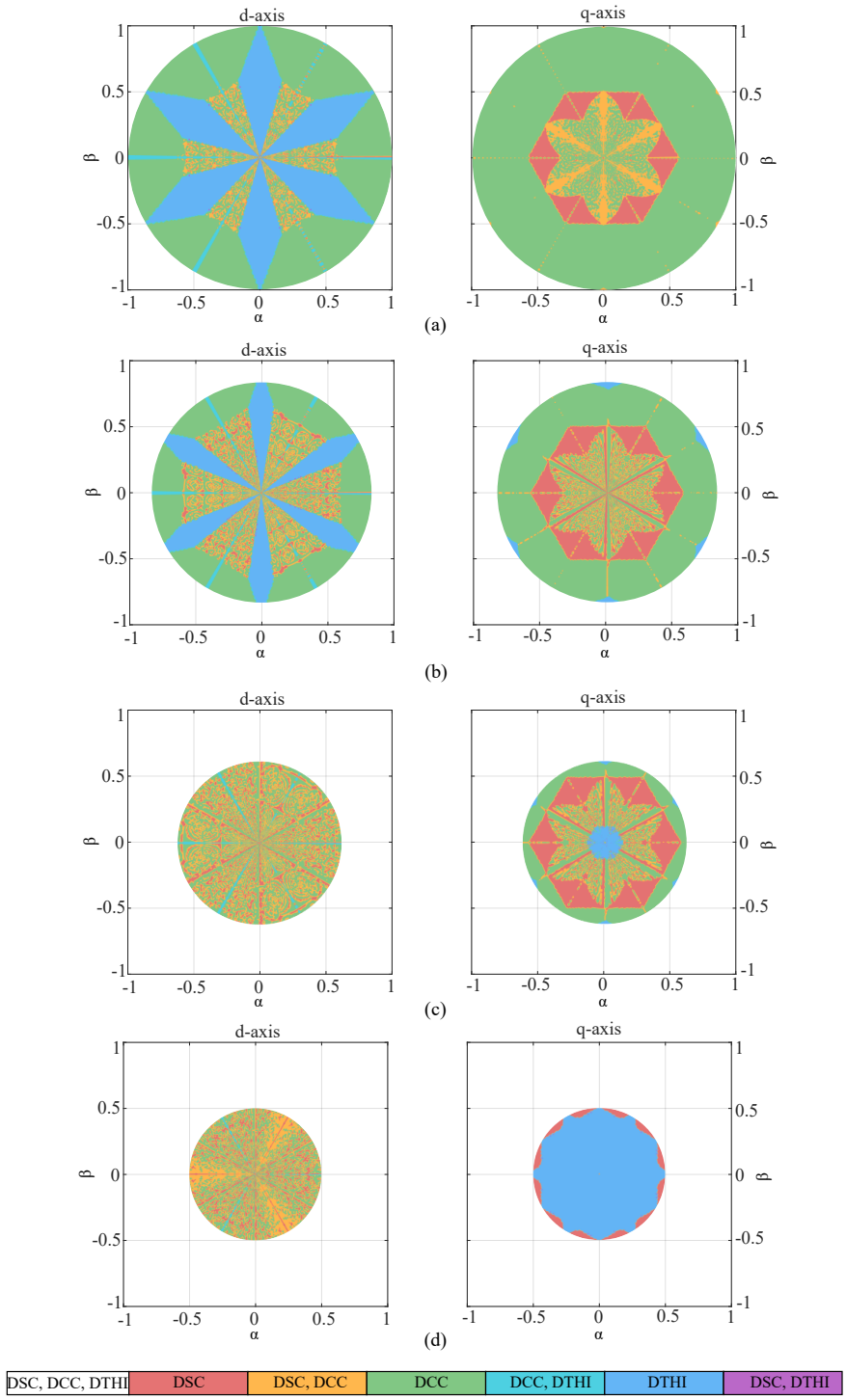


Figure 4.10: Polar plot representation of peak to peak ripple current for decoupled power sharing with different sharing factor. (a) $k_d = 0.5$, (b) $k_d = 0.6$, (c) $k_d = 0.8$, (d) $k_d = 1$.

DTHI scheme is minimum, which can be predicted from the ripple trajectory in Fig 4.8(c). In d-axis, similar to $k_d = 0.8$, DSC and DCC have minimum ripple. Though the discontinuous switching pattern has minimum ripple content for equal power sharing ($k_d = 0.5$) as claimed in [142], it changes for unequal power sharing. In the extreme case, when power is completely shifted to one of the inverters, DTHI has the least ripple. In decoupled power sharing, on keeping same carrier frequency, a effective power sharing can be implemented by changing the PWM schemes based on minimum ripple content in a linear modulation range.

For current ripple comparison of offset and decoupled power sharing, extreme

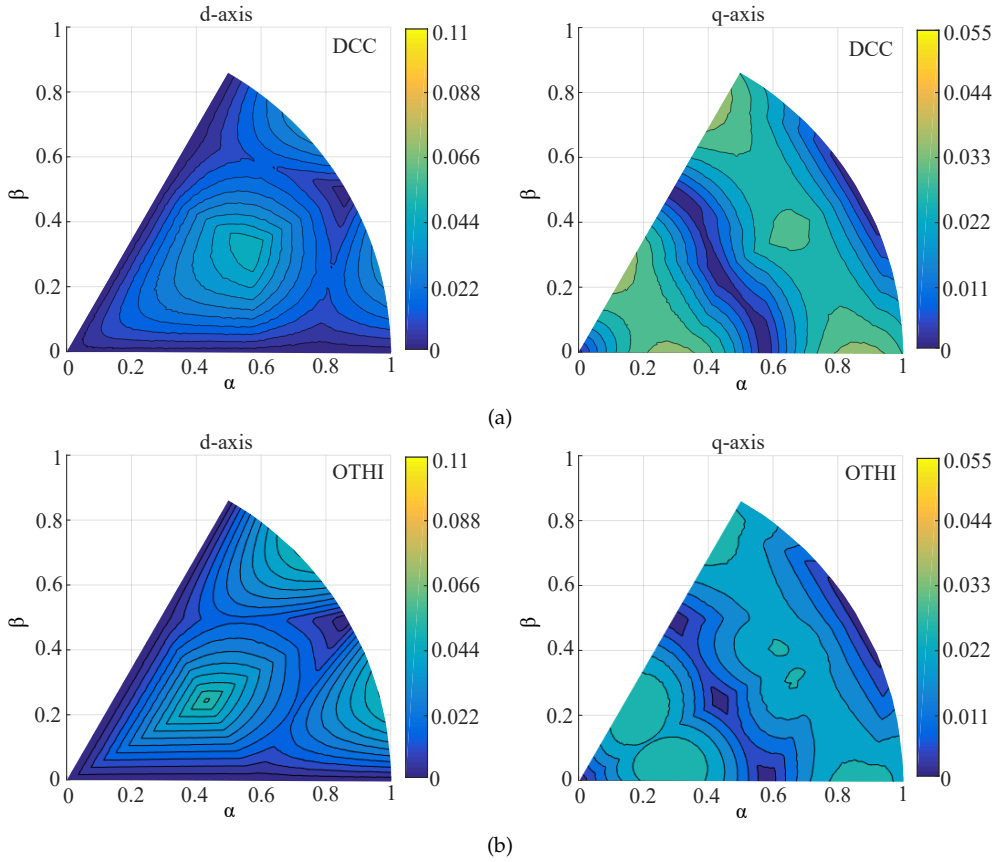


Figure 4.11: Peak to peak ripple current amplitude (a) DCC with $k_d = 0.5$, (b) OTHI with $k_c = 0$.

cases of half and full power from Inverter-1 is considered. It can be seen from Fig. 4.10 that, in q-axis, DCC and DTHI respectively has the least ripple for $k_d = 0.5$ and $k_d = 1$. Hence these PWM schemes can be compared with similar power sharing of OTHI as shown in Fig. 4.11 and 4.12. The peak to peak ripples are plotted for the first sector of SV structure in $\alpha\beta$ plane. The radii of the plots are fixed by (4.1) and (4.2). It can be noted that for equal sharing in DCC and OTHI schemes, the difference in the shape of the plot and the ripple amplitude is very small. For unequal sharing, the ripple in DTHI is double than that of the OTHI as shown in

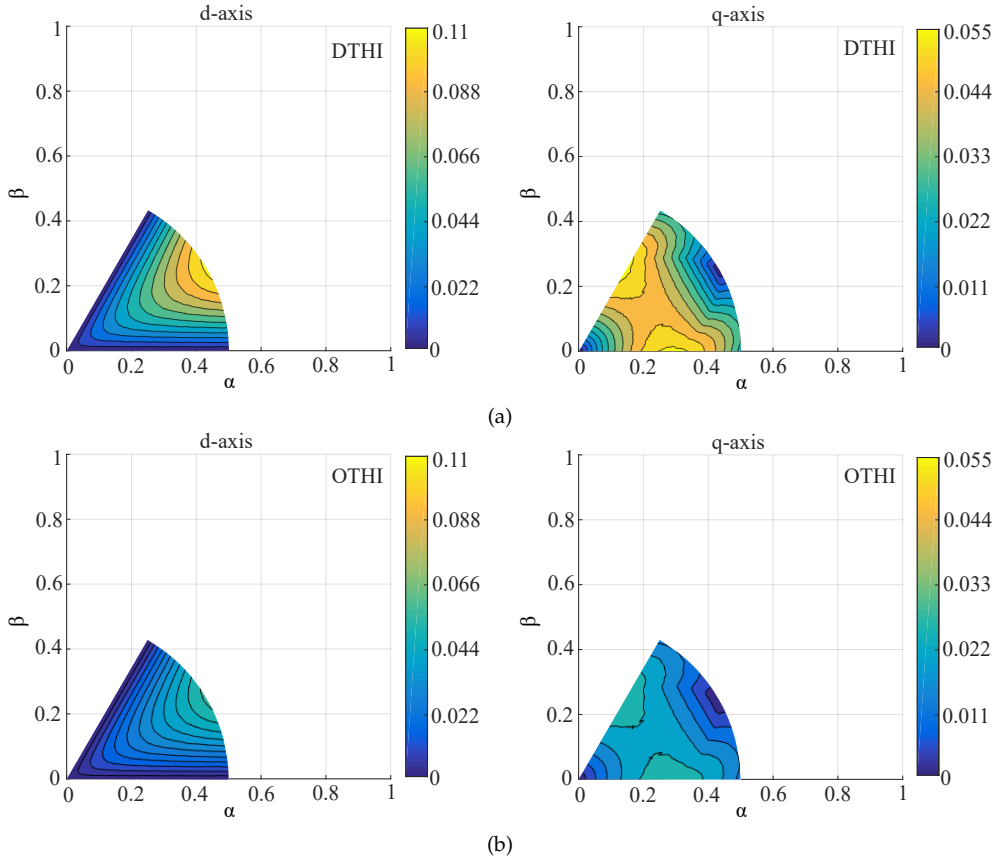


Figure 4.12: Peak to peak ripple current amplitude (a) DTHI with $k_d = 1$, (b) OTHI with $k_c = +ve$.

4.12(a) and 4.12(b). This shows that the power sharing with offset power sharing can be a suitable alternative to decoupled power sharing.

4.7.2 Current ripple envelope and multilevel voltage waveform

Fig. 4.13 and 4.14 shows the phase current and the ripple amplitude envelope of different PWM schemes in unequal sharing. The figures are obtained by post processing current data in MATLAB. Fig. 4.13(a) to 4.13(d) shows the peak to peak ripple envelope for lower M. It can be seen that OTHI scheme is having the lowest ripple compared to decouple sharing PWM schemes. Moreover, in decouple sharing method DTHI scheme will have minimum ripple than the discontinuous schemes when $k_d = 1$, as evident from the polar plot representation. Fig. 4.14(a) to

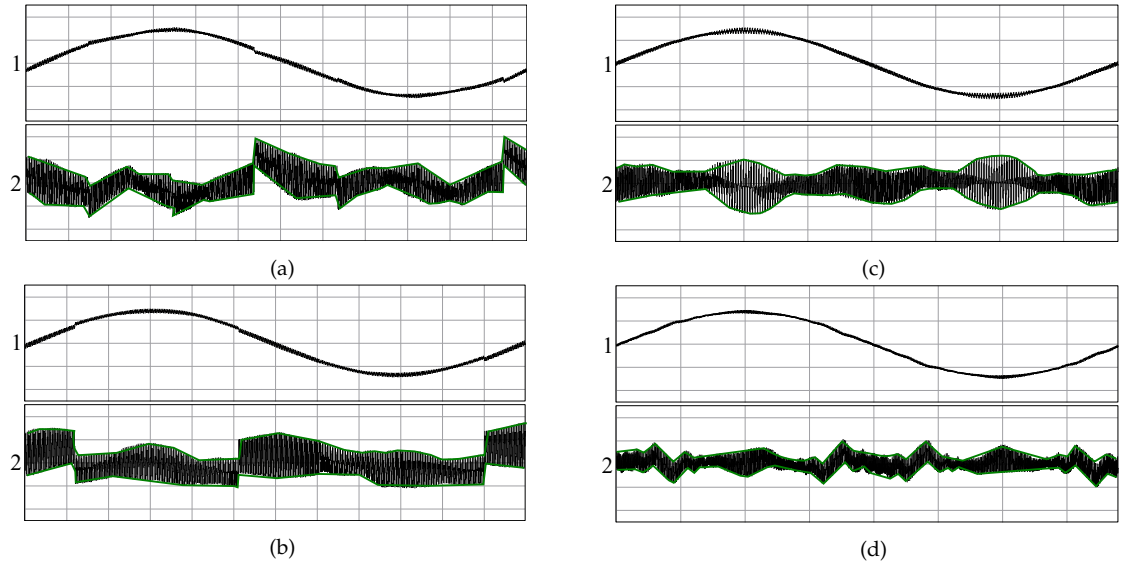


Figure 4.13: Phase current and peak-to-peak ripple amplitude envelopes at $M = 0.42$ for unequal sharing. (1) phase current (2 A/div), (2) peak to peak ripple (0.2 A/div). (a) DSC, (b) DCC, (c) DTHI and (d) OTHI.

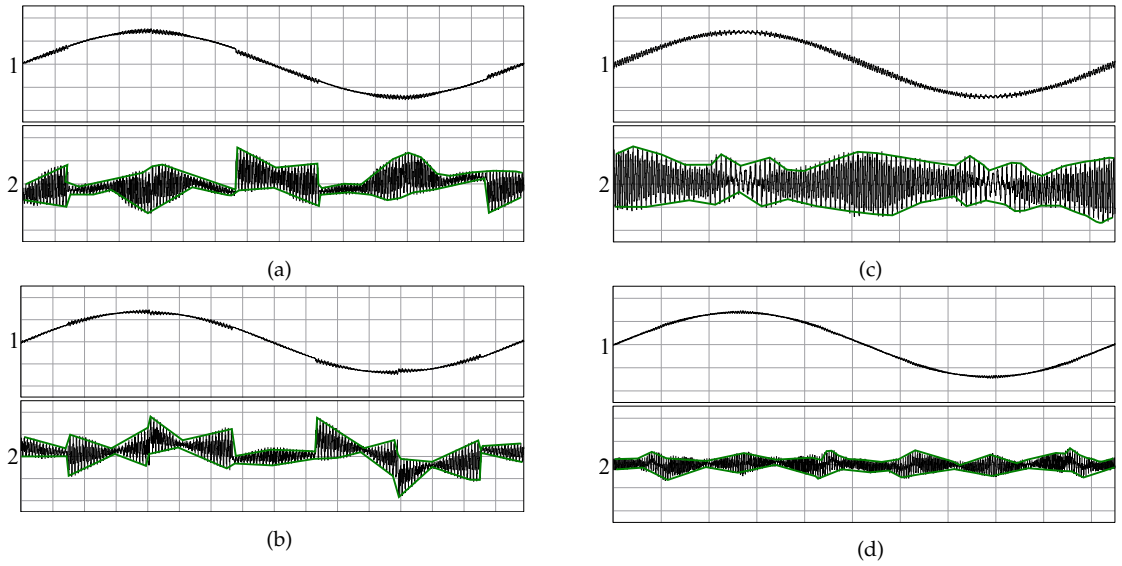


Figure 4.14: Phase current and peak-to-peak ripple amplitude envelopes at $M = 0.833$ for unequal sharing. (1) phase current (2 A/div), (2) peak to peak ripple (0.2 A/div). (a) DSC, (b) DCC, (c) DTHI and (d) OTHI.

4.14(d) shows the peak to peak ripple envelope for higher M. It can be noticed that discontinuous schemes has comparatively lower ripple than DTHI. However, the ripple envelope of OTHI is significantly smaller than all decouple sharing PWM schemes.

The motor phase voltage and no-load current waveform will be similar for both sharing techniques in unequal power sharing at lower M. However for unequal sharing at higher M, the multilevel voltage waveforms are very distinct for decoupled and offset power sharing as shown in Fig. 4.15. In decoupled power sharing schemes the voltage waveform has deviated from its ideal multilevel shape. However, a proper multilevel voltage waveform has been maintained using OTHI as shown in Fig. 4.15(d), even for unequal power sharing. It can also be observed that

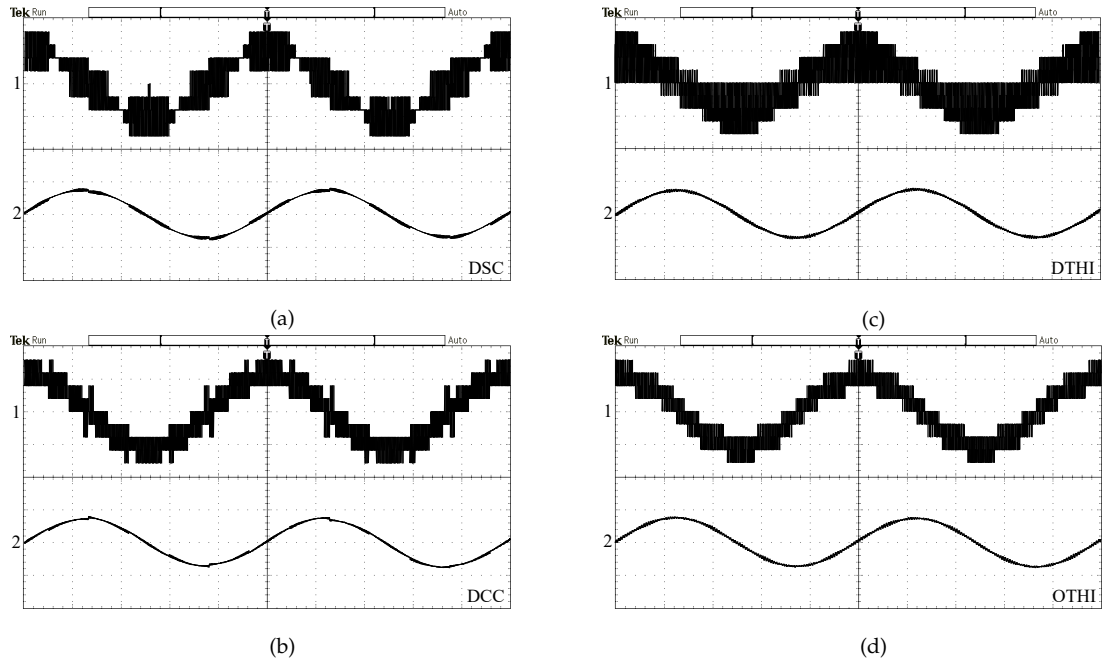


Figure 4.15: Experimental results at $M = 0.833$ (X-axis; 4 ms/div). (1) phase voltage (100 V/div), (2) phase current (2 A/div). (a) DSC, (b) DCC, (c) DTHI, and (d) OTHI.

the currents for discontinuous pattern (DSC and DCC) are similar and has considerable glitches at the peak of the waveform due to the clamping in the respective intervals. In DTHI, the voltage forms a multilevel waveform but there are large transitions from minimum to maximum level of voltage. However, for the OTHI scheme, the current and voltage are not affected by the offsets applied. Therefore it can have improved performance in dual two-level inverter drive compared to decoupled power sharing schemes.

4.8 Conclusion

In this chapter a time-domain analysis of output current ripple for different PWM techniques in dual two-level inverter with varying power sharing ratios is presented. The current ripple evaluation is performed based on the error voltage

vector and compared between decoupled and offset power sharing technique in the dual two-level inverter. From the studies, it can be observed that the ripple is not only dependent on the modulation index, but also on the sharing ratio. The switching sequence for different schemes in the first sector of space vector has been analyzed. The current error has been derived and trajectory of the current ripple for different modulation index and sharing ratio are plotted in a complex plane. Peak to peak current ripple amplitude for decoupled and offset sharing PWM techniques have been shown in complex plane. In decoupled power sharing, the DCC scheme can be more effective for equal sharing. When the full power is shifted to one inverter, DTHI is preferred. There is an attractive scope for interchanging between the PWM schemes in decoupled power sharing to provide minimum current ripple when the sharing ratio changes. Only continuous PWM scheme is suitable for offset power sharing technique. It is worth noting that, in decoupled power sharing, switching instances in a sub-cycle is more than that of the offset power sharing irrespective of sharing ratio. Overall it can be stated that in decoupled power sharing has more flexibility, while compromising the waveform quality. In contrast, offset power sharing has better waveform quality with reduced power sharing flexibility.

Chapter 5

Conclusion

5.1 Overview of thesis

A dual two-level inverter feeding an open-ended motor is an attractive multilevel topology for EV drives. The topology has several structural benefits when compared to other classic three-level inverters. Dual two-level inverter supplied form isolated DC sources can naturally eliminate the zero sequences current effect. In EVs, isolated sources can conveniently be implemented by splitting the battery pack into two equal sub-packs. With this configuration individual control of each two-level inverter is possible, making dual inverter a modular topology. Being fed from isolated DC sources, power flow will have to be managed from individual DC-links for one of the following reasons:

- The isolated battery packs may have different charge during normal operation of the drive. If the same amount of power is drawn from both sources,

the battery pack having a lower voltage level or SOC will discharge faster than the other. Therefore power need to be regulated for maintaining balance DC-link voltage and uniform discharge of individual packs, during dynamic and steady state operation.

- The isolated DC sources can be different energy storage element. For example, one DC-link voltage can be obtained from a battery pack and other can be from a high capacity element like ultracapacitor. Therefore with power regulation, ultracapacitor can be made to feed more power during start or acceleration, whereas power from the battery pack can be fed while cruising.

- A half-bridge fault can occur in any of the three phase inverters in dual inverter. For reliable operation during such conditions, power can shifted to the healthy inverter and the system can be operated as conventional three phase drive at half rated power and speed.

This thesis emphasis on PWM techniques for effective power sharing in dual two-level inverter.

A simple CBM technique for regulating power flow between isolated DC sources was presented in the second and third chapter. The proposed technique is a modified form of conventional PWM generation in three-level inverters. The sharing is implemented by a simple offset mechanism, in which the modulating waves are moved in the upper or lower carrier band. The technique is mathematically analyzed and different switching sequences are provided for applied offset. The limit, magnitude and sign of the offset are decided by the modulation index M

and the difference between the SOCs of the isolated DC source. Since SOC varies at a slower rate, a PI controller with a higher time constant is used for an average SOC balancing. The proposed sharing technique maintains a proper multilevel output, without altering the steady state operation of the drive. It also provides an effective SOC balancing and power flow control between the isolated DC sources during dynamic operation. Since CBM technique is used, a complex computation for sector identification and vector time calculation is not required.

The fourth chapter extends the analysis of motor current ripple for different PWM techniques when the power sharing ratio is changed. The main focus of this chapter is to provide a concept of generalized power sharing methods in the dual two-level inverter and their effect on the current ripple when different power sharing is applied. The analysis is performed for continuous and discontinuous switching schemes in CBM techniques based on the error voltage vector. A mathematical expression of peak to peak current ripple is also derived. Current error trajectories are plotted for equal and unequal sharing in different switching schemes. Polar plot representations for peak to peak current ripple are illustrated for various sharing factor in linear modulation range. In different modulation index, the current ripple envelopes are shown for various PMW schemes when the sharing ratio is unequal. Experimental results showing effective phase voltages and phase currents for different power sharing PWM techniques are given in this chapter.

The concepts were initially verified by conducting extensive simulation studies in MATLAB/Simulink and PLECS. Experimental validation was done using prototypes at low power as shown in Fig. 5.1. A 5.6 kW induction motor was used as

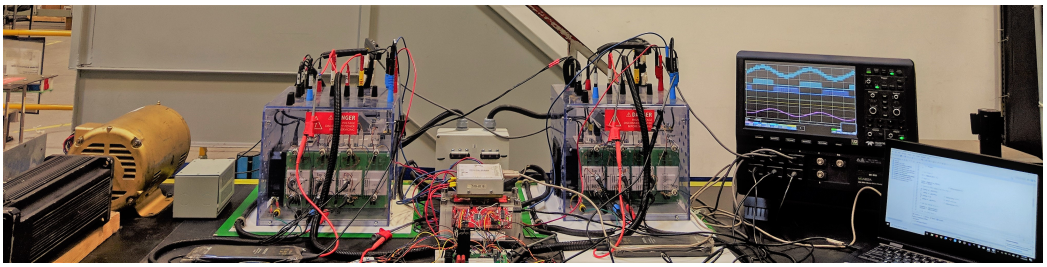


Figure 5.1: Photograph of experimental setup.

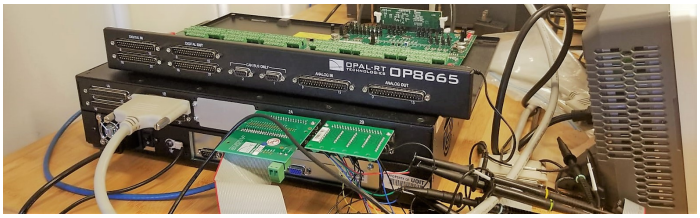


Figure 5.2: Photograph of OPAL-RT setup.

a three phase load, which was modified as an open-ended motor. The speed of the motor is controlled by a V/f controller for prototype experiments.

The dual two-level inverter system was build using two Semikron's stacks which are fed from two independent rectified DC-link voltages of 135 V from two separate auto-transformers. TMS320F28069M DSP platform was used to execute the control for the proposed drive schemes and the variables are represented in fixed point representation. The switching frequency was fixed at 3 kHz for comparison with existing systems in the literature which are below 5 kHz. The topology and proposed controller can be operated at higher switching frequencies. However, this may lead to higher switching losses and EMI. Moreover, the benefits of multilevel operation of the topology allows the drive to operate at lower switching frequencies with reduced harmonics and losses. For IGBT gate drivers the output

of the DSP was boosted from 3.3 V to 15 V using CD4504 B buffer ICs. A customized DAQ was used to measure the DC link voltage. For the driving profile tests, a 75 kW induction motor parameter was used in which torque and speed are controlled by the FOC controller. The motor and dual inverter were modeled in simulink. The battery and vehicle model were used from MATLAB and PLECs library blockset to implement on real-time simulator shown in 5.2. The controller was implemented using simulink and C2000 processor blockset in MATLAB. While the proposed concepts maybe easily extended to higher power levels by using suitably rated devices, the control techniques presented shall still remain applicable.

5.1.1 Disadvantages of dual inverter topology and proposed modulation technique

- **Power sharing ratio**: In the proposed modulation technique, when the offset voltage is applied to shift the modulating wave in either level-shifted carrier region, the actual power sharing ratio in the dual two-level inverter cannot be determined.
- **Power and speed limitation**: During fault tolerant operation, when the entire power is shifted to one of the inverters, the total power and speed of the drive system will be limited to half of the rated value. The other inverter will be providing the star point connection by clamping to its DC bus without delivering any power to the load. Moreover, the system will be operating as a conventional two-level inverter drive.

- **Two isolated DC supplies**: The topology fed from isolated DC sources will eliminate the zero sequence current. However, for isolated sources, two charging units are required both for on-board and utility charging.

5.2 Claims of originality

- Identified a simple PWM technique for power sharing in the dual two-level inverter fed from isolated DC sources. The control mechanism is feasible for three-level open-ended motor drives in EV application. The proposed modulation technique provides an effective power regulation without affecting the steady state operation of the drive. The proposed modulation technique does not have any digital implementation complexities.

- A fault tolerant implementation technique is presented for dual inverter which can operate the drive at half the rated power and speed without any auxiliary circuit or control mechanism. The proposed technique can provide an artificial neutral by clamping the faulty inverter to its DC bus. This can be obtained by shifting the reference wave in the carrier region corresponding to the healthy inverter. During this transition, the normal operation of the drive will not be affected and the neutral connection is obtained by using zero vector switching combination of faulty inverter.

- An instantaneous SOC balancing technique is proposed for isolated DC sources in dual inverter. If DC sources are fed from battery packs, the modulation

technique can provide SOC balancing which will be suitable for higher battery life. If DC sources are fed from different energy storing devices, the modulation technique provide SOC balancing for unequal capacities, which will provide assistance for mass acceleration in EVs.

- A current ripple analysis has been presented for dual inverter. It was found that different PWM techniques has different ripple content, when the sharing ratio in dual inverter changes. Based on the minimum peak to peak current ripple and appropriate multilevel waveform, a suitable PWM can be used for power sharing and multilevel operation in dual inverter drive.

Chapter 6

Scope of future work

There are several possibilities to explore the concepts proposed in this thesis for EV traction drives. The following topics can be investigated for further research studies:

- Regenerative braking is an important aspect to be considered for electric vehicles. During deceleration or breaking, the energy stored in the machines can be fed back to the DC source. In induction motors, while braking the supply frequency should be reduced and slip should be kept negative. This concept is extensively discussed in many literatures for two-level inverter with a single battery pack. In dual two-level topology the same concept can be implemented using the proposed power sharing technique. A control mechanism based on the instantaneous SOC can be used with the same slow PI controller, to feed the regenerated power to the battery pack having a higher capacity or lower SOC. A SOC monitoring and control can also be studied for a balanced regeneration when the battery packs are maintained at equal SOCs.

- The dual inverter topology can be implemented with different combinations of isolated energy storage systems. The combination can be battery pack and ultracapacitors or battery pack and fuel cell etc to form hybrid storage. The storage system with higher power density can be used to provide power assistance during mass acceleration, hill climbing etc. The source obtained from ultracapacitor can also be utilized for the initial reactive power compensation in the motor drive. With suitable control, an experiment can be performed with proposed power sharing technique to feed more power from higher capacity storage system while starting and heavy acceleration, then gradually shifting the power to the battery pack while cruising. An interleaved DC/DC converter can be designed to maintain voltage level symmetry in hybrid energy storage system.

- In decouple power sharing techniques, each inverter can be individually controlled. In the thesis, it has been discussed that different PWMs have different current ripple for varied sharing ratio. There is an attractive scope for interchanging between the PWM schemes by modifying the applied effective time period in a switching cycle. The effective time can be applied such that motor phases have minimum current ripple when the sharing ratio changes during linear operation. Moreover, individual inverters can be modulated by different PWM schemes, making a hybrid switching for minimum torque and flux ripple.

- In the offset power sharing technique, actual sharing ratio between the isolated sources cannot be determined. In order to extract more power from source having higher SOC, a control algorithm can be implemented to clamp

the instantaneous peaks of continuous modulating signals when the offset is applied. This will linearize the operation of the drive in over-modulation region.

- Different fault tolerant strategies can be investigated based on motor winding faults, inverter device faults etc., for conveniently shifting the power to one of the two-level inverters and operating as conventional three phase drive. The control should be capable of limiting the power and speed to half of the rated value, to avoid six-step operation of three phase inverter drive.

- Wide band gap devices like GaN, can be used to reduce the switching losses in dual inverter drive. The system can be analyzed with GaN devices when operated at a higher switching frequency to observe the reduction of total losses and efficiency improvement when the power sharing logic is applied.

- For a vehicular application, charging individual battery packs may not be cost effective. The secondary battery needs to be charged through the motor (standstill) using a single charging circuit. This can be implemented by the orthogonal components of the motor phase current. At standstill, there will be no motor torque, hence the q-axis current component can be made zero. The d-axis current corresponding to flux can be used to provide the charging current to the secondary battery using a simple PI controller. The controller should be capable of limiting the excess flow of d-axis current, as it may saturate the motor core.

Appendix A

Publications

[1] **R. Menon**, N. A. Azeez, A. H. Kadam, S. S. Williamson and C. Bacioiu, "An instantaneous power balancing technique for an open-end IM drive using carrier based modulation for vehicular application," *IEEE Transactions on Industrial Electronics*.

[2] **R. Menon**, N. A. Azeez, A. H. Kadam and S. S. Williamson, "Study and analysis of the effects of varied PWM techniques and power sharing ratios on the current ripple in open-ended, 3-level traction motor drives," *IET Electrical Systems in Transportation*. (under review)

[3] A. H. Kadam, **R. Menon** and S. S. Williamson, "A bidirectional three phase buck-boost ac-dc converter for common dc bus virtual electrical traction machine," *IEEE Transactions on Power Electronics*. (under review)

[4] **R. Menon**, S. S. Williamson, and A. H. Kadam, "A fault tolerant strategy for an open-ended dual inverter traction motor drives," *IEEE Transactions on Transportation Electrification*. (under review)

[5] **R. Menon**, S. S. Williamson, N. A. Azeez and A. H. Kadam "A modulation strategy for fault tolerant operation in dual inverter drive," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore. (under review)

[6] **R. Menon**, N. A. Azeez, A. H. Kadam and S. S. Williamson, "Carrier based power balancing in three-level open-end drive for electric vehicles," in *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, Doha, 2018, pp. 1-6.

[7] **R. Menon**, N. A. Azeez, A. H. Kadam and S. S. Williamson, "Energy loss analysis of traction inverter drive for different PWM techniques and drive cycles," in *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Hamilton, 2018, pp. 201-205.

[8] **R. Menon**, A. H. Kadam, N. A. Azeez and S. S. Williamson, "A comprehensive survey on permanent magnet synchronous motor drive systems for electric transportation applications," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 6627-6632.

Appendix B

Modeling

B.1 Induction motor parameters

The parameters of induction motor used for various simulation and experimental studies are given below.

Motor1 : For prototype tests
5.6 kW, open-end winding, squirrel cage induction motor, 460/230 V, 60 Hz, 3450 rpm, 2 poles, Rs = 1.39 Ω, Rr = 1.44 Ω, Ls = 0.22 H, Lr = 0.22 H, M = 0.21 H.

Motor2 : For drive cycle tests
75 kW, open-end winding, squirrel cage induction motor, 460/230 V, 60 Hz, 1748 rpm, 4 poles, Rs = 42.32 Ω, Rr = 42.32 Ω, Ls = 0.152 H, Lr = 0.152 H, M = 0.148 H.

The approximate parameters of the induction motor can also be estimated by using the empirical formals as giving the script below [104]:

Script for parameter estimation

```
%% Induction Motor Information %%
V_ll                                    %nominal line volatge
f                                       %rated frequency
I                                       %nominal current A
Io                                      %no load current A
N                                       %nominal speed in rpm
P                                       %no. of poles
%% Empirical Equations %%
wm = N*(pi/30);                         %nominal speed in rad/sec
zp = P/2;                               % no. of pole pairs
Ls = V_ll/(Io*wm*sqrt(3));              %stator inductance
sigmaLs = V_ll/(5.5*I*wm*sqrt(3));      %leakage inductance
M = Ls-sigmaLs;                         %mutual resitance
Rs = (0.02*V_ll)/(I-2);                 %stator resitance
Rr = (2*pi*(f-((zp*N)/60))*Ls*Io)/(sqrt((I^2)-(Io^2)));
                                        %rotor resitance
```

B.1.1 Induction motor modeling

In voltage controlled AC drives the three phase variables in the abc coordinate system are transformed into an equivalent two-phase coordinate system that has an

arbitrary speed in a given reference frame. The significant coupling that exists between the stator and rotor variables of a three-phase AC machine can be made to disappear by modeling the machine in term of dq variables. This enables a decoupled control of AC motor similar to a separately excited DC drive. For an induction motor the dq model in synchronous reference frame can be expressed as:

$$\begin{bmatrix} V_{sd} \\ V_{sq} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + L_s\frac{d}{dt} & -L_s\omega_s & M\frac{d}{dt} & -M\omega_s \\ L_s\omega_s & R_s + L_s\frac{d}{dt} & M\omega_s & M\frac{d}{dt} \\ M\frac{d}{dt} & -(\omega_s - \omega_r)M & R_r + L_r\frac{d}{dt} & -(\omega_s - \omega_r)L_r \\ (\omega_s - \omega_r)M & M\frac{d}{dt} & (\omega_s - \omega_r)L_r & R_r + L_r\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} \tag{B.1}$$

The subscript s and r denotes the stator and rotor variables respectively. L and M are self and mutual inductance receptively. ω is the angular frequency and R is the resistance of stater and rotor winding.

The electromagnetic torque in terms of dq variables can be written as:

$$T_e = \frac{2}{3}\frac{p}{2}M(i_{sq}i_{rd} - i_{sd}i_{rq}) \tag{B.2}$$

where p is the pole pair and $2/3$ is the factor for transformation. The electromagnetic torque can also be expressed in terms of rotor flux linkage as given below:

$$T_e = \frac{2}{3}\frac{p}{2}\frac{M}{L_r}(i_{sq}\lambda_{rd} - i_{sd}\lambda_{rq}) \tag{B.3}$$

B.2 Variable transformation matrix

ABC to $\alpha\beta$: Clarks transformation

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_A \\ f_B \\ f_C \end{bmatrix} \tag{B.4}$$

$\alpha\beta$ to dq: Parks transformation

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} sin\phi & -cos\phi \\ cos\phi & sin\phi \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{B.5}$$

B.3 Vehicle parameter

The vehicle parameter used for real time simulation is shown in Table B.1.

B.3.1 Vehicle modeling

A simplified vehicle model can be written as:

$$m\frac{dv}{dt} = F_t - F_d - F_g - F_r \tag{B.6}$$

Table B.1: Vehicle parameters.

Parameter	Value
Vehicle Mass (m)	$1225kg$
Front cross sectional area (A)	$3\ m^2$
Wheel radius (r_w)	$0.276\ m$
Height of vehicle center of gravity (H_g)	$0.54\ m$
Acceleration due to Gravity (g)	$9.81\ m/s^2$
Coefficient of Rolling Resistance (f_r)	0.01
Coefficient of Drag (C_d)	0.5
Gear ratio (g_r)	1.6
Gradient of road (α)	10^o
Air density a_d	$1.2\ kg/m^3$

where m is the mass of the entire vehicle, v is the actual vehicle speed, F_t is the traction motor driving force, F_d is the aerodynamic friction losses, F_g is the uphill driving losses and F_r is the rolling friction losses. The driving force is the input from traction motor to the wheel written as below:

$$F_t = r_w T_w \tag{B.7}$$

where r_w is radius of the wheel and T_w is torque input to the wheel. The aerodynamic friction losses are also called drag losses can be calculated as:

$$F_d = \frac{1}{2}\rho C_d A v_r^2 \tag{B.8}$$

where ρ is the density of the air, v_r is speed of the vehicle relative to the air, A is the cross-section area of the vehicle front, and C_d is drag coefficient. The uphill or inclined driving losses depends on mass of the vehicle, gravity and gradient of the road as written below:

$$F_g = mgsin\alpha \tag{B.9}$$

Rolling friction losses can be expressed as:

$$F_r = f_r mgcos\alpha \tag{B.10}$$

where f_r is the friction coefficient.

The vehicle speed in m/s can be expressed as below:

$$v = \int \frac{F_t - F_d - F_g - F_r}{m} \tag{B.11}$$

The motor speed in rad/s can be expressed as below:

$$\omega_m = v\left(\frac{g_r}{r_w}\right) \tag{B.12}$$

B.4 Three phase inverter modeling

Two-level inverter discussed in 1.2 can be realized in equation form by defining the logic switching. Let $m_1, m_2, .., m_6$ be the switching variable which can take two value 0 when all the switching devices ($S_1, S_2, .., S_6$) are open and value 1 when the

devices are closed. The pole voltage can be expressed in (B.13)

$$\begin{aligned} V_{AO} &= \frac{V_{dc}}{2}(m_1 - m_2 + 1) \\ V_{BO} &= \frac{V_{dc}}{2}(m_3 - m_4 + 1) \\ V_{CO} &= \frac{V_{dc}}{2}(m_5 - m_6 + 1) \end{aligned} \tag{B.13}$$

The expression for current continuity from each half bridge of inverter is shown below:

$$\begin{aligned} m_1 + m_2 &= 1 \\ m_3 + m_4 &= 1 \\ m_5 + m_6 &= 1 \end{aligned} \tag{B.14}$$

On solving (B.13) and (B.14) gives:

$$\begin{aligned} V_{AO} &= V_{dc} m_1 \\ V_{BO} &= V_{dc} m_3 \\ V_{CO} &= V_{dc} m_5 \end{aligned} \tag{B.15}$$

Since the algebraic sum of three-phase current is 0, the dc-link current can be expressed as in (B.17)

$$i_A + i_B + i_C = 0 \tag{B.16}$$

$$I_{dc} = i_A m_1 + i_B m_3 + i_C m_5 \tag{B.17}$$

The product of this I_{dc} and V_{dc} gives the input power. The three-phase line to line voltages and line to neutral (phase) voltages can be given by:

$$\begin{aligned} V_{AN} &= V_{AO} - V_{NO} \\ V_{BN} &= V_{BO} - V_{NO} \\ V_{CN} &= V_{CO} - V_{NO} \end{aligned} \tag{B.18}$$

where V_{NO} is the voltage between neutral of the motor and dc-link ground. It is also know as common mode voltage which is expressed as below:

$$V_{NO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \tag{B.19}$$

On solving (B.18) and (B.19), the phase voltage will become:

$$\begin{aligned} V_{AN} &= V_{dc}\left(\frac{2}{3}m_1 - \frac{1}{3}(m_3 + m_5)\right) \\ V_{BN} &= V_{dc}\left(\frac{2}{3}m_3 - \frac{1}{3}(m_1 + m_5)\right) \\ V_{CN} &= V_{dc}\left(\frac{2}{3}m_5 - \frac{1}{3}(m_1 + m_3)\right) \end{aligned} \tag{B.20}$$

From the equation above it can be observed that, the common mode voltage may be present in the pole voltage, but has no effect on the motor current. It is phase voltage components which is actually producing the motor phase current. The expressions in (B.20) can be used for defining the switching functions of two-level inverter in any reference frame.

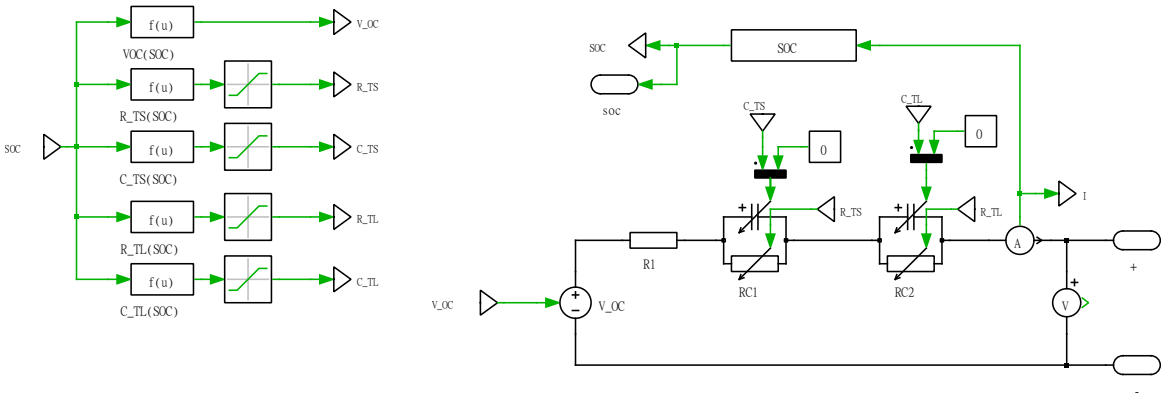


Figure B.1: RC-chain-based Li-ion model

B.5 Li-ion battery modeling

Li-ion batteries are often modeled as ideal constant voltage source circuits. However, as the battery is charged and discharged, the current and voltage (I-V) of the battery changes. These effects are not reflected in the models with a constant voltage source. To optimize the overall system performance, the I-V characteristics of the battery are considered. Further, the model can be used to analyze different charging and state-of-charge (SOC) estimation algorithms [145]. In the thesis RC circuit-based Li-ion cell model is considered as shown in Fig. B.1 .This Li-ion model consists of a SOC-dependent electrical circuit using RC-chains to enable battery transient behavior modeling during load current step changes. The implementation using multiple RC-chains provides better accuracy. However, this may add to the model's complexity and adversely affects the real time simulation speed [146], [147].

Appendix C

PWM Generation

C.1 Two-level PWM generation

In a single two-level inverter space vector, the active vectors are separated by 60^o and divide the polygon into six equal sectors. The tips of the active vectors when joined together form a space vectors hexagon. Any voltage reference vector, inside

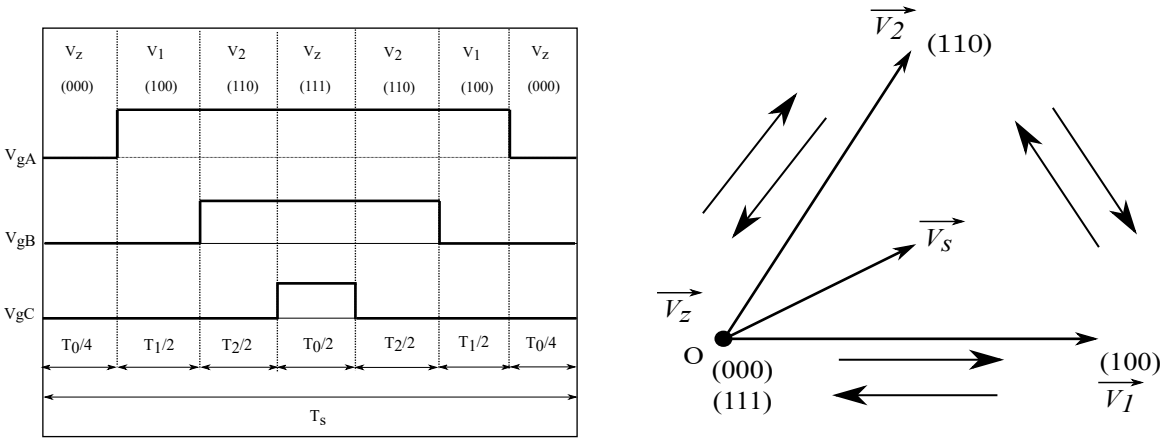


Figure C.1: Switching sequence for sector-I in continuous modulation

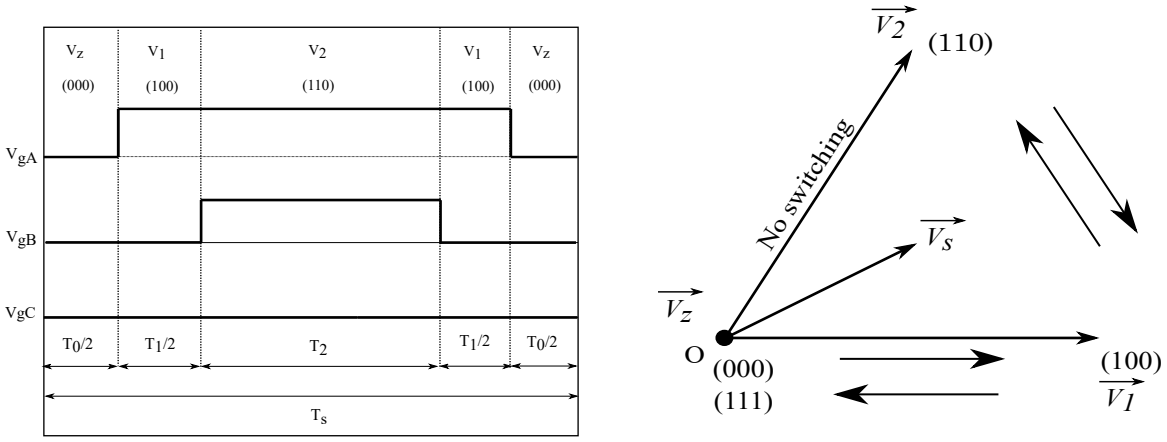


Figure C.2: Switching sequence for sector-I in discontinuous modulation

a hexagonal sector, can be generated using the available vectors of the sector. In the first sector the switching sequences for continuous modulation and discontinuous (60^o clamp) can be illustrated as in Fig. C.1 and C.2. The T_s is the total switching time. T_1 and T_2 are the active vector dwell time and T_z is the zero vector dwell time.

The equation for generating the modulating waves in carrier based continuous modulation can be expressed as below:

$$\begin{aligned} T_x &= \frac{T_s}{V_{dc}} v_x; x = a, b, c \\ T_{max} &= max(T_a, T_b, T_c) \\ T_{min} &= min(T_a, T_b, T_c) \\ T_{eff} &= T_{max} - T_{min} \\ T_0 &= T_s - T_{eff} \\ T_{offset} &= \frac{T_0}{2} - T_{min} \\ T_{xs} &= T_x + T_{offset}; x = a, b, c \end{aligned} \tag{C.1}$$

In the above expressions the T_{xs} gives the modulating signals which are then compared to the high frequency carrier wave. In discontinuous modulation, the modulating waves can be obtained by modifying the equation in C.1 as expressed below:

$$\begin{aligned} T_{H_{clamp}} &= T_s - T_{max} \\ T_{L_{clamp}} &= -T_{min} \\ T_{comp} &= T_{max} > T_{min} \\ T_{offset} &= (T_{H_{clamp}} - T_{L_{clamp}}).T_{comp} \\ T_{xs} &= T_x + T_{offset}; x = a, b, c \end{aligned} \tag{C.2}$$

C.2 Three-level PWM generation with single carrier

The carrier based modulation technique used for the two-level inverter can be extended to generate the gating signals for the three-level inverter. The main problem in digital implementation is to handle the multiple level shifted carriers as shown in Fig. C.3. One technique to solve this problem is by splitting the modulating wave and translating to one carrier. It can be seen from Fig. C.3 that the upper

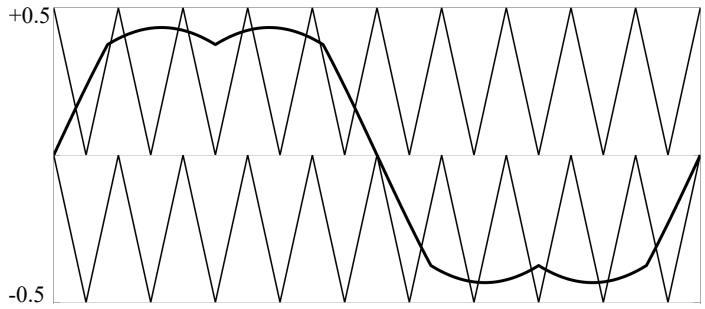
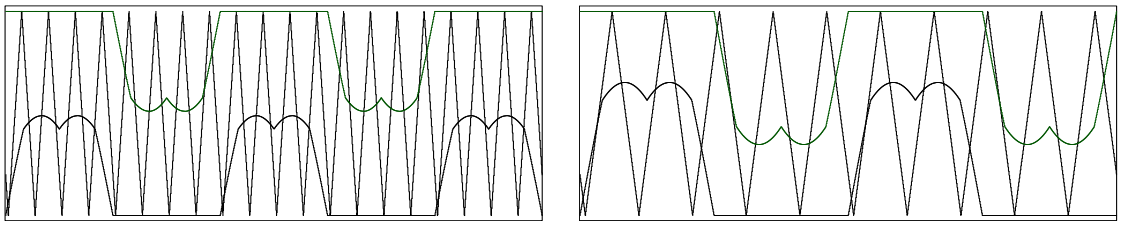


Figure C.3: Modulating and carrier wave for three-level PWM generation



(a) (b)

Figure C.4: Splitting of modulating wave equally in lower and higher M.

and lower half of the modulating wave is compared to a particular portion in both carriers, and other portions in the respective carrier remain unused. Therefore the modulating wave can be split into two independent parts and compared to a single carrier as shown in Fig. C.4. In the figure the black wave generates PWM signal for A_1 phase leg in Inverter-1 and green wave generates PWM signal for A_2 phase leg in Inverter-2. The zero crossing of each independent wave will be clamped to either side of the carrier and comparison logic for both waves will be opposite. For better understanding, A_1A_2 phase modulating wave is compared with carriers at a reduced frequency.

Fig. C.5(a) to C.5(d) shows the simulation and digital implementation of modulating wave when Inverter-1 is feeding more power in lower and higher M respectively. It can be observed that for lower M, the modulating wave comparison is similar to conventional method, keeping the other wave clamped to provide zero vectors. When the modulation index is higher, black wave is compared to full portion of the carrier, whereas the green wave is compared to less portion of the carrier. For $M = 1$, the sharing will be equal and both waves will be equally displaced in the carrier as shown in Fig. C.5(e) and C.5(f). The gate pulses for top switches of the two individual inverters in phase A_1A_2 are shown in Fig. C.6

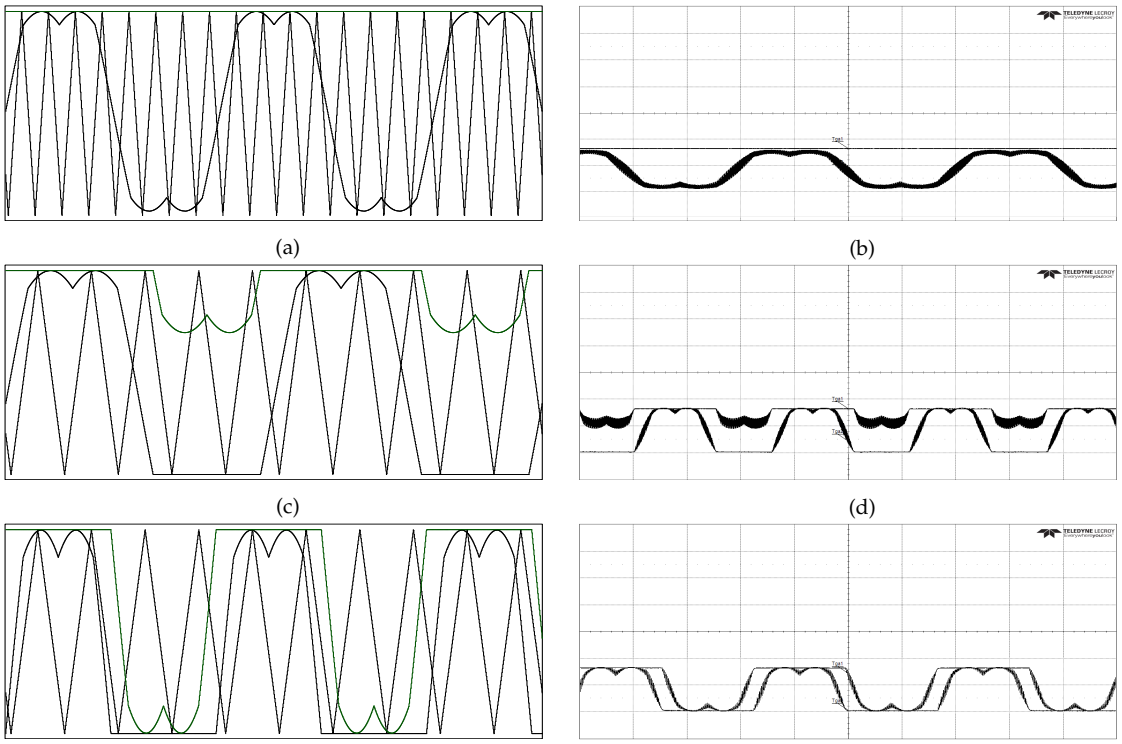


Figure C.5: Simulation and digital generation of modulating wave. (a) and (b) Modulating wave at lower M. (c) and (d) Modulating wave at higher M. (e) and (f) Modulating wave at $M = 1$

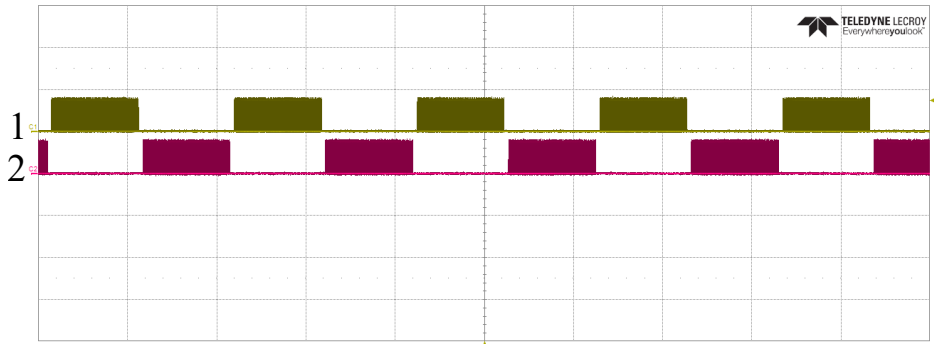


Figure C.6: Pulses for top devices in phase A_1A_2.

C.3 Sector and sub-sector identification in three-level space vector

The Fig. C.7 shows the three-level space vectors structure. It can be seen that A-phase is aligned to α-axis, i.e. α-axis corresponds to 90^0 of A-phase. The sectors are equally divided by 60^0 angle and equal sub-sectors are sequentially numbered. The three-phase reference voltage can be obtained from V_α and V_β reference voltage values using standard inverse-Clarke transformation. The Fig. C.8 shows the three-phase voltages along the sector information. From relative values of the three-phase voltages in the different sectors, the sector detection logic can be summarized as in Table C.1.

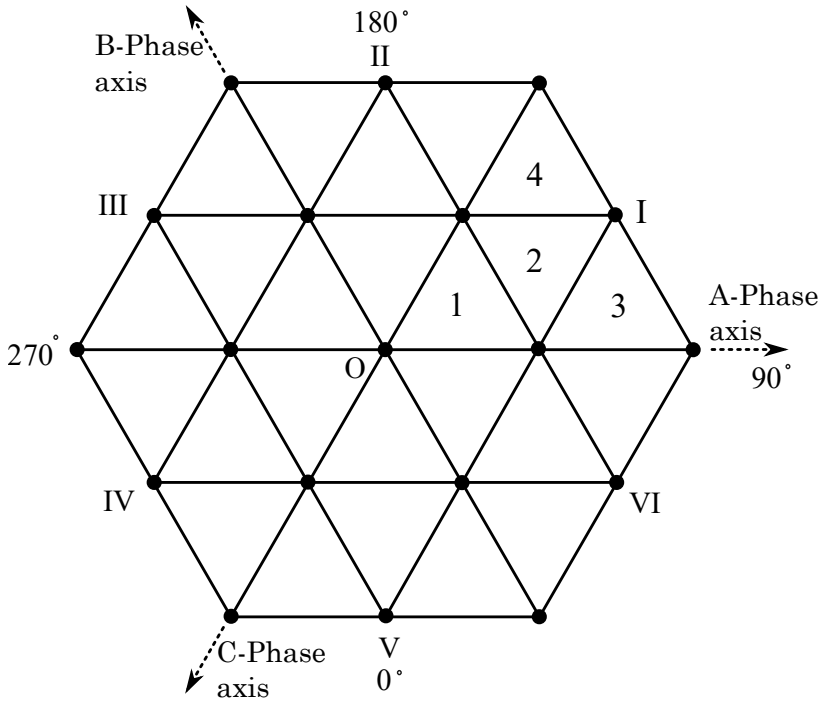


Figure C.7: Three-level space vector aligned to α-axis.

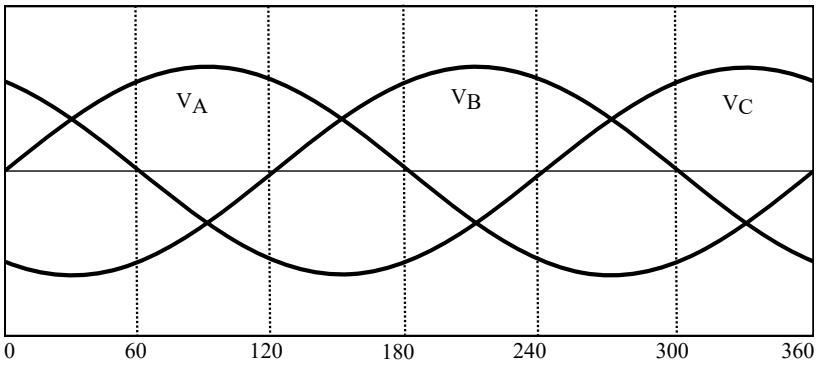


Figure C.8: Three phase reference voltages and corresponding sectors.

Table C.1: Sector detection logic.

Condition	Sector
V_A>V_B>V_C	I
V_B>V_A>V_C	II
V_B>V_C>V_A	III
V_C>V_B>V_A	IV
V_C>V_A>V_B	V
V_A>V_c>V_B	VI

Table C.2: Sub-sector detection logic.

Condition	Sub-sector
(T_1+T_2)<$T_s/2$	1
T_1>$T_s/2$	2
T_1>$T_s/2$	3
(T_1+T_2)>$T_s/2$	4

In space vector based PWM generation, the dwell time of the switching vectors represents the duty-cycle time. The dwell timing of vectors in each sector can be calculated based on volt-second balance. Different methods can be used to get the

active vector dwell times. The vector timings for desired sectors and sub-sectors can be computed offline and stored in a lookup table. Only timings corresponding to one sector need to be stored, as all sectors are equilateral triangles and have same active vector timings for the same relative position of the reference voltage vector. Depending on the values of active vector dwell time (T_1, T_2) and sampling time (T_s), the sub-sector information can be summarized as in Table C.2.

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