Soft-switched, Active-clamped DC/AC and AC/AC Converters for IPT-based Wireless Charging Applications

by

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

ABSTRACT

The acquisition of inductive power transfer (IPT) technology in commercial electric vehicles (EVs) alleviates the inherent burdens of high cost, limited driving range, and long charging time. In EV wireless charging systems using IPT technology, power electronic converters play a vital role to reduce the size and cost, as well as to maximize the efficiency of the overall system. Conventionally, the IPT systems utilize two power conversion stages to generate a high-frequency primary current/voltage from low-frequency utility supply, causing the lower power density and higher cost of the system. Recent research shows that the use of direct AC/AC converters in the IPT systems can mitigate these limitations. However, these topologies still have the drawbacks such as large switching component count, poor input current quality, or complex control schemes.

In this thesis, a novel direct AC/AC active-clamped half-bridge (HB) converter for the wireless EV IPT charging application is proposed and implemented. The proposed converter can overcome the aforementioned limitations of the existing power converter topologies. It offers several appealing features such as high efficiency, less component requirement, continuous sinusoidal input current, and zero voltage switching (ZVS) operation. Moreover, a new simple hybrid (nonlinear and linear) dual-loop control strategy for the AC/AC active-clamped HB converter based IPT charging system is developed. It enables the input current correction and charging current regulation in a single power conversion stage. The performance of the proposed charging system is verified by simulation and experimental results on a 1.0-kW prototype. The experimental verification shows that the proposed IPT system with a peak overall efficiency of 93.4 % is more efficient than the existing single-stage converter based IPT systems. In order to have a knowledge foundation for the successful analysis, design and implementation of the proposed AC/AC converter system, an active-clamped half-bridge boost inverter (HBBI) based IPT charging system is initially studied. The ZVS operation principles, mathematical model, design methodology, and control strategy of the active-clamped HBBI based system are derived and developed in detail. Simulation and experimental results are given to verify the theoretical analyses and system performance.

Keywords: AC/AC converter; active-clamped circuit; DC/AC inverter; EV charger; inductive power transfer.

AUTHOR'S DECLARATION

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STATEMENT OF CONTRIBUTIONS

Part of the work described in Chapter 1, 2, and 3 has been published as:

[1] **P. S. Huynh**, D. Ronanki, D. Vincent, and S. S. Williamson "Overview and comparative assessment of single-phase power converter topologies of inductive wireless charging systems," *Energies,* vol. 13, no. 9, 2020.

I performed the majority of the synthesis, testing of membrane materials, and writing of the manuscript.

[2] **P. S. Huynh**, D. Ronanki, S. S. Williamson, “Power electronics for wireless charging of future electric vehicles” in Emerging power converters for renewable energy and electric vehicles, *CRC press.* (Accepted)

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LIST OF ABBREVIATIONS

AC	Alternating current
APT	Acoustic power transfer
CC	Capacitor-capacitor
CC-CV	Constant-current constant-voltage
CPT	Capacitive power transfer
CSI	Current-source inverter
DC	Direct current
DCM	Discontinuous conduction mode
EDF	Extended describing function
EMF	Electromagnetic field
EMI	Electromagnetic interference
EV	Electric vehicle
FB	Full-bridge
FBMC	Full-bridge matrix converter
G2V	Gird-to-vehicle
GA	Ground assembly
GHG	Greenhouse gas

HB	Half-bridge
HBBI	Half-bridge boost inverter
ICE	Internal combustion engine
IIR	Infinite impulse response
IPT	Inductive power transfer
LCCL	Inductor-capacitor-capacitor-inductor
LCL	Inductor-capacitor-inductor
MC	Matrix converter
MCC	Multi-step constant-current
MPET	Maximum efficiency point tracking
MPPT	Maximum power point tracking
OPT	Optical power transfer
PCB	Printed circuit board
PFC	Power factor correction
PP	Parallel-parallel
PS	Parallel-series
PV	Photovoltaic
PWM	Pulse-width modulation

RFPT	Radio frequency power transfer
RHP	Right-hand-plane
SAE	The Society of Automotive Engineers
SiC MOSFET	Silicon-carbide metal-oxide-field-effect transistor
SP	Series-parallel
SS	Series-series
THD	Total harmonic distortion
V2G	Vehicle-to-grid
VA	Volt-amp
VSI	Voltage-source inverter
WPT	Wireless power transfer
ZCS	Zero current switching
ZVS	Zero voltage switching

LIST OF SYMBOLS

Chapter 2

η	Efficiency
i_p	Primary current
i_s	Secondary current
L_p	Primary inductance
L_s	Secondary inductance
M	Mutual inductance
P_L	Output power
R_L	AC load resistance.
r_p	Internal resistance of primary coil
r_s	Internal resistance of secondary coil
v_{Lp}	Voltage across the primary coil
ω	Angular frequency of v_{Lp}
Z_{eq}	Reflected impedance from the secondary side to primary side
Z_p	Primary coil impedance
Z_s	Secondary equivalent impedance
Z_t	Total impedance seen from the primary side end

Chapter 3

C_{dc}	DC-link capacitor
C_g	Grid filter capacitor
C_o	Output filter capacitor
C_p	Primary compensation capacitor in SS compensation network

C_{pp}	Parallel capacitor of parallel-series CC compensation network
C_{ps}	Series capacitor of parallel-series CC compensation network
C_s	Secondary compensation capacitor in SS compensation network
D_p	Duty cycle of primary voltage
f_s	Switching frequency
k	Coupling coefficient
L_g	Grid filter inductor
L_i	Boost inductor of PFC
L_p	Primary inductance
L_s	Secondary inductance
M	Mutual inductance
P_o	Output power
V_b	Battery voltage
V_{dc}	DC-link voltage
V_g	RMS value of grid voltage
v_p	Primary voltage
v_s	Secondary voltage
ω_s	Angular switching frequency

Chapter 4 and 5

C_i	Clamping capacitor
C_o	Output filter capacitor
C_{oss1}, C_{oss2}	Output capacitors of upper and lower switches
C_p	Primary compensation capacitor
C_s	Secondary compensation capacitor

D	Duty cycle of HBBI
ΔI_{Li}	Input current ripple
ΔV_{Ci}	Clamping voltage ripple
f_s	Switching frequency
η	Efficiency
i_{Ci}	Clamping capacitor current
I_{Li}	Input current
I_o	Output current
i_p	Primary current
i_s	Secondary current
k	Coupling coefficient
L_i	Boost inductor of PFC
L_p	Primary inductance
L_s	Secondary inductance
M	Mutual inductance
P_o	Output power
Q_s	Secondary quality factor
r_b	Internal battery resistance
t_d	Dead time
V_b	Battery voltage
V_{Ci}	Clamping voltage
v_{Cp}	Primary compensation capacitor voltage
v_{Cs}	Secondary compensation capacitor voltage
V_i	Input voltage
V_o	Output voltage
v_p	Primary voltage
v_s	Secondary voltage

ω_p	Angular primary resonant frequency
ω_s	Angular switching frequency
Z_{eq}	Reflected impedance from the secondary side to primary side

Chapter 6 and 7

C_i	Clamping capacitor
C_o	Output filter capacitor
C_p	Primary compensation capacitor
C_s	Secondary compensation capacitor
ΔI_m	Maximum input current ripple
d_p	Duty cycle of active-clamped AC/AC converter
D_{pm}	Minimum duty cycle of active-clamped AC/AC converter
d_s	Duty cycle of secondary rectifier
ΔV_c	Maximum clamping voltage ripple
f_s	Switching frequency
η	Efficiency
I_b	Battery current
i_i	Input current of active-clamped AC/AC converter
I_m	Peak input current
i_p	Primary current
i_s	Secondary current
L_i	Input inductor
L_p	Primary inductance
L_s	Secondary inductance
M	Mutual inductance
P_o	Output power
θ	Phase displacement between primary and secondary voltage
T_s	Switching period

V_b	Battery voltage
v_{Ci}	Clamping voltage
V_{cm}	Peak clamping voltage
v_i	Input voltage of active-clamped AC/AC converter
V_m	Peak input voltage
v_p	Primary voltage
v_s	Secondary voltage
ω_s	Angular switching frequency

Chapter 1. Introduction

1.1 Wireless Power Transfer

Wireless power transfer (WPT) enabling transferring energy from a source to a load without electrical contact has been extensively studied and successfully demonstrated using various techniques namely acoustic power transfer (APT) [1, 2], radio frequency power transfer (RFPT) [3, 4], optical power transfer (OPT) [5, 6], capacitive power transfer (CPT) [7], and inductive power transfer (IPT) [8]. The WPT techniques are differentiated based on their power transfer medium; however, their system configuration is similar. It basically comprises a power source, a load, a coupler, and primary/secondary electronic circuits. The WPT systems can be powered by a utility AC or DC supply, and their loads vary from AC to DC depending on different applications. For example, an induction-heating load is AC, whereas a wireless battery charging system has a DC load. The WPT coupler including a transmitter and a receiver is different for different WPT technologies. The couplers of the APT, RFPT and OPT systems are Piezo transducers, antenna/rectenna, and laser diode/photovoltaic diode, respectively. For the CPT and IPT systems, their mutual couplings are formed by metal plates and inductive coils, respectively. The primary and secondary electronic circuits are usually composed of power electronic converters (inverters, rectifiers, and DC/DC converters…) and compensators. In the CPT and IPT systems, the compensators are *LC* circuits which play an important role in achieving reactive power compensation, unity power factor, low volt-amp (VA) rating, low electromagnetic interference (EMI), high power transfer capability, and high efficiency [9-11]. The compensators in the RFPT systems are the RF resonant circuits or filters, while the DC filters or current balancing circuits are the compensators in the OPT systems.

Among aforementioned WPT technologies, the IPT technology has been recognized in many applications such as implantable devices [12-14], home appliances [15, 16], and mobile phones [17, 18]. Especially, it has been proven that the IPT technology is the most suitable for the EV charging applications where the output power is from few to several kilowatts, and the air gap varies from a few centimeters to a few meters [19, 20]. Recently, researchers and engineers have been fitting the outcomes of the IPT to the EV battery charging systems in various commercial products (Witricity [21], Qualcomm [22], Evatran/Plugless Power [23], Brusa [24], and Momentum Dynamics [25], etc.) and standards [26-29]. The EV charging systems using the IPT technology are focused in this thesis.

1.2 Necessity of Wireless Charging Systems for Electric Vehicles

Vehicular emissions across the globe are rapidly increasing, contributing a significant portion of global greenhouse gas (GHG) emissions, and causing the climate change. In Canada, the transportation sector was the second largest source of the GHG emissions, occupying 24.3% (equivalent 174 megatons (Mt) of carbon dioxide) of the total emissions in 2017 [30], as shown in Figure 1.1. Alternative to conventional internal combustion engine (ICE) vehicles, the EVs can be considered as a promising solution to reduce the emissions in transportation [31]. In the recent year, the wide adoption of the renewable energy sources in power production has been even making the EVs gain more attentions due to possible zero-emission achievement [32, 33]. In March 2019, one of globally leading EV manufacturers, Nissan, reported that its Nissan Leaf owners worldwide achieved the mileage of over 10 billion kilometers, and saved 3.8 million barrels of oil per year since 2010 [34].

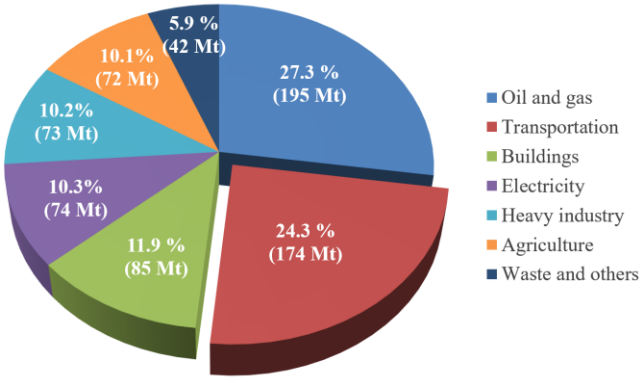


Figure 1.1: GHG emissions of the economic sectors in Canada in 2017.

In order to achieve a greater commercial success for the EVs, their main inherent drawbacks such as bulky and costly energy storage unit, and long charging time must be addressed. The primary energy source of the EVs is the battery that should have high energy and power density, reliability, safety, and long lifespan. Although the lithium-ion batteries with the high energy density (100-265 Wh/kg) and power density (250-340 W/kg) are being commonly used in the EVs, the battery packs are still significantly heavy and cumbersome [35]. For instance, the 24-kWh battery pack of Nissan Leaf is around 200 kg, and the 85-kWh battery pack of Tesla Model S weighs 540 kg. Moreover, the high cost of the battery packs, approximately $180/kWh - $350/kWh, makes the EVs less affordable compared to the conventional ICE counterparts. Constantly, the driving range of the EVs has been extended. Modern electric cars such as Chevrolet Bolt, Kia Niro EV, and Hyundai Kona Electric offer the range of nearly 250 miles on a single charge; even Tesla Model S can achieve 370-mile range, which is comparable to the gasoline vehicles. Nevertheless, recharging the EVs usually takes from an hour to several hours depending on the how full the battery pack is and the type of chargers that is used. It is much longer than refueling the gasoline vehicles, which takes only few minutes. For example, it takes four hours to charge the 24-kWh battery pack of the Nissan Leaf from empty to full with a Level-2 home charger (7.7 kW). In addition, EV charging stations are not as widely accessible as gas stations.

Wireless chargers using IPT technology can mitigate the aforementioned issues [19, 36-43]. With the fully-automated wireless chargers, the EVs can obtain more opportunity charging, which allows charging the EVs little and often during the day when they are not employed [44]. As a result, the deep discharge on the battery can be avoided with the EVs' driving range extension [45]. Moreover, a 20-percent reduction of the battery capacity requirement can be achieved through the opportunity charging techniques, which consequently reduces the weight and price of the EVs [46]. The wireless chargers can be deployed in residential garages, and office/service/shopping center parking lots for static wireless charging [47], or they can be placed at bus stops, taxi ranks, and traffic lights to implement quasi-dynamic wireless charging [48, 49]. Moreover, dynamic wireless charging systems can be installed on the roads to constantly charge the EVs, in turn to extend the driving range and reduce the battery volume of the vehicles [50-52]. Additionally, the wireless chargers are safe and convenient because they have inherent galvanic isolation, and enable WPT via an air gap between the power source and the vehicles without any direct electrical contacts. As a result of that, long electric cables between the charging points and the vehicles are removed in the wireless chargers, which eliminates the drawbacks of the conventional plug-in chargers, e.g., plug-in failure, tripping hazards, and the risk of electrocution due to aging or eroded cables/connectors [42]. Last but not least, the wireless charging process is not unaffected by hostile environment because the power transfer takes place through an electromagnetic link where the transmitting pad can be buried underground. Consequently, the wireless chargers are safe in extreme weather conditions such as rain or snow, and require less maintenance or replacement [36, 53].

Compared to the conventional conductive charging systems, the main drawback of the wireless charging systems is the high initial investment in the infrastructure including road construction, installation work, constituent materials and components, etc. However, this high initial cost can be significantly reduced by optimizing design and planning for the charging infrastructure (number and locations of wireless chargers, power level, and transmitter length) [54]. Additionally, this large initial cost can be compensated by the battery size reduction and driving range extension [55].

1.3 EV Wireless Charging Standards

Recently, SAE J2954 [26], IEC 61980 [28], and ISO 19363 [29] are available standards for the EV wireless charging application, and they have many common points. In this thesis, the wireless charging prototypes are designed following the standard SAE J2954. The standard SAE J2954 is established by the Society of Automotive Engineers (SAE), a global association based in the United States. Its essential role is to develop international standards for industry, especially in the transportation sector. It has recently involved over 128,000 global members who are engineers and experts in the aerospace, automotive and commercial vehicle areas. The standard SAE J2954 is developed to define criteria for interoperability, electromagnetic compatibility, electromagnetic field (EMF), minimum performance, safety, and testing for static wireless charging of light-duty EVs.

Table 1.1 shows the power classes, operating frequency and efficiency performance targets of the WPT systems specified in the SAE J2954. As can be seen from Table 1.1, four WPT classes are defined based on the maximum input VA drawn from the grid by the primary side/ground assembly (GA) electronics. The input real power depends on the input power factor, while the output power depends on the efficiency of the system. The SAE J2954 also specifies that the WPT systems should be operated at a single nominal frequency of 85 kHz. However, for the WPT systems using frequency control to compensate system variations, their operating frequency must be in the band of 81.38 to 90.00 kHz. The interoperability requirements among the WPT classes are shown in Table 1.2. It can be explained that the primary and secondary coils of the WPT 1 and WPT 2 systems are necessarily compatible, whereas the WPT 3 primary coils must be compatible with the WPT 2 secondary coils. There are no interoperability requirements for the WPT 4 coils. Another important specification of the WPT systems is the air gap between the primary and secondary coils. Although it is not exactly specified in SAE J2954, but can be estimated from the Z classification which is defined based on the secondary or vehicle assembly coil ground clearance, as shown in Table 1.3.

In this thesis, the developed wireless charging prototypes comply with SAE J2954 in terms of operating frequency (85 kHz), coil air gap (Z2), and efficiency (> 93%). Although their output power is only 1.0 kW, it can be scaled up to the power levels specified in SAE J2954.

Table 1.1: WPT power classifications for light duty vehicles

WPT power classes	**1**	**2**	**3**	**4**
Maximum AC input power (kVA)	3.7	7.7	11.1	22
Minimum target efficiency at nominal alignment (%)	> 85	> 85	> 85	TBD
Minimum target efficiency at offset position (%)	> 80	> 80	> 80	TBD
Operating frequency (kHz)	81.38 – 90 (typical 85)			

Table 1.2: Interoperability by power class

Secondary coils **Primary coils**		**WPT classes**			
		WPT 1	WPT 2	WPT 3	WPT 4
WPT classes	WPT 1	Required	Required	Optional	Optional
	WPT 2	Required	Required	Optional	Optional
	WPT 3	Optional	Required	Required	Optional
	WPT 4	Optional	Optional	Optional	Required

Table 1.3: Z-classes specifications

Z-class	**VA coil ground clearance range (mm)**
Z1	100 – 150
Z2	140 – 210
Z3	170 – 250

1.4 Purpose of the Thesis

1.4.1 Motivations

In recent years, the wireless EV charging systems via the IPT technology have been intensively studied, and their performance has been continuously improved. However, those systems have still needed further improvements regarding cost, deployment, efficiency, infrastructure, interoperability, and magnetic field emissions before gaining wide commercial acceptance. The research aspects of the IPT systems are 1) Power converters 2) Inductive coil design, 3) Compensation network topologies, 4) Control system, 5) EMI shielding methods, and 6) Communication.

Power electronic converters play a vital role in the IPT-based EV charging systems regarding maximizing the system efficiency, power density, and cost-effectiveness. Nowadays, most IPT systems are directly supplied from the mains, thus a front-end AC/DC rectifier and an inverter are required to generate a high-frequency current/voltage exciting the IPT systems. Those power supply topologies take large installation space and may unnecessarily increase cost. It is desirable but challenging to design structurally simple and compact power supplies with high performance. Some power-conversion-stage-reduction topologies have been proposed for the IPT charging systems to alleviate the limitations, as presented in Chapter 2 and 3. However, they still have drawbacks, e.g., large switching component count, discontinuous input current leading to a bulky input filter, or high control complexity. These issues are the main motivations of this thesis to develop a new single-stage AC/AC converter that has high efficiency, simple structure, low component count, and low control complexity to improve the overall performance of the IPT charging systems.

1.4.2 Research Goals and Objectives

Many review studies including charging standards, coil structures, power converters, and compensation networks for both static and dynamic wireless charging have been reported in the literature [40, 42, 43, 53, 56-59]. However, design considerations and comparative analysis focusing on the power converter topologies for the wireless charging systems have not been discussed in detail. This thesis initially aims to fill this gap by providing the detailed design procedure of the widely used dual-stage and single-stage power conversion topologies in the IPT charging application. Then a comprehensive comparison of their performance is presented to provide a deeper understanding of their properties and constraints, which is useful for engineers to design better IPT charging systems. Consequently, by considering the limitations of the existing power converter topologies, a novel direct AC/AC active-clamped half-bridge converter with several benefits such as less component requirement, high-quality input current, and low control complexity is developed and implemented in this thesis. Before exploring the proposed AC/AC converter, an active-clamped HBBI based IPT charging system has been investigated with operation principles, modeling, design methodology and control strategy to create a foundation for analysing the proposed AC/AC converter system.

Review, design and comparative assessment of the existing power supply converter topologies for the EV IPT charging systems. An extensive overview of single-phase power conversion topologies employed in the EV wireless charging applications is presented. Then, the design procedure and performance comparison of the common topologies including conventional dual-stage (power factor correction (PFC) and full-bridge voltage-source inverter (FB VSI)), single-stage buck-derived full-bridge matrix converter (FBMC), and single-stage boost-derived FBMC are provided. The comparison involves the input power factor, input current distortion, power losses, switching stress, and normalized cost, while taking into account the requirements of Standard J2954. It concludes that the buck-derived FBMC surpasses the other counterparts with the advantages of high efficiency, less component count and cost reduction. On the other hand, the conventional dual-stage topology has the low stress on switching devices, and maintains a comparable efficiency over wide load range. Although the single-stage converter topologies have the advantage of the DC-link capacitor removal and cost reduction, they still require many active switches and complex control schemes. A novel direct AC/AC active-clamped HB converter is proposed in this thesis will address these issues.

Analysis, design, and control of soft-switched, active-clamped HBBI for the IPT charging system. A comprehensive investigation on the IPT charging system fed by the active-clamped HBBI is realized. Firstly, the ZVS operation principles of the active-clamped HBBI in the IPT charging system are presented. Then, both the steady-state model and the small-signal model are correctly derived using the extended describing function (EDF) method. The derived steady-state model is employed to develop a new design approach to achieve zero-voltage switching (ZVS) for the inverter. The proposed ZVS design methodology enables not only reducing switching losses but also avoiding bifurcation. The dynamic behavior of the system is investigated based on the derived small-signal model, and then a digital controller is designed to regulate the charging current. Simulation and experimental results on a 1.0-kW laboratory prototype are provided to verify the accuracy of the theoretical analyses. Also, the experimental results demonstrate that the developed controller can effectively regulate the charging current with a fast response and no steady-state errors, and the inverter can achieve ZVS over a wide variation of the charging current and the battery voltage. The hardware prototype achieves a peak DC-to-DC efficiency of 93.4% at a 170-mm air gap.

Analysis, design, and control of direct AC/AC active-clamped half-bridge converter for the IPT charging system. A new direct AC/AC active-clamped half-bridge converter feeding the IPT charging system is proposed. The proposed converter eliminates the rectification stage, resulting in an actual single-stage (AC-to-AC) conversion with less the number of switching devices. Furthermore, it avoids the use of bulky life-limited electrolytic DC-link capacitors. Based on the analyses on active-clamped HBBI for the IPT charging system, the operation principles, steady-state model, and design considerations of the proposed AC/AC converter are explored. Moreover, a new hybrid control scheme combining a predictive dead-beat controller for grid current correction and a linear average charging current controller is developed for the proposed converter. It enables the power factor correction and charging current regulation in a single conversion stage. The performance of the proposed IPT charger is validated through simulation and experimental results on a 1.0-kW laboratory prototype. It is observed that the battery charging current is effectively controlled, and the unity power factor is obtained under the variation of the charging current command, the battery voltage, mutual inductance, compensation capacitors. The input current harmonic content complies with the IEC 61000-3-2 Class A standard. Due to single-stage-power-conversion and soft-switching features, the proposed charging system achieve the maximum overall (AC-to-DC) efficiency of 93.4 %, which is higher than that of the dual-stage converter based and single-stage converter based IPT systems reported in literature.

1.5 Thesis Outline

Chapter 1: It includes an overview of the WPT technologies, the reasons of adopting wireless IPT charging for the EVs, and the basic specifications of the static wireless EV charging systems defined in the Standard SAE J2954. The statements of the main research motivations, goals and objectives are also presented in this chapter.

Chapter 2: It provides an overview of the structure of the IPT systems. The compensation networks, inductive coupling structures, power converter topologies and control strategies of the IPT systems are reviewed.

Chapter 3: It describes the design considerations and comprehensive simulation assessment of the conventional dual-stage (PFC+VSI) topology and the single-stage counterparts including the buck-derived FBMC and boost-derived FBMC in the EV IPT charging application.

Chapter 4: The theoretical background of the proposed AC/AC active-clamped half-bridge converter is initially established through an investigation on the active-clamped HBBI based IPT charging system. In Chapter 4, the detailed operation principles, modeling analysis, and design methodology of the active-clamped HBBI based IPT charging system are given.

Chapter 5: In this chapter, the simulation and experimental results on a 1.0-kW active-clamped HBBI based IPT charging prototype with a developed closed-loop current controller are given to verify the theoretical analyses and design methodology presented in Chapter 4.

Chapter 6: Based on the foundation provided in Chapter 4, the operation principles, steady-state model, and design procedure of the proposed AC/AC active-clamped half-bridge converter are established in detail in Chapter 6.

Chapter 7: In this chapter, a hybrid dual-loop control strategy composed of the predictive dead-beat current control and the linear average current control is developed for the IPT charging system fed by the direct AC/AC active-clamped half-bridge converter. The feasibility and performance of the proposed controller are verified by simulation and experimental results.

Chapter 8: It concludes the thesis with a summary of the accomplishments, and an outlook on possible future work.

Chapter 2. Background and Literature Review

An IPT charging system essentially comprises an inductive coupling coil pair, compensation networks, primary converters to generate high-frequency inputs, and a secondary rectifier to convert AC to DC current to charge the battery. In this chapter, an overview of the existing compensation configurations, inductive coupling structures, primary conversion topologies, and power control strategies for the EV IPT charging systems are presented.

2.1 Compensation networks

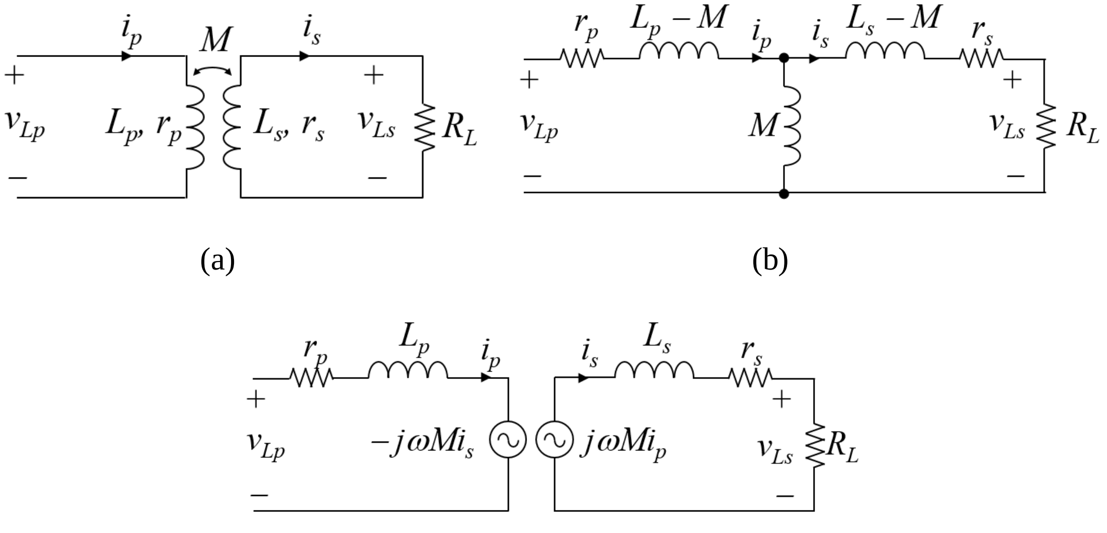
Figure 2.1 illustrates the electric circuit of an inductive coupler and its equivalent models, which are T-circuit and mutual inductance models [60], where L_p and L_s are the self-inductances of the primary (transmitting) and secondary (receiving) coils, r_p and r_s are their parasitic resistances, M is the mutual inductance between two coils, and R_L is the AC load resistance.

Assume that the primary coil is excited by a sinusoidal voltage v_{Lp} with angular frequency ω. The steady-state equations in the phasor domain can be obtained from the equivalent circuits as follows

$$\dot{V}_{Lp} = r_p \dot{I}_p + j\omega L_p \dot{I}_p - j\omega M \dot{I}_s \tag{2.1}$$

$$j\omega M \dot{I}_p = j\omega L_s \dot{I}_s + r_s \dot{I}_s + R_L \dot{I}_s \tag{2.2}$$

where $\dot{V}_{Lp}$ is the voltage across the primary coil, $\dot{I}_p$ and $\dot{I}_s$ are the currents flowing in the primary and secondary coils, respectively.



(a) (b)

(c)

Figure 2.1: Inductive coupler. (a) Electric circuit, (b) Equivalent T-circuit model, and (c) Equivalent mutual inductance model.

From (2.2), the equations (2.3) and (2.4) can be derived as follows

$$\dot{I}_p = \frac{\dot{I}_s Z_s}{j\omega M} \tag{2.3}$$

$$\frac{\dot{I}_s}{\dot{I}_p} = \frac{j\omega M}{Z_s} \tag{2.4}$$

where $Z_s = r_s + R_L + j\omega L_s$ is the secondary equivalent impedance.

Substitution of (2.3) in (2.1) results in

$$\dot{I}_s = \frac{j\omega M}{Z_p Z_s + \omega^2 M^2} \dot{V}_{Lp} \tag{2.5}$$

where $Z_p = r_p + j\omega L_p$ is the primary coil impedance.

Then, the output power is derived as follows

$$P_L = \left|\dot{I}_s\right|^2 R_L = \frac{\omega^2 M^2 \left|\dot{V}_{Lp}\right|^2}{\left|Z_p Z_s + \omega^2 M^2\right|^2} R_L \tag{2.6}$$

From (2.3), the reflected impedance from the secondary side to primary side can be derived as

$$Z_{eq} = \frac{-j\omega M\, \dot{I}_s}{\dot{I}_p} = \frac{-j\omega M\, \dot{I}_s}{\dot{I}_s\, Z_s \big/ j\omega M} = \frac{\omega^2 M^2}{Z_s} \tag{2.7}$$

The total impedance seen from the primary side end is given by

$$Z_t = r_p + j\omega L_p + \frac{\omega^2 M^2}{Z_s} = \operatorname{Re}\left(Z_t\right) + j\operatorname{Im}\left(Z_t\right) \tag{2.8}$$

where

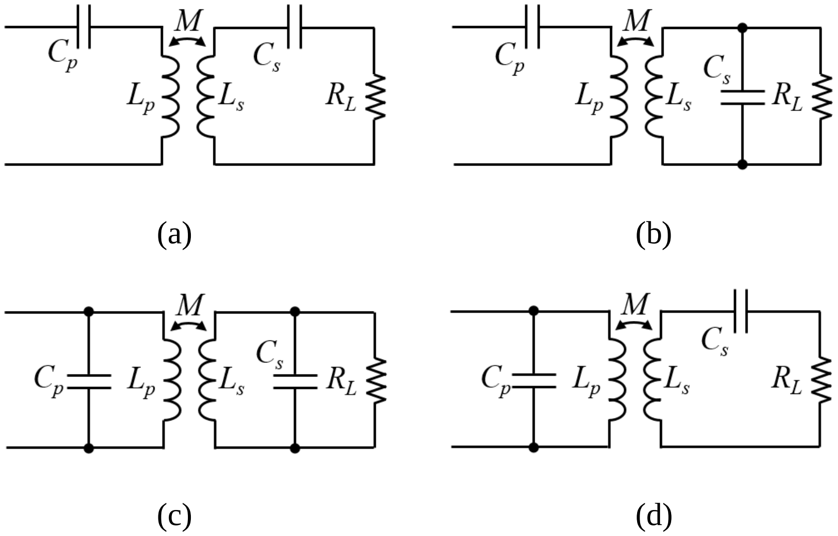
$\operatorname{Re}\left(Z_t\right) = r_p + \dfrac{\left(r_s + R_L\right)\omega^2 M^2}{\left(r_s + R_L\right)^2 + \left(\omega L_s\right)^2}$, and $\operatorname{Im}\left(Z_t\right) = j\left[\omega L_p - \dfrac{\omega^3 L_s M^2}{\left(r_s + R_L\right)^2 + \left(\omega L_s\right)^2}\right]$ are the real and imaginary parts of the total impedance Z_t seen from the primary side end.

From (2.4) and (2.8), the system efficiency is given by

$$\eta = \frac{\left|\dot{I}_s\right|^2 R_L}{\left|\dot{I}_P\right|^2 \operatorname{Re}\left(Z_t\right)} = \frac{R_L}{\left(r_s + R_L\right)\left[\dfrac{r_p\left(r_s + R_L\right)}{\omega^2 M^2} + 1\right] + r_p \dfrac{L_s^2}{M^2}} \tag{2.9}$$

It can be seen from (2.6) and (2.9) that for a given mutual inductance, frequency and load resistance, the efficiency and power transfer capability can be enhanced by compensating secondary reactance. Additionally, by including a compensation network in the primary side to compensate the reactance component of the total impedance Z_t, the VA rating of the source is minimized, thus the size of the source is reduced.

The simplest compensation topologies use only a single capacitor on each side. Depending on the placement of the capacitor on the primary and secondary side, there are four basic compensation topologies [61], namely series-series (SS), series-parallel (SP), parallel-parallel (PP), and parallel-series (PS), as shown in Figure 2.2. The design summary of basic compensation topologies is listed in Table 2.1. The studies conducted in [19, 56, 62-64] to compare the basic compensation topologies reveal that the SS topology is suitable for the EV charging applications since it is simple, load/mutual coupling-independent compensation, constant output current, efficient, cost-effective, and has low coil-fabrication copper mass.



(a) (b)

(c) (d)

Figure 2.2: Basic compensation topologies for IPT. (a) SS, (b) SP, (c) PP, and (d) PS.

Table 2.1: Design summary of compensation topologies [61].

Topologies	Secondary capacitance	Primary capacitance
SS	$C_s = \frac{1}{\omega_0^2 L_s}$	$C_p = \frac{1}{\omega_0^2 L_p}$
SP		$C_p = \frac{1}{\left(L_p - \frac{M^2}{L_s}\right)\omega_0^2}$
PS		$C_p = \frac{L_p}{\left(\frac{\omega_0^2 M^2}{R_L}\right)^2 + \omega_0^2 L_p^2}$
PP		$C_p = \frac{L_p - \frac{M^2}{L_s}}{\left(\frac{M^2 R_L}{L_s^2}\right)^2 + \left(L_p - \frac{M^2}{L_s}\right)^2 \omega_0^2}$

These basic compensation topologies are not so efficient for varying load conditions and coil position misalignments, which affects the maximum power transfer [65]. Several high-order compensation topologies including more than one reactive component on each side have been proposed to improve the system performance [56]. However, the increase of compensation elements is limited to avoid the significant extra power losses and cost. The most common high-order compensation networks are the inductor-capacitor-inductor (*LCL*) [66-68], inductor-capacitor-capacitor-inductor (*LCCL*) [69-71], and parallel-series capacitor-capacitor (*CC*) [72, 73]. The double-sided *LCL* and *LCCL* topologies are suitable to the dynamic chargers [74, 75], bidirectional systems [66, 67, 69, 76-78], and multiple pick-up systems [79, 80].

2.2 Inductive Coupling Structure

The high-frequency inductive coupler is the most crucial part of the IPT systems, which comprises the transmitting and receiving coils separated by air as a medium. The desired characteristics for the couplers are the high coupling coefficient, maximum power transfer capability, high misalignment tolerance, and low losses. The IPT couplers are usually planar structures. The Litz wire-based planar coils with ferrite spokes have minimized leakage inductance and improved misalignment tolerance [61, 81]. The planar couplers can be divided into non-polarized and polarized pads based on the orientation of magnetic path.

The most popular non-polarized coupler structures are circular, rectangular, and square-shaped pads, as shown in Figure 2.3 [82]. Ferrite cores are added to these couplers with the optimal arrangement so that maximum flux lines are guided from the primary to the secondary side, which increases coupling [83]. These structures are characterised by the single-sided direction of the magnetic field. It means their flux lines come in and out from one side [84]. Despite its lower coupling coefficient, the circular charging pads employing symmetrical Archimedean spiral coil pairs is one of the widely adopted pad shapes in static EV battery charging applications. This is because of its identical misalignment tolerance in all directions, facilitating vehicle parking [85]. The rectangle and square-shaped coil structures have better power transfer capability and higher flux areas with effective design [86].

The polarized charging pads use the parallel/horizontal component of the flux. The most popular coil structures are DD, DD-Q, and bipolar, as shown in Figure 2.4 [56, 82]. These coupling structures provide a greater misalignment tolerance in horizontal directions (X and Y). It is demonstrated that bipolar pad (BP) exhibits identical performance in terms

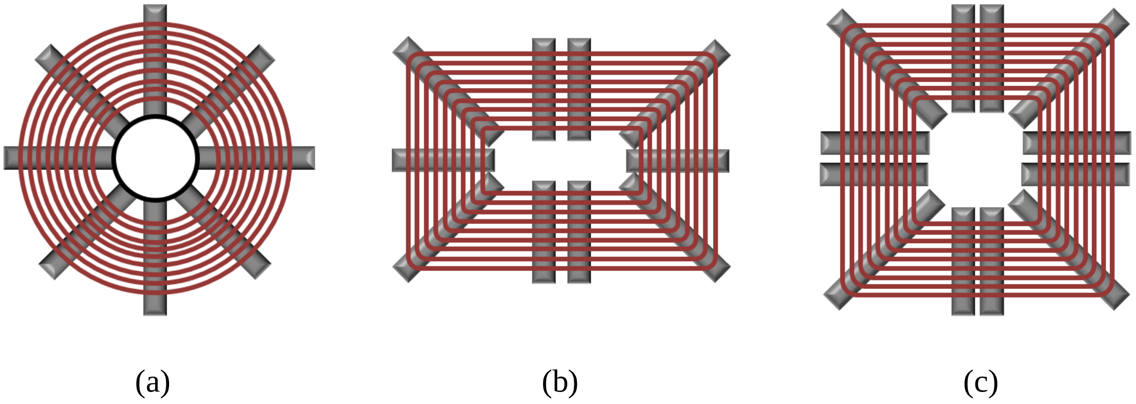

(a) (b) (c)

Figure 2.3: Non-polarized planar couplers. (a) Circular, (b) Rectangular, and (c) Square.

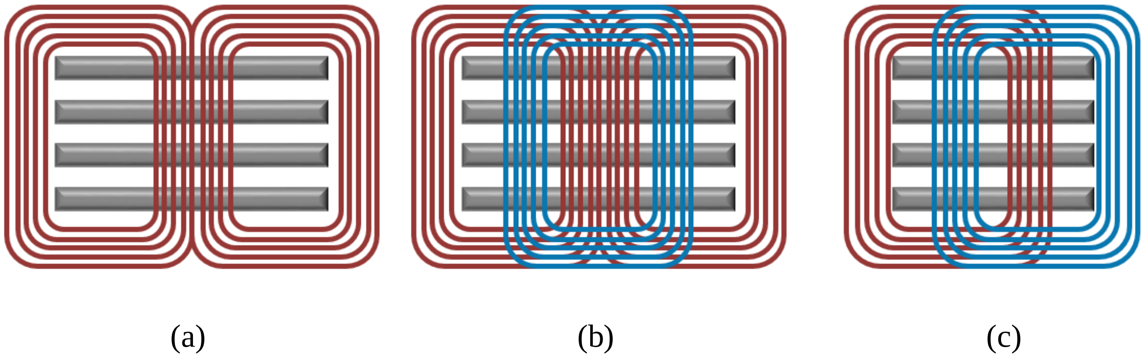

(a) (b) (c)

Figure 2.4: Polarized planar couplers. (a) DD, (b) DD-Q, and (c) Bipolar.

of coupling coefficient and misalignment tolerance to DDQ structure, but it has simple structure and requires 25-30% less copper mass [87].

2.3 Power Converter Topologies

Until recently, dual-stage conversion (AC/DC/AC) were popularly employed in the GA of IPT systems where power factor correction (PFC) is necessary during rectification from AC main voltage to DC voltage in order to assure the quality of AC input power. Then a high-frequency inverter connected to the PFC rectifier via a DC-link capacitor generates high-frequency inputs feeding the primary coil. The dual-stage converter topologies are intensively studied and widely used in industry [88-90]. The main advantage of the IPT systems using dual-stage conversion is that the PFC rectifier and the inverter are decoupled through the DC-link capacitor; therefore, they can be separately designed and controlled to optimize specific performance indices. However, the presence of multiple conversion stages and a bulky DC-link capacitor increases cost, size and weight of the system. Figure 2.5 (a) shows an EV IPT charging system using dual-stage conversion.

In recent years, the use of matrix converters (MCs) for feeding the IPT systems has drawn increasing attention [91-101]. MCs enable direct conversion of low-frequency AC inputs (50-60 Hz) to high-frequency outputs (up to 85 kHz) without any intermediate conversion stage; therefore, they enhance the system performance in terms of power density, reliability, and cost [93, 102]. The single-phase MC based IPT systems remove the DC-link energy storage elements in primary side to absorb double line frequency ripple, thus it appears on the battery side. Sinusoidal ripple current (SRC) charging technique reported in [101, 103-110] allows batteries to be charged by double line frequency (100 or 120 Hz) current with minor side effects on their performance. Therefore, the MC based IPT systems can use the sinusoidal charging technique advantageously and remove the intermediate DC-link capacitor. The single-stage EV IPT charging system using MCs is illustrated in Figure 2.5 (b).

In this section, an overview of front-end converter topologies for IPT applications is provided. They can be classified into two groups namely dual-stage and single-stage based on the power conversion stages. The classification of single-phase converter topologies for IPT systems is shown in Figure 2.6.

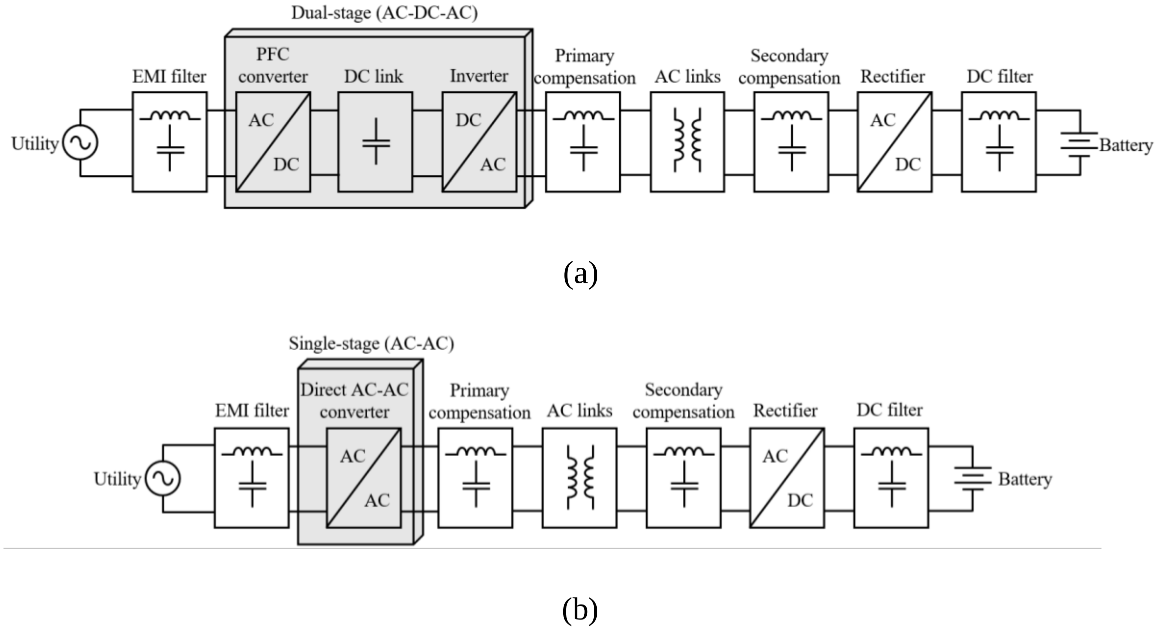


Figure 2.6: Configuration of EV IPT systems with (a) Dual-stage power conversion and (b) Single-stage power conversion.

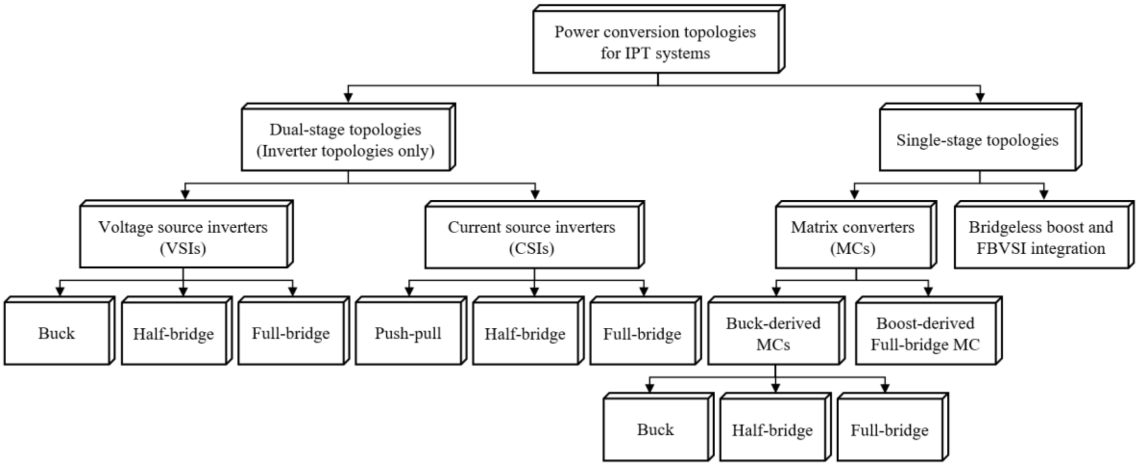
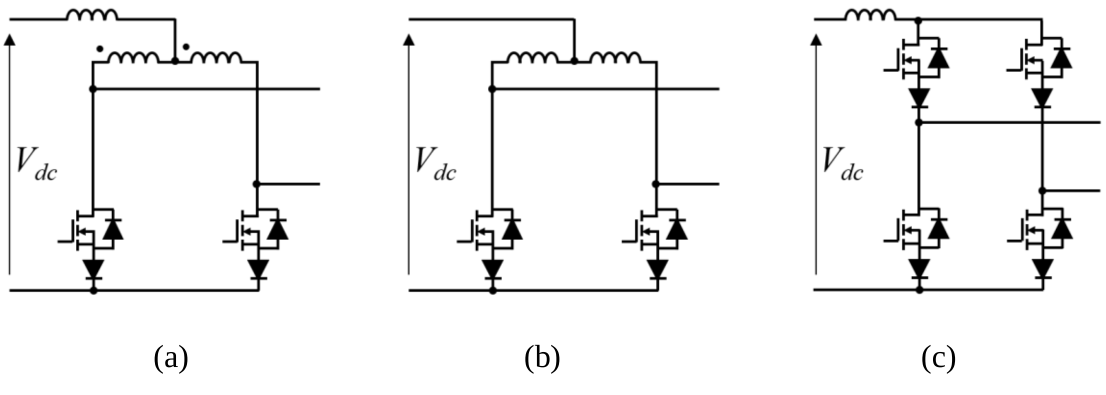


Figure 2.5: Classification of front-end converter topologies for IPT applications.

2.3.1 Dual-stage Conversion

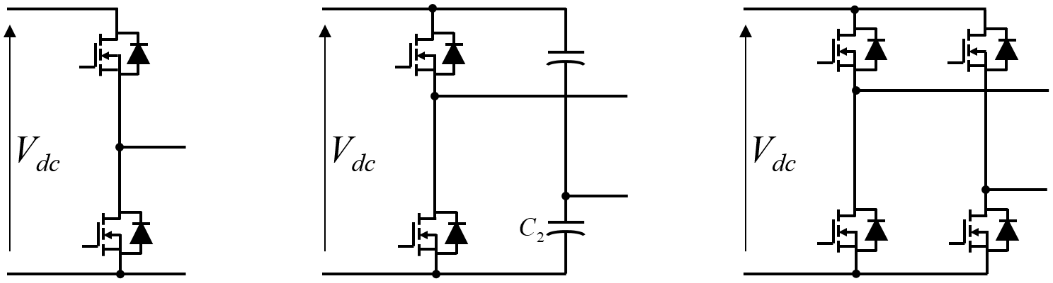
A front-end AC/DC converter is used to convert the supply AC voltage to an intermediate DC-link voltage and to shape the input current for both PFC and harmonic reduction. A comprehensive review for the PFC rectifiers is presented in [111] and [112]. For the inversion stage, a current-source inverter (CSI) or a voltage source-inverter (VSI) can be employed.

The CSI topologies commonly used in IPT systems are push-pull, half-bridge (HB) [72, 113-117] and full-bridge (FB) [73, 118]. Figure 2.7 shows the configuration of CSIs. The requirement of blocking diodes and bulky inductors that increases the size and cost of the whole IPT system is one of the major drawbacks of the CSIs. A single parallel compensating capacitor in the primary circuit is usually used with CSIs. The blocking diodes of the CSIs can be removed if the inverters are operated at zero voltage switching (ZVS) to prevent momentary short circuit. A variable frequency control scheme is normally used to regulate load variation and to achieve ZVS. However, the CSI based IPT systems using the variable frequency control suffer the start-up and bifurcation issues. Moreover,



(a) (b) (c)

Figure 2.7: Current-source inverter topologies. (a) Push-pull, (b) Half-bridge, and (c) Full-bridge.

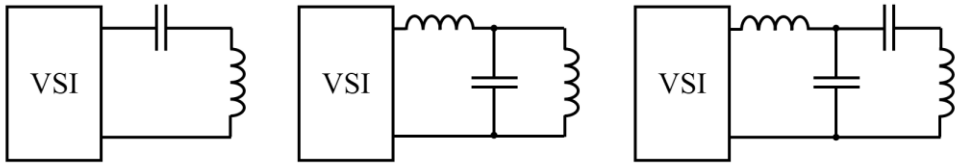


(a) (b) (c)

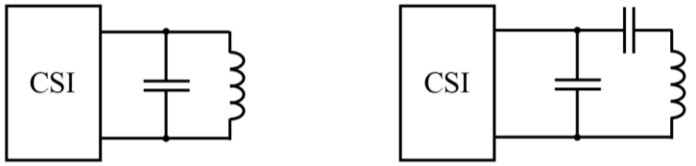
Figure 2.8: Voltage-source inverter topologies. (a) Buck, (b) Half-bridge, and (c) Full-bridge.

the inverter switches will experience high voltage stress in high-power applications if only single parallel capacitor compensation is used [113, 115, 117, 118]. In order to overcome this drawback, a parallel-series *CC* compensation circuit is introduced in [72, 73]. The fixed-frequency controlled FB CSI combining with the parallel-series *CC* compensation circuit can mitigate the problems of start-up, bifurcation and switching stress.

For VSI topologies, buck, HB and FB topologies shown in Figure 2.8 can be used in the IPT systems, and they are compatible with single capacitor series, *LCL*, and *LCCL* compensation networks [36, 53, 66, 69, 81, 119-130]. The SS compensation is simple and cost-effective. However, under light load conditions or in the absence of the receiver, the system experiences severe instability [56, 63]. The *LCL* or *LCCL* tanks can overcome these issues, they also have a higher tolerance to coil misalignments, and improve power transfer capability [56]. Therefore, the *LCL* or *LCCL* topologies are suitable to the dynamic chargers [74, 75], bidirectional systems [66, 67, 69, 76-78], and multiple pick-up systems [79, 80]. However, a significant amount of lower-order harmonics in the output current of the VSIs connected with *LCL* and *LCCL* compensation circuits deviates zero-phase-angle



(a) Series *C* (b) *LCL* (c) *LCCL*



(d) Parallel *C* (d) Parallel-series *CC*

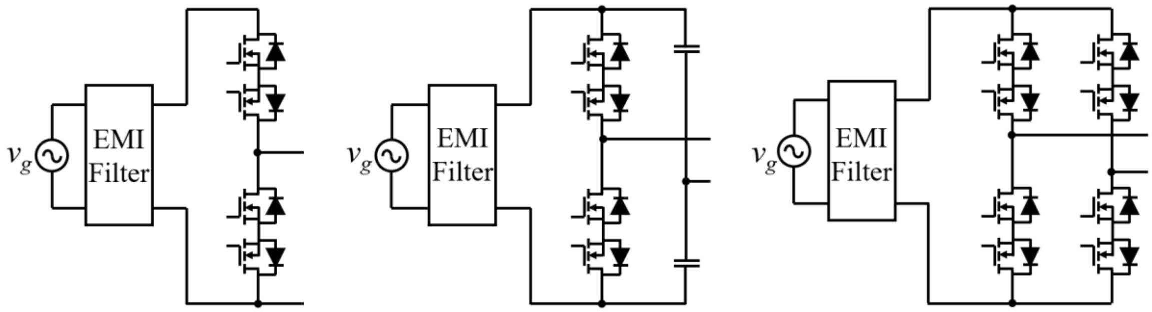
Figure 2.9: Compatibility between inverter types and primary compensation circuits in IPT systems.

operation of the inverters [131]. Moreover, the inductors in *LCL* and *LCCL* compensation circuits must be designed precisely as the effective power transfer capability is highly sensitive to the inductance value [66, 69]. Figure 2.9 shows the compatibility of the inverter types and primary compensation circuits of the IPT systems.

2.3.2 Single-stage Conversion

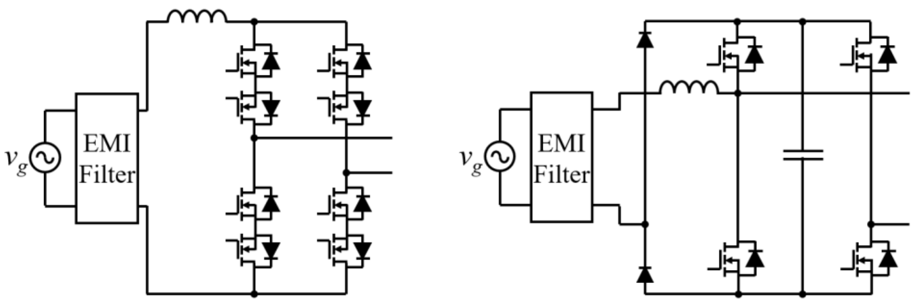
MCs are considered as a prominent candidate for powering the WPT systems with only single-stage power conversion. Several MCs including buck [98, 99], HB [91, 101], and FB [96, 132] have been introduced to IPT applications in literature. All MCs reported in [91, 96, 98, 99, 101, 132] have a buck-derived configuration, as shown in Figure 2.10, so they are compatible with series, *LCL*, and *LCCL* compensation networks. Due to the buck-derived configuration, the line-current regulation of these topologies is compromised. In the EV charging applications, if a highly nonlinear diode-bridge rectifier is used at the battery side, there will be severe line current distortion and power factor deterioration, as explained in [133]. In [96], a secondary active full-bridge rectifier whose phase shift angle follows the line-voltage waveform is used to shape the line current. In this topology, the primary and secondary converters must be controlled synchronously in every switching cycle, which increases implementation complexity.

In order to overcome the above issue, a boost-derived FBMC compatible with a primary parallel-series *CC* compensation network is proposed in [100]. The proposed converter topology is able to shape the line current and regulate power flow through two control loops which are similar to those of a conventional boost converter. In [102], a single-stage topology integrating bridgeless boost PFC converter and FB VSI is proposed for IPT applications. The converter is operated in discontinuous conduction mode (DCM), thereby the line current control loop is eliminated. However, the converter incurs more current stress, losses, and EMI problems in DCM, which is not suitable for high-power applications. Figure 2.11 shows the configuration of the boost-derived FBMC and the FB VSI-integrated bridgeless boost PFC converter in the IPT systems.



(a) (b) (c)

Figure 2.10: Buck-derived MCs. (a) Buck, (b) Half-bridge, and (c) Full-bridge.



(a) (b)

Figure 2.11: (a) Boost-derived MC, and (b) FB VSI-integrated bridgeless boost converter.

2.4 Power Control Schemes

Figure 2.12 shows the classification of power control schemes for IPT systems. Power control in IPT systems can be implemented on the primary, secondary side, or both sides. The secondary side control is suitable for the IPT applications where multiple secondary coils are coupled to a single primary coil. In these applications, the frequency and the magnitude of primary current are fixed, and the power flow is controlled on the secondary side by an active rectifier or a back-end DC/DC converter illustrated in Figure 2.12 for each secondary coil [79, 101, 120, 121, 134-136]. These topologies are normally employed in long-power track systems where a constant track current is required to power independent secondary coils. However, in charging applications where only one secondary coil is coupled to a primary coil and keeping the secondary-side configuration as simple as possible is a priority, the primary side control is selected. The primary side control can be divided into three groups: fixed frequency, variable frequency and discrete energy injection. In fixed frequency control, the switching frequency of the inverter is kept at a constant value, which is slightly different from the primary resonant frequency to offer soft-switching operation. In order to control the power flow, the phase (phase shift control)

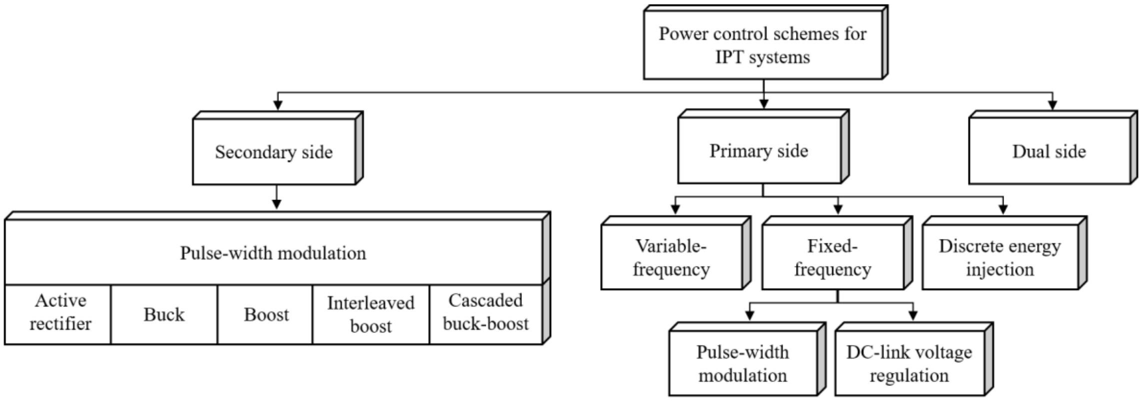


Figure 2.12: Classification of power control schemes for IPT applications.

or the duty cycle of the inverter switches is varied [137, 138]. This allows the inverters to produce output voltage/current with variable pulse width. The other way to regulate the power flow with the fixed switching frequency is controlling the input DC voltage of the inverter using a front-end DC/DC converter [113]. For the variable switching frequency control scheme, the duty cycle of the gating signals is maintained constant at 50% and the switching frequency is varied to regulate the output power [114]. However, if the operating frequency is largely different from the resonant frequency, the resonant tank will incur a large circulating current, causing an efficiency drop in the overall system due to large losses in switches and in the coils. Moreover, the bifurcation phenomenon must be carefully considered in this control technique [139].

In [98], a discrete energy injection control is used for the matrix buck converter in order to control the magnitude of the primary current. The control technique reduces switching frequency and enables soft switching. However, the zero-crossing detection of primary high-frequency current which is required to ensure the converter to be operated in zero current switching (ZCS) conditions is an implementation challenge. Moreover, current sag occurs during the zero-crossing of its single-phase input voltage, which degrades the average power transferred. The dual-side control is suitable for bidirectional IPT systems where power flow can be regulated in both directions by controlling the duty cycle of the primary and secondary converters and the phase-shift between them [66, 119, 140]. Table 2.2 shows the compatibility of power conversion topologies and control schemes.

2.5 Summary

An extensive overview of the compensation networks, power conversion topologies, coupling structure, and control schemes of the IPT systems was presented. Table 2.2 shows the comparison summary of the power converter topologies in terms of component count and control schemes. It can be seen that the CSIs have more components but less control scheme options compared to the VSIs. The parallel-series *CC* compensation network is a good choice for the CSIs in the high-power applications, since it mitigates the current and voltage stresses on the inverter switches. Although the single-stage converter topologies have the advantage of the removal of the front-end rectifier and the DC-link capacitor, they still require many active switches, and complex control schemes, as shown in Table 2.2.

Although the power converter topologies for the EV charging applications was generally reviewed with their own advantages and disadvantages in this chapter, they need to be more intensively evaluated based on several other performance indices such as input power factor, input current distortion, power losses, switching stress, and cost to obtain a sound understanding of their properties and constraints. A more intensive performance evaluation on the most common converter topologies including the conventional dual-stage, single-stage buck-derived FBMC, and boost-derived FBMC topologies will be given in the next chapter along with their design considerations.

Table 2.2: Compatibility of power conversion topologies and control schemes of the IPT systems

Power conversion topologies		**Figure**	**Component requirement**		**Control schemes**
			Switches	Passive components	
Dual-stage (excluding front-end PFC stage)	push-pull	2.4 (a)	2 reverse blocking	1 inductor, 1phase-splitting transformer	• Variable switching frequency • DC-link voltage control • Secondary-side control • Dual-side control
	HB CSI	2.4 (b)	2 reverse blocking	2 inductors	
	FB CSI	2.4 (c)	4 reverse blocking	1 inductor	• Variable switching frequency • DC-link voltage control • Pulse width modulation (duty cycle control) • Secondary-side control • Dual-side control
	Buck VSI	2.5 (a)	2 reverse conducting	None	• Discrete energy injection • Variable switching frequency • DC-link voltage control • Pulse width modulation (duty cycle control) • Secondary-side control • Dual-side control
	HB VSI	2.5 (b)	2 reverse conducting	2 capacitors	
	FB VSI	2.5 (c)	4 reverse conducting	None	• Discrete energy injection • Variable switching frequency • DC-link voltage control • Pulse width modulation (phase-shift control) • Secondary-side control • Dual-side control
Single-stage	Buck MC	2.7 (a)	2 bidirectional	None	• Discrete energy injection • Pulse width modulation (duty cycle control) • Secondary-side control • Dual-side control
	Buck-derived half-bridge MC	2.7 (b)	2 bidirectional	2 capacitors	
	Buck-derived FBMC	2.7 (c)	4 bidirectional	None	• Discrete energy injection • Pulse width modulation (phase-shift control) • Secondary-side control • Dual-side control
	Boost-derived FBMC	2.8 (a)	4 bidirectional	1 inductor	• Pulse width modulation • Secondary-side control • Dual-side control
	Bridgeless boost	2.8 (b)	2 diodes, 4 reverse conducting	1 inductor, 1 capacitor	• Pulse width modulation • Secondary-side control • Dual-side control

Chapter 3. Design Considerations and Comparative Assessment of Typical Single-phase Power Converter Topologies of Inductive Wireless Electric Vehicle Charging Systems

In this chapter, the design considerations and comprehensive performance comparison of the conventional dual-stage (PFC and FB VSI) and single-stage topologies including the buck-derived FBMC and boost-derived FBMC in the EV IPT charging application are presented. The IPT charging systems are designed based on the requirements of the WPT 1 system in the SAE J2954 wireless charging standard. The performance comparison are realized by using the simulation PSIM software that is developed by Powersim to specifically simulate power electronic and motor drive systems. The comparison takes account into input power factor, input current distortion, power losses, switching stress, and cost.

3.1 Design Considerations

The conventional dual-stage IPT charging system is illustrated in Figure 3.1. At the front end, a conventional boost rectifier is used to shape the grid current and maintain a constant DC voltage V_{dc} across DC-link capacitor C_{dc}. As a bulky and costly inductor is required for the CSIs, an FB VSI is the most common choice at the primary side to generate a high-frequency voltage (v_p) feeding the primary coil. A SS compensation topology is used because it is simple, cost-effective, and primary compensation is independent of the coupling coefficient and load [56, 62]. In order to maximize the power transfer capabilities and minimize the VA rating of the primary inverter, the resonant circuits at both sides of the coupling are usually tuned to the same resonant frequency equal to switching frequency (ω_s) of the inverter.

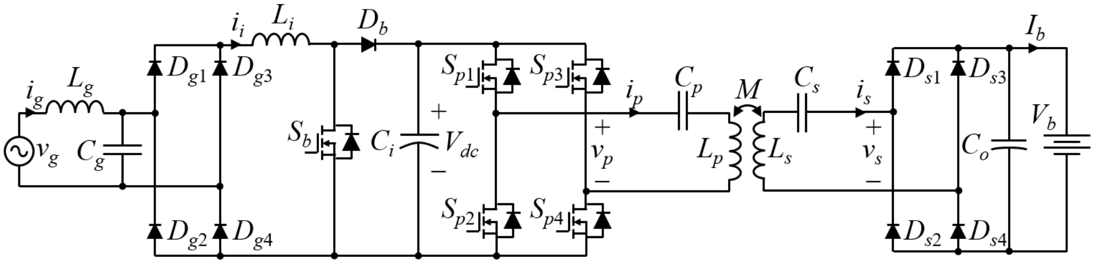


Figure 3.1: IPT charging system fed by dual-stage power converter (PFC and FB VSI).

$$\omega_s = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{3.1}$$

where L_p and L_s are primary and secondary coil self-inductances, and C_p and C_s are primary and secondary tuning capacitors.

Power regulation is conducted using the phase-shift control at the primary inverter side. According to [126, 130], considering an ideal IPT system operating at the resonant frequency, power transferred from the primary to the secondary side can be given by

$$P_o = \frac{8V_{dc}V_b}{\pi^2 \omega_s M} \sin \pi D_p \tag{3.2}$$

where D_p is the duty cycle of the primary voltage (v_p), and M is mutual inductance and can be calculated as

$$M = k\sqrt{L_p L_s} \tag{3.3}$$

In EV wireless charging applications, the coupling coefficient k may be in the range of 0.1- 0.3. In dual-stage topology, the major drawback is low power density due to multiple conversion stages and a bulky DC-link capacitor. The reduction of the number of power conversion stages can be obtained using MCs. Figure 3.2 shows the IPT charging

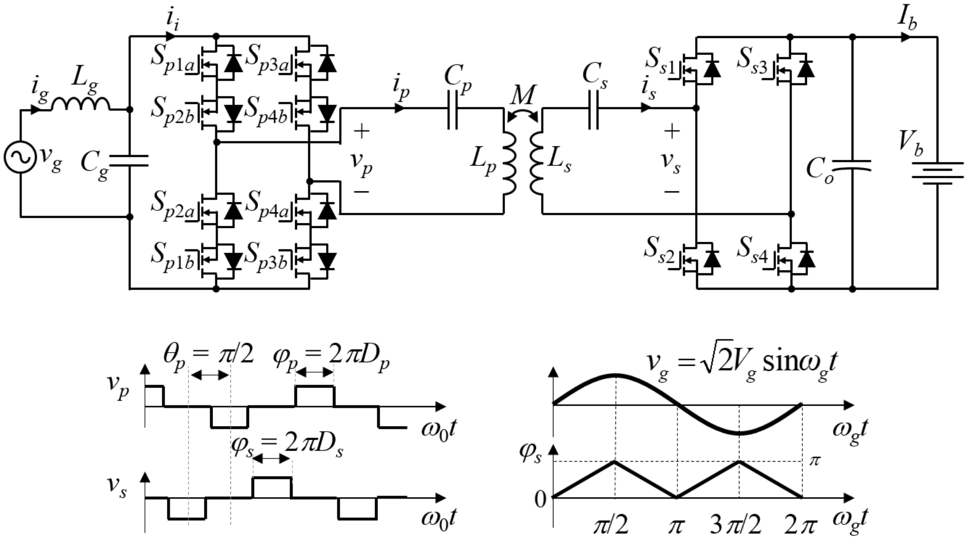


Figure 3.2: IPT charging system fed by buck-derived FBMC.

system using a buck-derived FBMC [132]. The FBMC constituted by four bidirectional switches can directly convert low frequency (50-60 Hz) grid voltage to resonant frequency (85 kHz) voltage feeding the inductive coil. During the positive half cycle of the grid voltage v_g, switches S_{pnb} (n = 1, 2, 3, 4) are turned on and switches S_{pna} are controlled by the phase-shift pulse-width modulation (PWM) strategy. Otherwise, during the negative half-cycle, the switches S_{pna} are kept on and switches S_{pnb} are controlled by the phase-shift PWM strategy.

An active rectifier is employed in the battery side for shaping the input current. The primary and secondary converters are synchronized in every switching cycle so that primary voltage v_p is 90^0 lagging with secondary voltage v_s, and the duty cycle of the secondary voltage is controlled following grid voltage waveform to correct input current as shown in Figure 3.2. In [132], The power transferred is controlled by adjusting the duty cycle of the primary voltage.

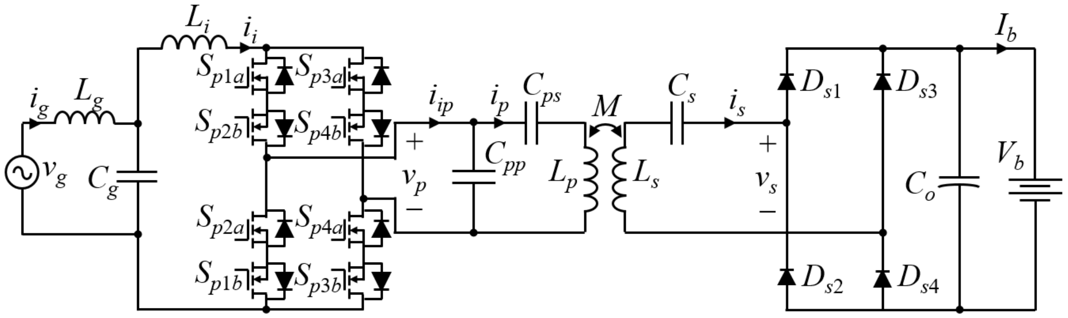


Figure 3.3: IPT charging system fed by boost-derived FBMC.

$$P_o = \frac{4\sqrt{2}V_g V_b}{\pi^2 \omega_s M} \sin \pi D_p \tag{3.4}$$

where V_g is the RMS value of the grid voltage.

Although the buck-derived FBMC based IPT charging system removes the intermediate conversion stage, high-frequency communication is required to synchronize the PWM patterns of the primary and secondary converters in every switching cycle, which increases the control complexity. The boost-derived MC can solve the above issue. It is capable of correcting the grid current and regulating power flow through two control loops which are similar to those of a conventional boost converter. Figure 3.3 shows an IPT topology fed by a boost- derived FBMC [100]. On the primary side, parallel-series *CC* compensation is used to reduce voltage stress on the MC switches. The tuning capacitor C_{ps} is selected so as to limit the maximum peak of v_p across the converter switches. It is desirable to restrict v_p to 0.5~0.7 of the rating voltage of the switches [113]. The switching scheme and controller design for boost-derived FBMC are described in [100]. Table 3.1 shows the component design of the converter components.

Table 3.1: Power conversion topologies and control schemes of the IPT systems

Topologies	**Components**	**Parameters**	
Dual-stage [130]	Boost inductor L_i	Inductance $L_i = \frac{1}{\%\Delta I_i} \frac{V_g^2}{P_{o(\max)} f_s} \left(1 - \frac{\sqrt{2} V_g}{V_{dc}}\right)$	Peak current $\hat{I}_{Li} = \sqrt{2} \frac{P_o}{V_g} + \frac{\Delta I_i}{2}$
	DC-link capacitor C_{dc}	Capacitance $C_{dc} = \frac{1}{\%\Delta V_{dc}} \frac{P_o}{\omega_g V_{dc}^2}$	Peak voltage $\hat{V}_{dc} = V_{dc} + \frac{\Delta V_{dc}}{2}$
	Boost switch S_b and diode D_b	Peak current $\hat{I}_{Sb} = \hat{I}_{Db} = \sqrt{2} P_o / V_g + \Delta I_i / 2$	Break down voltage $\hat{V}_{Sb} = \hat{V}_{Db} > V_{dc} + \Delta V_{dc} / 2$
	Compensation capacitors C_p and C_s	Capacitance $C_p = \frac{1}{\omega_0^2 L_p};\ C_s = \frac{1}{\omega_0^2 L_s}$	Peak voltage $\hat{V}_{Cp} = \frac{4V_b}{\pi \omega_0^2 C_p M};\ \hat{V}_{Cs} = \frac{4V_{dc}}{\pi \omega_0^2 C_s M}$
	Primary inverter switches S_{pn} (n = 1, 2, 3, 4)	Peak current $\hat{I}_{Spn} = 4V_b / \pi \omega_0 M$	Break down voltage $\hat{V}_{Spn} > V_{dc} + \Delta V_{dc} / 2$
	Secondary rectifier diodes D_{sn} (n = 1, 2, 3, 4)	Peak current $\hat{I}_{Dsn} = 4V_{dc} / \pi \omega_0 M$	Break down voltage $\hat{V}_{Dsn} > V_b$
Buck-derived FB MC [132, 141]	Compensation capacitors C_p and C_s	Capacitance $C_p = \frac{1}{\omega_0^2 L_p};\ C_s = \frac{1}{\omega_0^2 L_s}$	Peak voltage $\hat{V}_{Cp} = \frac{4V_b}{\pi \omega_0^2 C_p M};$ $\hat{V}_{Cs} = \frac{4\sqrt{2} V_g}{\pi \omega_0^2 C_s M}$
	Primary inverter switches S_{pnx} (n = 1, 2, 3, 4 and x = a, b)	Peak current $\hat{I}_{Spnx} = 4V_b / \pi \omega_0 M$	Break down voltage $\hat{V}_{Spnx} > \sqrt{2} V_g$
	Secondary rectifier switches S_{sn} (n = 1, 2, 3, 4)	Peak current $\hat{I}_{Ssn} = 4\sqrt{2} V_g / \pi \omega_0 M$	Break down voltage $\hat{V}_{Ssn} > V_b$
Boost-derived FB MC [100]	Boost inductor L_i	Inductance $L_i = \sqrt{2} V_g / 2\Delta I_i f_s$	Peak current $\hat{I}_{Li} = \sqrt{2} P_o / V_g + \Delta I_i / 2$
	Compensation capacitors C_{pp}, C_{ps}, and C_s **Note:** C_{ps} is designed to limit the peak of primary voltage v_p, which is the voltage stress on MC switches.	Capacitance $C_s = \frac{1}{\omega_0^2 L_s};$ $C_{pp} = \frac{L_p - \frac{1}{\omega_0^2 C_{ps}}}{\frac{\omega_0^4 M^4}{R_{oeq}^2} + \omega_0^2 \left(L_p - \frac{1}{\omega_0^2 C_{ps}}\right)^2}$	Peak voltage $\hat{V}_{Cs} = \frac{\pi P_o}{\omega_0 C_s V_b};\ \hat{V}_{Cps} = \frac{4V_b}{\pi \omega_0^2 C_{ps} M};$ $\hat{V}_{Cpp} = \hat{V}_p = \sqrt{\left(\frac{4V_b}{\pi M}\right)^2 \left(L_p - \frac{1}{\omega_0^2 C_{ps}}\right)^2 + \left(\frac{\pi \omega_0 M P_o}{V_b}\right)^2}$
	Primary inverter switches S_{pnx} (n = 1, 2, 3, 4 and x = a, b)	Peak current $\hat{I}_{Spnx} > \sqrt{2} P_o / V_g + \Delta I_i / 2$	Break down voltage $\hat{V}_{Spnx} > \hat{V}_p$
	Secondary rectifier diodes D_{sn} (n = 1, 2, 3, 4)	Peak current $\hat{I}_{Dsn} > \pi P_o / V_b$	Break down voltage $\hat{V}_{Dsn} > V_b$

3.2 Specifications of the IPT charging systems

The IPT charging systems are designed in compliance with the level 1 (WPT1) of static wireless charging standard for light-duty vehicles provided in SAEJ2954 technical information report [26] with power rating P_o = 3.3 kW, operating frequency f_s = 85 kHz, grid voltage V_g = 208 V, and battery voltage V_b = 300–400 V. The parameters of the charging system with each type of power conversion configuration are shown in Table 3.2. All the parameters are calculated based on Table 3.1. The selection of components is based on their maximum current and voltage stresses. Note that, available discrete Rohm SiC MOSFETs and Schottky diodes are considered for all power conversion topologies.

Table 3.2: Specifications of IPT charging systems

Topologies	**Parameter**	**Symbol**	**Value**	**Unit**
Dual-stage	Primary, secondary, mutual inductance	L_p, L_s, M	356, 328, 65	μH
	Compensation capacitors	C_p, C_s	10, 11	nF
	Boost inductor	L_i	0.215	mH
	DC-link capacitor	C_{dc}	1540	μF
	DC-link voltage	V_{dc}	400	V
	Grid filter inductor	L_g	0.215	mH
	Grid filter capacitor	C_g	0.78	μF
	Output filter capacitor	C_o	500	μF
Buck-derived FBMC	Primary, secondary, mutual inductance	L_p, L_s, M	111, 111, 24	μH
	Compensation capacitors	C_p, C_s	32, 32	nF
	Grid filter inductor	L_g	0.215	mH
	Grid filter capacitor	C_g	0.78	μF
	Output filter capacitor	C_o	500	μF
Boost-derived FBMC	Primary, secondary, mutual inductance	L_p, L_s, M	111, 111, 24	μH
	Compensation capacitors	C_{ps}, C_{pp}, C_s	43, 115, 32	nF
	Boost inductor	L_i	0.215	mH
	Grid filter inductor	L_g	0.036	mH
	Grid filter capacitor	C_g	0.136	μF
	Output filter capacitor	C_o	500	μF

Table 3.3: Main components of power conversion stages

Topolo-gies	**Components**	**Symbol**	**Part number**	**Quantity**	**Rating**	**Unit cost ($) ****
Dual-stage	Front-end rectifier diodes	D_{gn}^*	SCS240AE2C-ND	4	650 V/40 A	12.75
	Boost diode	D_b	SCS240AE2C-ND	1	650 V/40 A	12.75
	Boost switch	S_b	SCT3060ALGC11-ND	1	650 V/39 A	8.74
	Primary inverter switches	S_{pn}^*	SCT3120ALHRC11-ND	4	650 V/21A	7.02
	Secondary rectifier diodes	D_{sn}^*	SCS230AE2HRC-ND	4	650 V/30 A	8.97
	Boost inductor	L_i	HF5712-561M-25AH	2 parallel	25 A/430 μH	29.25
	DC-link capacitor	C_{dc}	LGN2X221MELC50	7 parallel	600 V/220 μF	7.78
	Grid inductor	L_g	HF5712-561M-25AH	2 parallel	25 A/430 μH	29.25
	Grid capacitor	C_g	B32656T7394K000	2 parallel	500 V/0.39 μF	4.23
	Gate driver IC	N/A	UCC5390SCD	5	N/A	2.16
	Gate driver supply	N/A	R12P21503D	4	+15 V/-3 V/2 W	7.11
Buck-derived FBMC	Primary MC switches	S_{pna}, S_{pnb}^*	SCT3030ALGC11-ND	8	650 V/70 A	19.46
	Secondary rectifier diodes	S_{sn}^*	SCT3060ALGC11-ND	4	650 V/39 A	8.74
	Grid inductor	L_g	HF5712-561M-25AH	2 parallel	25 A/430 μH	29.25
	Grid capacitor	C_g	B32656T7394K000	2 parallel	500 V/0.39 μF	4.23
	Gate driver IC	N/A	UCC5390SCD	12	N/A	2.16
	Gate driver supply	N/A	R12P21503D	7	+15 V/-3 V/2 W	7.11
Boost-derived FBMC	Primary MC switches	S_{pna}, S_{pnb}^*	SCT2080KEC-ND	8	1200 V/40 A	17.77
	Secondary rectifier diodes	D_{sn}^*	SCS240AE2C-ND	4	650 V/40 A	12.75
	Boost inductor	L_i	HF5712-561M-25AH	2 parallel	25 A/430 μH	29.25
	Grid inductor	L_g	HF467-980M-25AV	2 parallel	25 A/72 μH	21.15
	Grid capacitor	C_g	B32654A1683K000	2 parallel	500 V/68 nF	1.01
	Gate driver IC	N/A	UCC5390SCD	8	N/A	2.16
	Gate driver supply	N/A	R12P21503D	4	+15 V/-3 V/2 W	7.11

*n = 1, 2, 3, 4.

** Pricing source: Digikey and Mouser, June 20, 2020.

Moreover, *LC* filters are used as interfaces between the grid and the charging systems to limit current harmonic injection due to the switching power converters. The *LC* filters are designed based on the spectrum analysis of the input current waveforms (i_i). The details of selected components for different power conversion stages are listed in Table 3.3.

Figure 3.4, 3.5 and 3.6 show the typical waveforms of IPT charging systems with different power supply topologies. It can be seen that the absence of DC-link energy storage in MC based topologies causes a double line frequency fluctuation in transferred power. This results in a fluctuating charging current as shown in Figure 3.5 and 3.6. As reported in [101, 103-108], batteries can be charged by double line frequency (100 or 120 Hz) current with negligible side effects on their performance, and the MC based IPT systems advantageously adopt the low-frequency sinusoidal current ripple charging technique and remove the intermediate DC-link capacitors to improve their power density. However, the power fluctuation in the MC based topologies causes higher current stresses on the switching devices, which is demonstrated in Section 3.3.2.

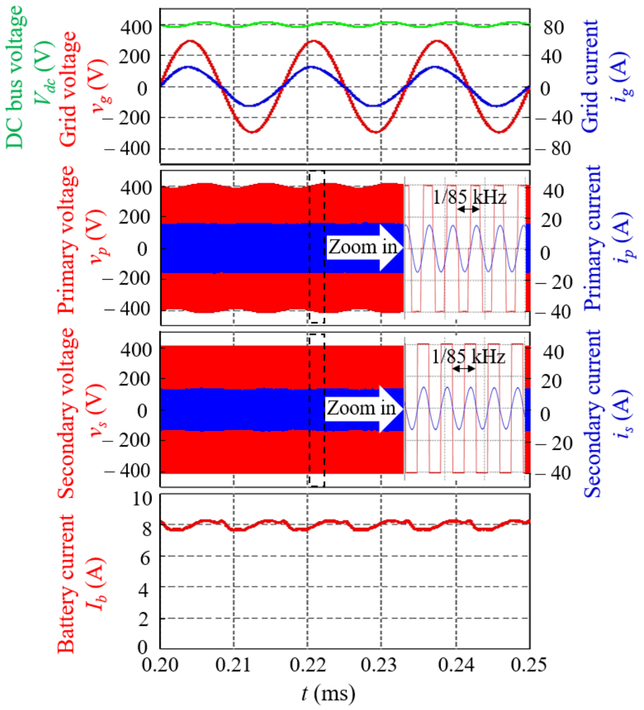


Figure 3.4: Simulation waveforms of IPT charging systems fed by dual-stage converter with the horizontal magnification of the high-frequency signals (v_p, i_p, v_s, and i_s).

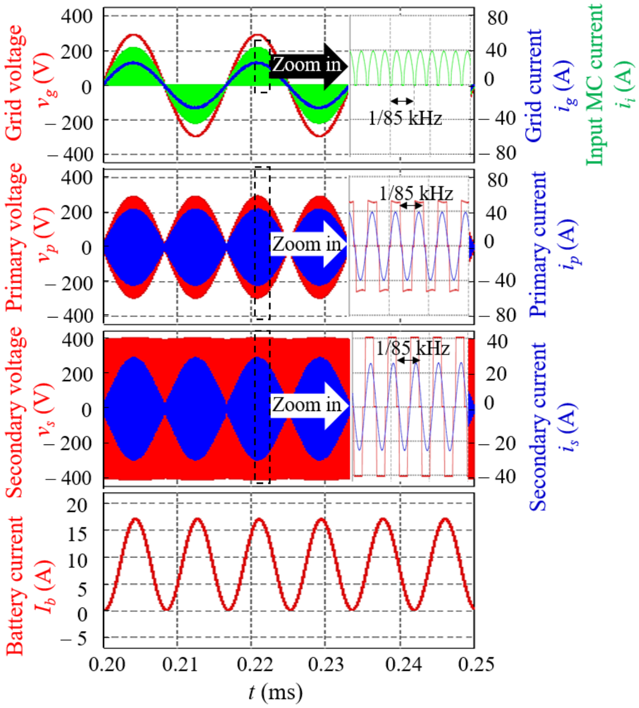


Figure 3.6: Simulation waveforms of IPT charging systems fed by buck-derived FBMC with the horizontal magnification of the high-frequency signals (i_i, v_p, i_p, v_s, and i_s).

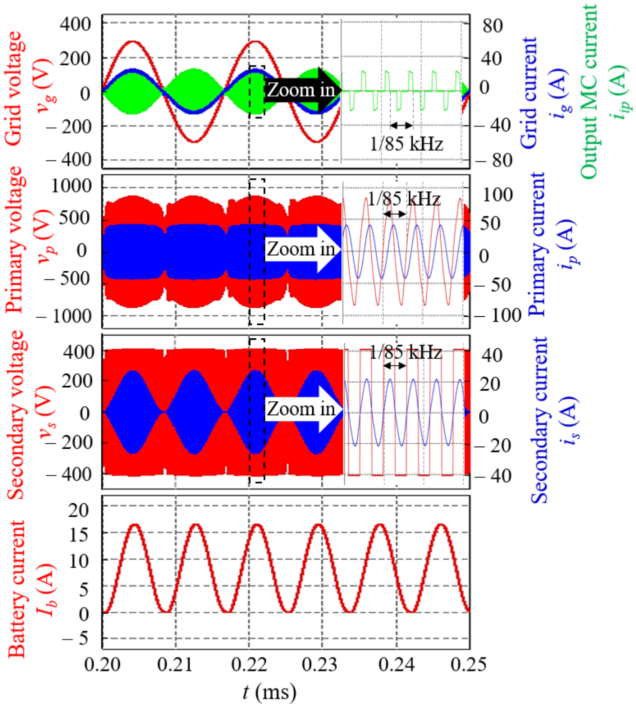


Figure 3.5: Simulation waveforms of IPT charging systems fed by boost-derived FBMC with the horizontal magnification of the high-frequency signals (i_{ip}, v_p, i_p, v_s, and i_s).

3.3 Performance Comparison

3.3.1 Input Power Factor and Input Current Distortion

An EV charger must ensure a good grid power quality with high power factor and low current distortion. All three topologies provide sinusoidal grid currents with the power factor of 0.99. Figure 3.7 shows total harmonic distortion (THD) of the grid current under different load conditions (20%, 50% and 100% of load). It can be seen that the three topologies can be preferred in order of boost-derived FBMC, dual-stage converter, and buck-derived FBMC regarding grid current distortion. Despite having the identical input *LC* filter, the buck-derived FBMC injects higher current harmonics to the grid than dual-stage topology since its input current is discontinuous. The boost-derived FBMC has the continuous input current with ripple frequency at a twice switching frequency, thereby gaining the significant harmonic reduction of grid current with a smaller input filter.

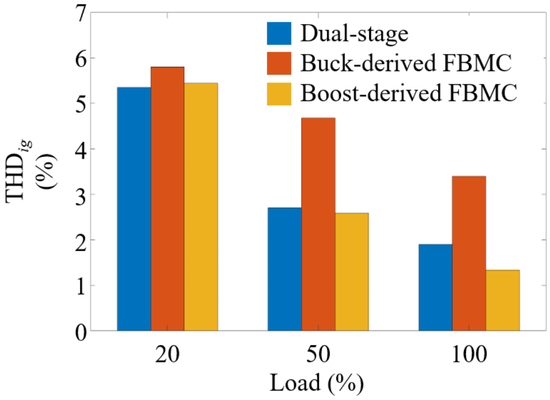
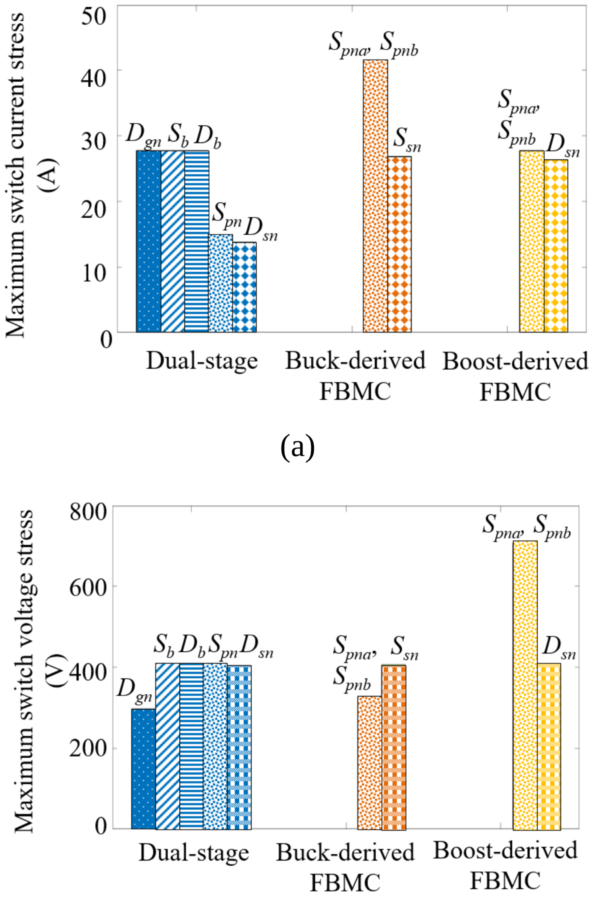


Figure 3.7: Total harmonic distortion (THD) of grid current.

3.3.2 Switching Stress

Figure 3.8 (a) and (b) show maximum current and voltage stress on the converter switches. Although the parallel-series *CC* compensation is used, the switches of boost-derived FBMC still suffer from high voltage stress. The buck-derived FBMC is characterized by low switch voltage stress (grid voltage peak) and high switch current stress. The dual-stage topology exhibits the lowest switch current stress in the primary inverter and secondary rectifier. As the result of the large charging current ripple as shown in Figures 3.5 and 3.6, the current stresses on the secondary rectifiers of the MC-based systems is higher compared to the dual-stage system. The high current or voltage stresses on the switching devices of the MC topologies might lead to high thermal stresses and challenging thermal management. However, this issue can be mitigated by using the SiC switching devices. These devices have a low voltage drop, thereby generating lower heat during operation.



(a)

(b)

Figure 3.8: Switching stresses. (a) Current stress, and (b) Voltage stress.

3.3.3 Efficiency and Loss Distribution

The losses on the conversion stages of each system are simulated and analyzed using the thermal modules in PSIM simulation. The efficiency of the power conversion stages of each system versus various output power is illustrated in Figure 3.9. It is clear that the efficiency of the buck-derived FBMC system is the highest (almost 98%) at full load conditions, but it decreases gradually to 93% at the light load conditions. In contrast, the efficiency of the boost-derived FBMC system steadily increases from 92.5% to 96% when the load decreases from 100% to 20%. The dual-stage system remains fairly high efficiency (94%~96.5%) in a wide load range. The detailed loss distribution of the three systems is shown in Figure 3.10. It can be observed that the conduction losses of primary converters dominate the total losses of power conversion stages. In the dual-stage system, the conduction losses of the front-end rectifier and the primary inverter are the two major parts. For the single-stage systems, the conduction losses of MCs contribute to the largest proportions (> 60%).

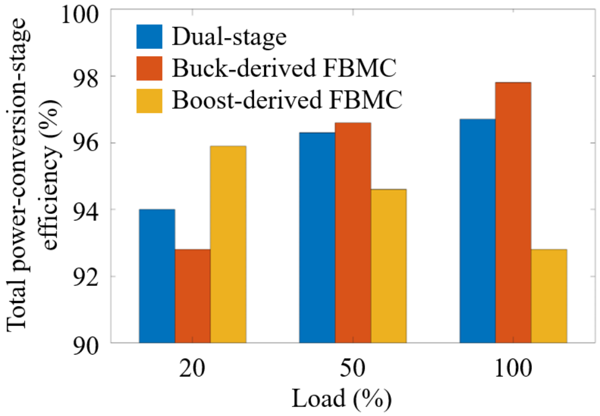


Figure 3.9: Power-conversion-stage efficiency.

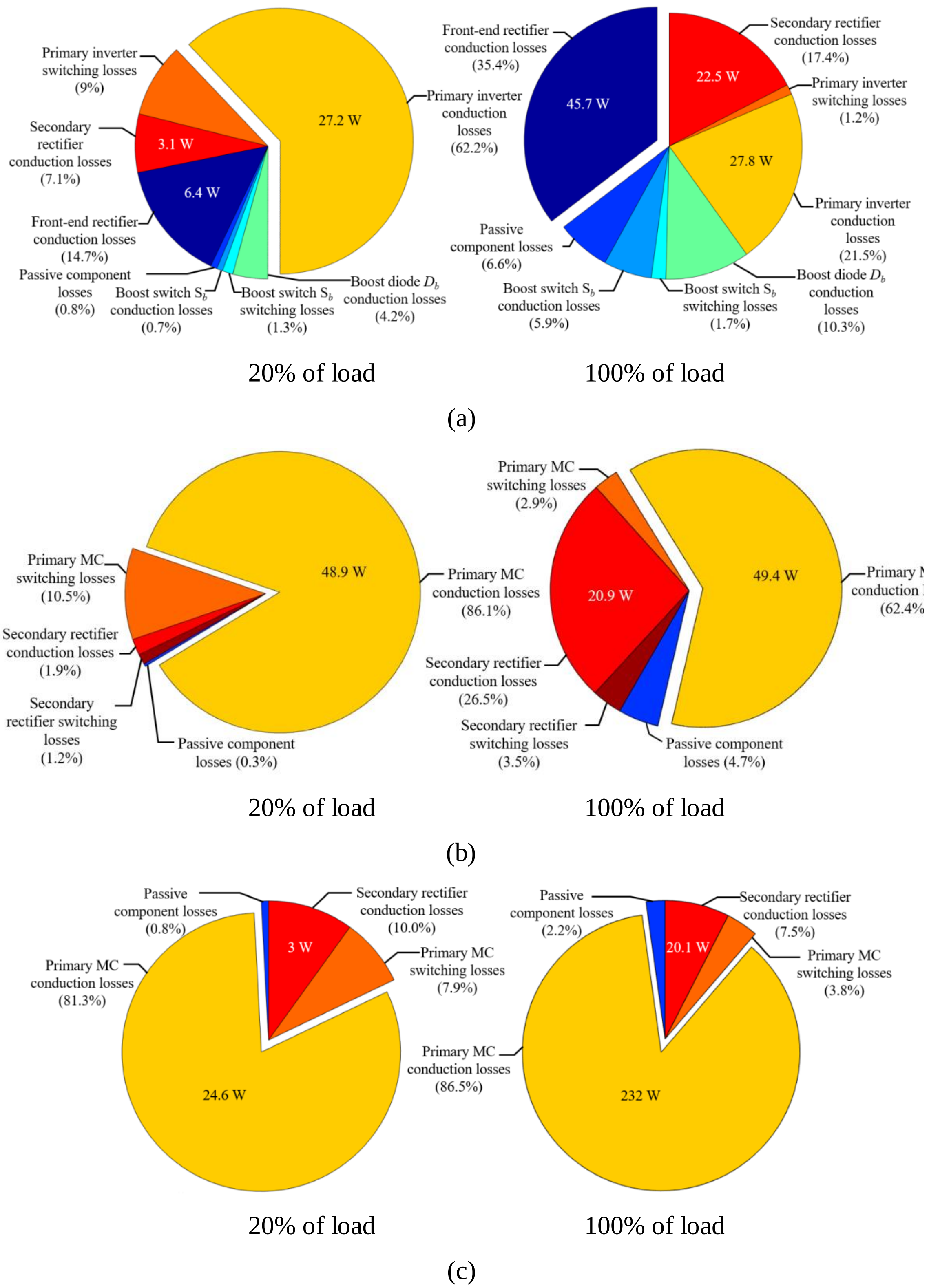


Figure 3.10: Loss distribution. (a) Dual-stage topology, (b) Buck-derived FBMC, and (c) Boost-derived FBMC.

As shown in Figure 3.10 (c), the conduction loss of the boost-derived MC converter dramatically increases with the increase in load, and its maximum value at the full-load condition is much higher compared to the other topologies. As a result, a higher heat is produced, which requires a larger cooling system. Moreover, based on the detail loss distribution, the opportunities of efficiency improvement can be explored. Particularly, the PFC rectifier (front-end diode rectifier and boost converter) contributes significant losses in the dual-stage topology, as shown in Figure 3.10 (a), so it can be replaced with an active FB PFC rectifier with lower losses [111], in turn to increase the system efficiency.

3.3.4 Cost

Cost is also an important quantity to evaluate the performance of a power converter. The cost structure of each charging system excluding inductive coupling coils and compensation networks is illustrated in Figure 3.11. The costs of the power conversion stages are calculated based on the component cost, referred to Digikey and Mouser on June 20, 2020, given in Table 3.3. In order to simplify the cost analysis, the auxiliary cost including printed circuit board (PCB) cost, cooling system cost and housing cost is assumed to be 10% of the power converter cost. Note that, MOSFETs are driven by isolated gate drivers, and MOSFETs having common-source connection utilize a common gate driver power supply to reduce the system cost. This shows that the cost of single-stage systems is lower than that of the dual-stage counterpart. The buck-derived FBMC system is the most cost-effective solution, it presents 6.3 % less cost than the dual-stage system. It is found that the costs of the passive components dominate in the dual-stage system, whereas the semiconductor devices of MCs occupy the largest portions in the total cost of the single-stage systems.

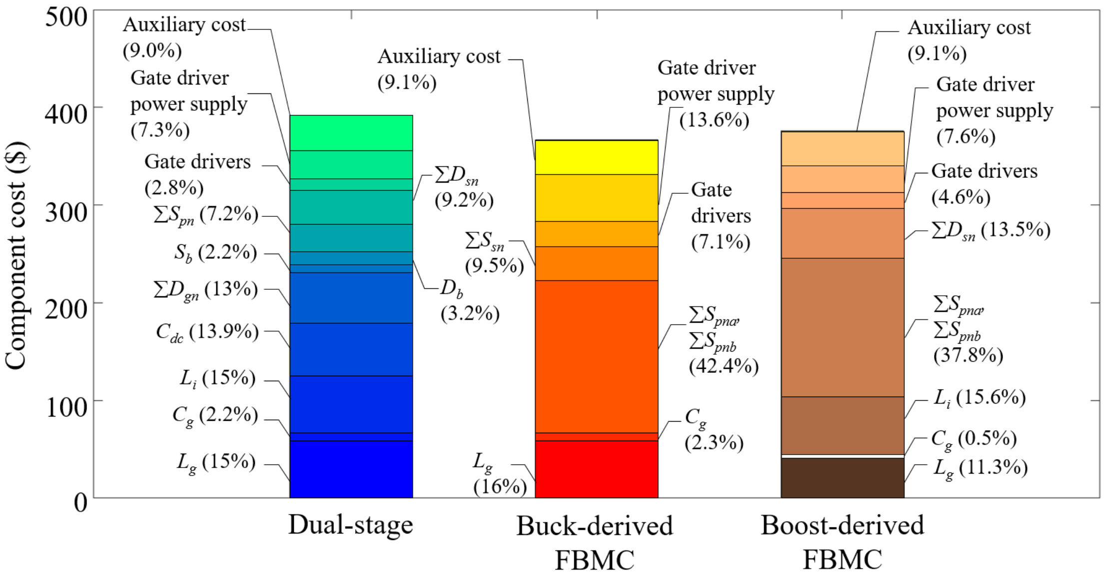


Figure 3.11: Component cost structure of the charging system excluding inductive coupling coils and compensation networks.

3.4 Discussions

From the above analysis, it can be observed that the three IPT charging systems have their own advantages and disadvantages. The MC based IPT systems advantageously adopt the SRC charging technique and remove the intermediate DC-link capacitors. A comparison summary of the three IPT charging systems is shown in Figure 3.12, where performance indices are presented on a scale range from 1 (worst) to 3 (best). In order to evaluate the efficiencies of the three systems, their average values under all load conditions are considered. The switching stresses are assessed based on the product of the maximum current and voltage stresses. It is concluded that the buck-derived FBMC surpasses the other counterparts with the advantages of high efficiency, cost reduction and possible power density improvement due to less component count, while the boost-derived FBMC

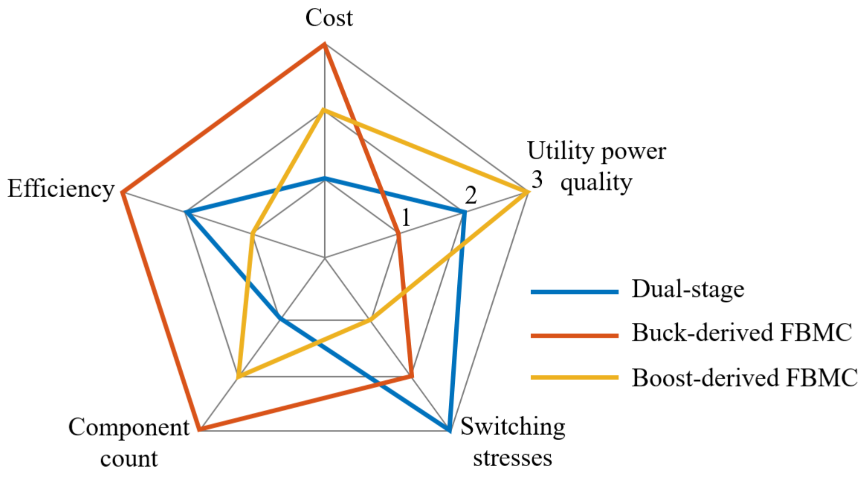


Figure 3.12: Comparison summary of the dual-stage and single-stage IPT systems.

has the greatest input current quality due to the feature of the continuous input current with ripple frequency at a twice switching frequency. The conventional dual-stage topology has the lowest stress on switching devices, and its efficiency maintains a comparable level over wide load range.

3.5 Summary

This chapter presented design considerations of the conventional dual-stage topology and two potential single-stage topologies including buck- and boost-derived FBMCs were presented with detailed design equations. In addition, the comprehensive performance comparison of these topologies was provided through the simulation results. The comparison strengthened the understanding of the properties and issues of the systems, which is a crucial guideline for improving the IPT systems. It can be seen that although the DC-link capacitors are removed in the single-stage topologies, they still have the drawbacks of many active switches (4 bidirectional switches = 8 MOSFETs), complex control strategies, or low input current quality. In order to further improve the system performance, new switch-count-reduced single-stage topologies with a simple control scheme and high-quality input power should be developed.

Chapter 4. Soft-switched, Active-clamped Half-bridge Boost Inverter for Inductive Wireless Charging Applications – Operation Principles, Modeling and Design

4.1 Introduction

An inductive wireless charging system basically consists of a loosely coupled coil pair, compensation networks, a primary inverter, and a secondary rectifier. Both the primary and secondary capacitive compensation networks are required in IPT systems to compensate reactive power consumed by the coils, consequently to reduce the VA rating of the power converters, and to increase the power transfer efficiency of the system [139]. Based on the placement of compensation capacitors, the four basic topologies of compensation networks can be classified such as SS, SP, PS, and PP [80, 142-144]. Among the aforementioned compensation networks, the SS topology is suitable for the EV charging applications since it is simple, load/mutual coupling-independent compensation, constant output current, efficient, cost-effective, and has low coil-fabrication copper mass in high-power applications [19, 56, 62-64].

In the inversion stage, the CSIs or the VSIs can be employed to generate a high-frequency AC current or voltage feeding the primary coil through the compensation network. The VSIs are widely utilized in the IPT applications due to high efficiency, low component count, and low control complexity [81, 121-123, 127, 137]. However, the discontinuous input current in the VSIs requires a bulky input EMI filter which is the major drawback. The CSIs are preferable in applications where a continuous and low-ripple input current is demanded. However, CSI based IPT systems have some of following drawbacks: 1) Extra blocking diodes are required, which increases the inverter design complexity, the size and the cost of the systems; 2) The CSIs are compatible to the primary parallel compensation topologies, in which the compensation capacitor values varies with the variation of mutual inductance and load, and the inverter switches suffer from high voltage stress; and 3) CSI based IPT systems usually adopt the variable frequency control technique for load regulation, which causes the start-up and bifurcation issues, as well as a significant efficiency degradation due to a large circulating current when the switching frequency highly deviates from the resonant frequency.

The use of an active-clamped half-bridge boost inverter (HBBI), in which a boost converter is integrated with a HB VSI, can overcome the above issues. According to [145], the major advantages of this particular inverter are listed as follows:

1) Switching component count is less compared to the CSIs and FB VSI;
2) Low-ripple input current minimizes input filter;
3) Unlike conventional CSIs, the active-clamped HBBI generates a high-frequency voltage, so it is naturally compatible to the SS-IPT system;
4) The active-clamped HBBI can adopt both the fixed-frequency and variable frequency control techniques for the load regulation.

In the fixed frequency control, the switching frequency of the inverter is kept at a constant value, which is slightly different from the primary resonant frequency to obtain soft-switching operation. In order to control the power flow, the duty cycle of the inverter switches is varied. For the variable switching frequency control scheme, the duty cycle of the gating signals is maintained constant at 50% and the switching frequency is varied to regulate the output power. However, in the EV charging applications with a wide variation of the mutual inductance and load, the frequency control method requires a wide operating frequency band to regulate output power. It causes the difficulties to comply the light-duty EV static wireless charging standard, SAEJ2954, with a limited operating frequency band of 81.39 kHz - 90 kHz, and to design passive components. Moreover, it exacerbates EMI problems, and efficiency degradation [53, 143, 146]. In this chapter, the analysis, modeling, and design for the fixed-frequency-controlled active-clamped HBBI based SS-IPT charging system are presented in detail. Figure 4.1 shows the topology of the active-clamped HBBI based SS-IPT charging system.

The achievement of an accurate modeling plays a vital role in the design and control of switching power converters. The well-known state-space averaging method [147] is successfully used to model switching power converters; however, this method is invalid to model resonant converters, where the switching frequency of the converters is close to the natural frequency of the resonant circuits. Among the modeling techniques for the resonant converters, the EDF method [148] is widely used because it is simple, intuitive and accurate. Here, the EDF method is adopted for modeling the active-clamped HBBI based

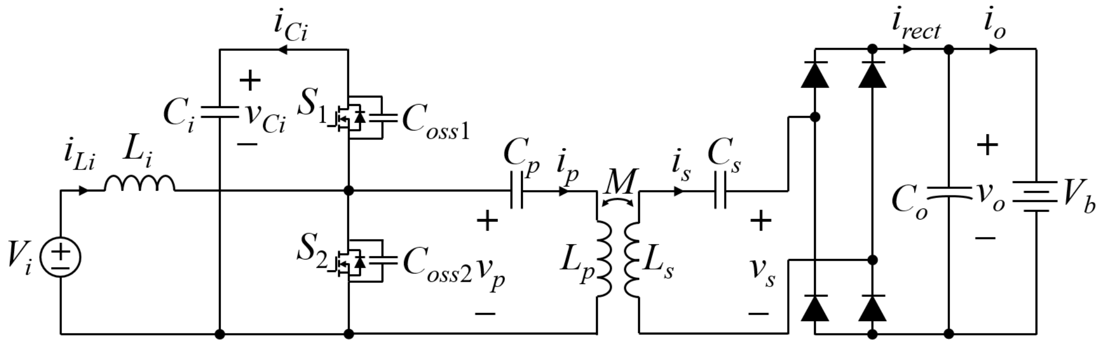


Figure 4.1: Active-clamped HBBI based SS-IPT charging system.

SS-IPT charging system. By using the EDF method, the large-signal model, steady-state model and small-signal model are obtained. The steady-state analysis is used to develop an effective design approach to achieve ZVS operation for the active-clamped HBBI based SS-IPT charging system. In addition, the proposed design approach allows the system to avoid the bifurcation.

4.2 Operation Principles

The key steady-state waveforms of the active-clamped HBBI based SS-IPT charging system are shown in Figure 4.2. The steady-state duty cycle D is defined as the ratio between the on-time of the upper switch S_1 and the switching period, T_s, without considering dead time. However, in practical implementation, a dead time t_d is introduced to prevent the short circuit through the clamping capacitor C_i. For operation analysis, the system is simplified by replacing the secondary circuit with an equivalent impedance Z_{eq} [63]. Eight operation modes can be classified in one switching cycle as shown in Figure 4.3.

Mode 1 ($t_0 – t_1$): This mode begins with $i_p > i_{Li}$. During this mode, the boost inductor L_i discharges its energy into the resonant tank. The difference between the input current i_{Li} and the primary current i_p is compensated by capacitor C_i through the upper switch S_1, which has been turned ON in the previous interval. This mode finishes when S_1 is turned OFF.

Mode 2 ($t_1 – t_2$): The upper switch S_1 is turned OFF at $t = t_1$. Due to the dead time, the lower S_2 is still OFF, and the difference between i_{Li} and i_p is shared to charge and discharge the output capacitors of the switches, C_{oss1} and C_{oss2}, respectively. This mode

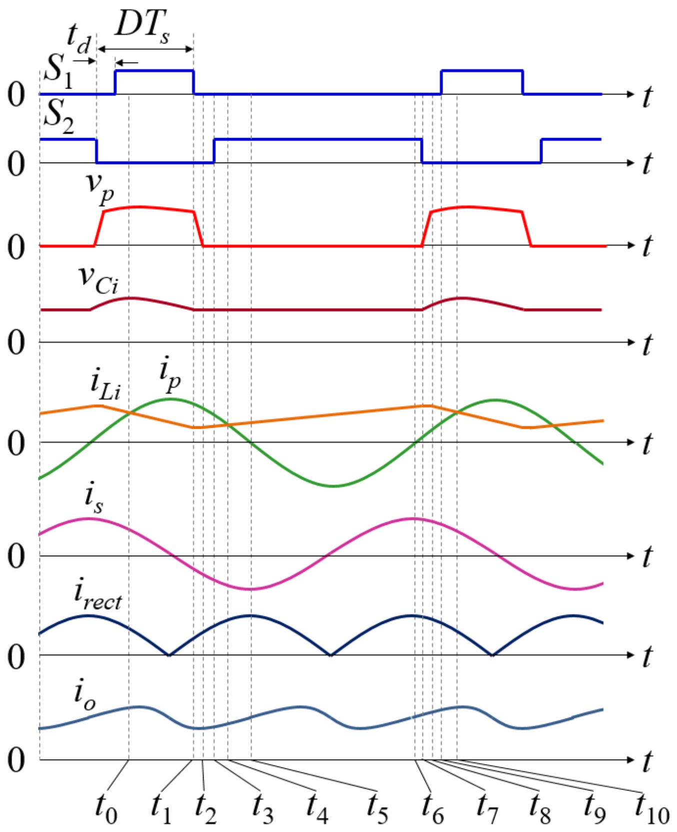


Figure 4.2: Steady-state waveforms of the active-clamped HBBI based SS-IPT charging system.

finishes at $t = t_2$ when the voltage across C_{oss1} reaches V_{Ci}, and the voltage across C_{oss2} becomes zero. The interval of this mode can be given as

$$\Delta t_{\text{mode 2}} = t_2 - t_1 = \frac{(C_{oss1} + C_{oss2})V_{Ci}}{i_p(t_1) - i_{Li}(t_1)} \tag{4.1}$$

Mode 3 ($t_2 - t_3 - t_4$): As soon as voltage across S_2 reaches zero, the body diode of S_2 starts conducting a current equal $i_p - i_{Li}$. The input current i_{Li} flows through the resonant tank to charge the boost inductor L_i, and it begins linearly increase. At $t = t_3$, S_2 is turned

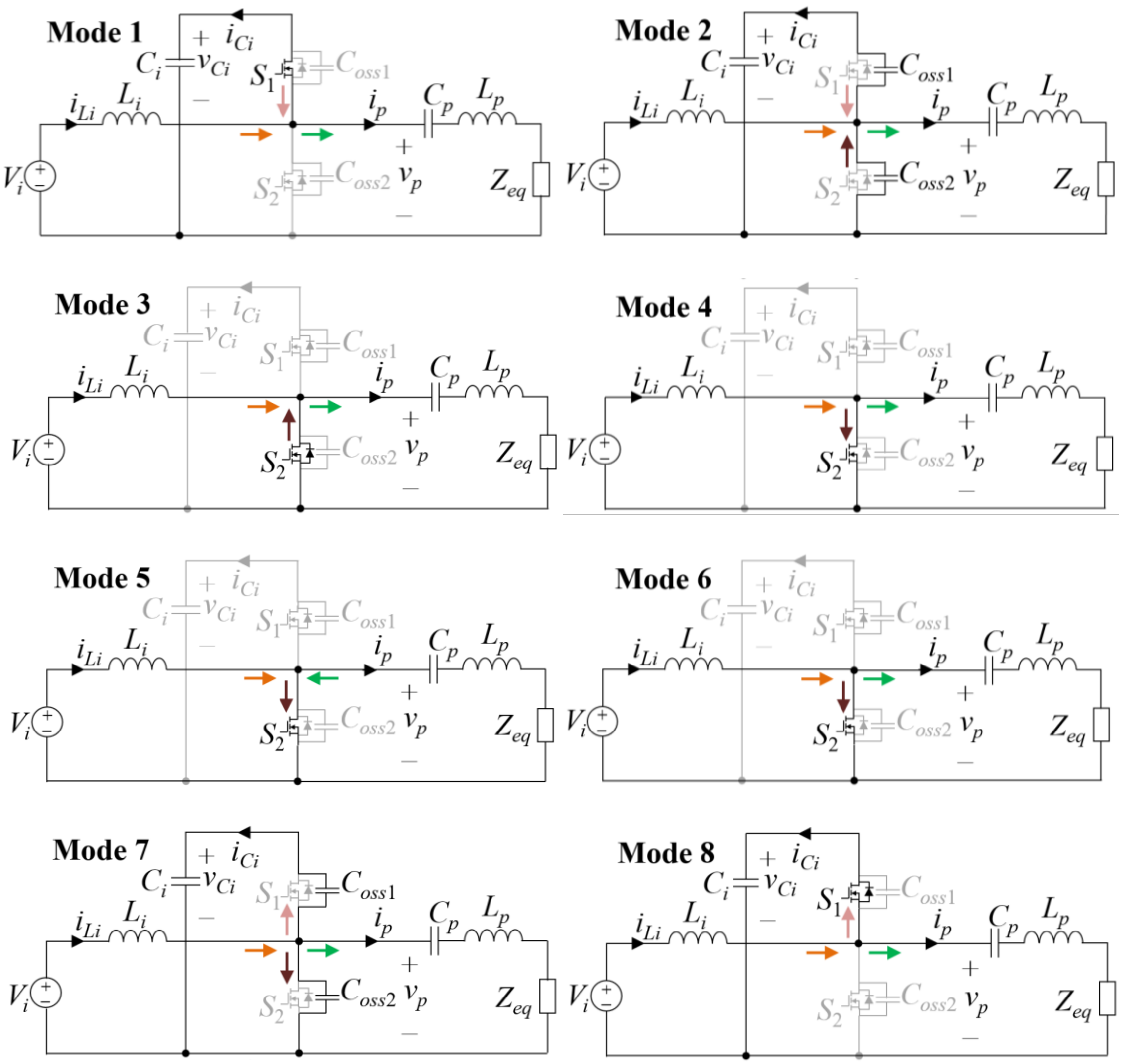


Figure 4.3: Circuit states of the operation modes during one switching cycle.

ON with ZVS because its body diode has been conducting in the previous interval. This mode finishes at $t = t_4$ when i_{Li} is equal to i_p.

Mode 4 ($t_4 - t_5$): This mode begins with $i_p < i_{Li}$. The current flowing through S_2 reverses its direction. The input current i_{Li} is still linearly increasing. This mode finishes at $t = t_5$ when i_p becomes zero.

Mode 5 ($t_5 - t_6$): During this mode, i_p becomes negative, and S_2 carries both i_p and i_{Li}. The input current i_{Li} keeps linearly increasing. This mode finishes at $t = t_6$ when i_p returns to zero.

Mode 6 ($t_6 - t_7$): This mode begins with $i_p > 0$, and it is identical to mode 4.

Mode 7 ($t_7 - t_8$): The switch S_2 is turned OFF at $t = t_7$. Due to the dead time, S_1 is still OFF, and the difference between i_{Li} and i_p is shared to discharge and charge C_{oss1} and C_{oss2}, respectively. The input current i_{Li} starts decreasing. This mode finishes at $t = t_8$ when the voltage across the capacitor C_{oss1} is zero and the voltage across C_{oss2} reaches V_{Ci}. The interval of this mode can be expressed as

$$\Delta t_{\text{mode }7} = t_8 - t_7 = \frac{(C_{oss1} + C_{oss2})V_{Ci}}{i_{Li}(t_7) - i_p(t_7)} \tag{4.2}$$

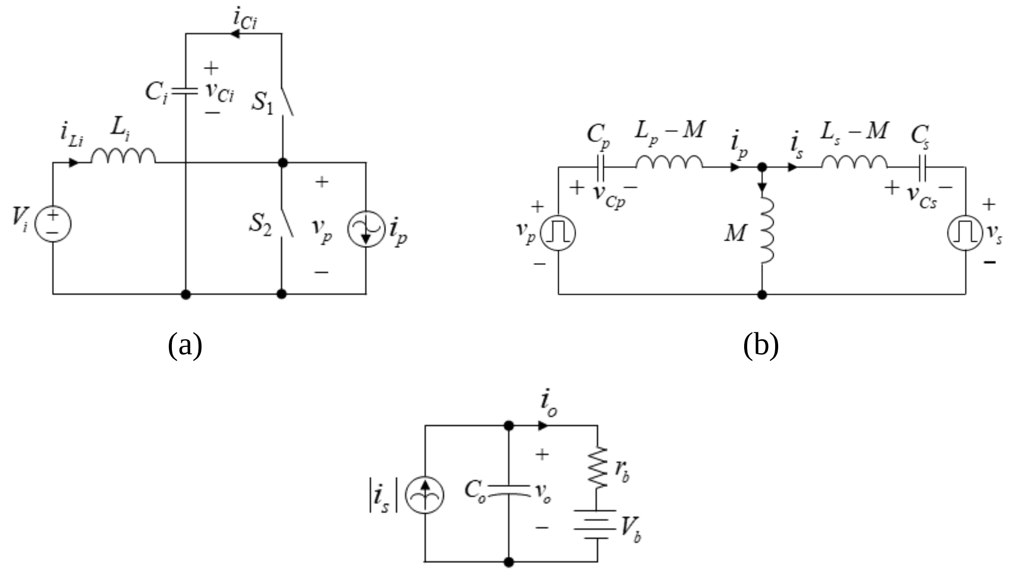
Mode 8 ($t_8 - t_9 - t_{10}$): As soon as the voltage across S_1 becomes zero, the body diode of S_1 starts conducting a current equal $i_{Li} - i_p$. The boost inductor L_i discharges its energy into the resonant tank and the capacitor C_i. The current i_{Li} linearly decreases. At $t = t_9$, S_1 is turned ON with ZVS because its body diode has been conducting in the previous interval. At $t = t_{10}$, i_p equals i_{Li}, and the circuit state returns to mode 1 to restart a new cycle.

4.3 Modeling Analysis

Figure 4.4 shows the equivalent circuit of the proposed IPT charging system. The M-equivalent circuit is used to model the loosely coupled coils for the analysis in. In order to simplify the analysis, some assumptions are made as follows:

1) All switches and diodes are ideal.

2) Dead time is neglected.



(a)

(b)

(c)

Figure 4.4: Equivalent circuits. (a) Inversion stage, (b) Resonant inductive coupling, and (c) Rectification stage.

3) Inductors, capacitors and coils have no parasitic resistance

4) Boost inductor L_i is sufficiently large to maintain constant low-ripple current.

5) Capacitors C_i and C_o are sufficiently large to maintain constant low-ripple voltages.

6) Primary and secondary currents (i_p and i_s) are nearly sinusoidal.

4.3.1 Nonlinear State Equations

Based on the equivalent circuits shown in Figure 4.4, the nonlinear state equations can be derived as follows

$$L_i \frac{di_{Li}}{dt} = v_i - m v_{Ci} \tag{4.3}$$

$$C_i \frac{dv_{Ci}}{dt} = m\left(i_{Li} - i_p\right) \tag{4.4}$$

$$L_p \frac{di_p}{dt} = v_p - v_{Cp} + M \frac{di_s}{dt} \tag{4.5}$$

$$L_s \frac{di_s}{dt} = -v_s - v_{Cs} + M \frac{di_p}{dt} \tag{4.6}$$

$$C_p \frac{dv_{Cp}}{dt} = i_p \tag{4.7}$$

$$C_s \frac{dv_{Cs}}{dt} = i_s \tag{4.8}$$

$$C_o \frac{dv_o}{dt} = |i_s| - i_o \tag{4.9}$$

where m in (4.3) and (4.4) is the switching function of the inverter. It equals 1 when S_1 is ON and S_2 is OFF, otherwise it equals 0.

$$m = \begin{cases} 1, & \frac{T_s}{4} - \frac{dT_s}{2} \le t \le \frac{T_s}{4} + \frac{dT_s}{2} \\ 0, & \text{otherwise} \end{cases} \tag{4.10}$$

where d is the duty cycle defined with respect to the on-time of S_1.

By rearranging (4.5) and (4.6), we have

$$\frac{di_p}{dt} = \frac{1}{L_2} v_p - \frac{1}{L_2} v_{Cp} - \frac{1}{L_m} v_{Cs} - \frac{1}{L_m} v_s \tag{4.11}$$

$$\frac{di_s}{dt} = \frac{1}{L_m} v_p - \frac{1}{L_m} v_{Cp} - \frac{1}{L_1} v_{Cs} - \frac{1}{L_1} v_s \tag{4.12}$$

where $L_1 = \dfrac{L_p L_s - M^2}{L_p}$, $L_2 = \dfrac{L_p L_s - M^2}{L_s}$, and $L_m = \dfrac{L_p L_s - M^2}{M}$.

The output voltage v_o is given as

$$v_o = r_b i_o + v_b \tag{4.13}$$

where r_b is the internal battery resistance.

4.3.2 Harmonic Approximation and Extended Describing Functions

In the resonant inductive coupling circuit shown in Figure 4.4 (b), the primary and secondary currents, i_p and i_s, and the primary and secondary compensation capacitor voltages, v_{Cp}, and v_{Cs}, are nearly sinusoidal. Thus, they can be approximated to their fundamental components which are described in sine and cosine terms [149]. Equations (4.14)–(4.17) show their approximation and the derivative of these quantities

$$i_x = i_{xs} \sin \omega_s t + i_{xc} \cos \omega_s t \tag{4.14}$$

$$v_{Cx} = v_{Cxs} \sin \omega_s t + v_{Cxc} \cos \omega_s t \tag{4.15}$$

$$\frac{di_x}{dt} = \left(\frac{di_{xs}}{dt} - i_{xc}\omega_s \right) \sin \omega_s t + \left(\frac{di_{xc}}{dt} + i_{xs}\omega_s \right) \cos \omega_s t \tag{4.16}$$

$$\frac{dv_{Cx}}{dt} = \left(\frac{dv_{Cxs}}{dt} - v_{Cxc}\omega_s \right) \sin \omega_s t + \left(\frac{dv_{Cxc}}{dt} + v_{Cxs}\omega_s \right) \cos \omega_s t \tag{4.17}$$

where x refer to p and s.

Also, the nonlinear terms, v_p and v_s, in the resonant inductive coupling circuit can be approximated to their fundamental components

$$v_p = mv_{Ci} = \frac{2}{\pi} v_{Ci} \sin \pi d \sin \omega_s t \tag{4.18}$$

$$v_s = sign(i_s) v_o = \frac{4v_o}{\pi} \frac{i_{ss}}{i_{sp}} \sin \omega_s t + \frac{4v_o}{\pi} \frac{i_{sc}}{i_{sp}} \cos \omega_s t \tag{4.19}$$

where the operator $sign(\bullet)$ is the sign function, and $i_{sp} = \sqrt{i_{ss}^2 + i_{sc}^2}$.

In the inversion and rectification stages, the state variables, i_{Li}, v_{Ci}, i_o, and v_o, are dominated by DC components, so they are approximated to their DC components. The DC approximation of the terms $v_i - mv_{Ci}$, $m(i_{Li} - i_p)$, and $|i_s|$ in (4.3), (4.4), and (4.9) can be obtained as follows

$$\langle v_i - mv_{Ci} \rangle_{dc} = \frac{1}{T_s} \int_0^{T_s} (v_i - mv_{Ci}) dt = v_i - dv_{Ci} \tag{4.20}$$

$$\langle m(i_{Li} - i_p) \rangle_{dc} = \frac{1}{T_s} \int_0^{T_s} m(i_{Li} - i_p) dt = di_{Li} - \frac{1}{\pi} i_{ps} \sin \pi d \tag{4.21}$$

$$\langle |i_s| \rangle_{dc} = \frac{1}{T_s} \int_0^{T_s} |i_s| dt = \frac{2}{\pi} i_{sp} = \frac{2}{\pi} \sqrt{i_{ss}^2 + i_{sc}^2} \tag{4.22}$$

where the operator $\langle \bullet \rangle_{dc}$ denotes the DC approximation function.

4.3.3 Harmonic Balance

By applying (4.14)–(4.22) to (4.3)–(4.4), (4.7)–(4.9), and (4.11)–(4.12), we obtain

$$\frac{di_{Li}}{dt} = \frac{1}{L_i} v_i - \frac{d}{L_i} v_{Ci} \tag{4.23}$$

$$\frac{dv_{Ci}}{dt} = \frac{d}{C_i} i_{Li} - \frac{1}{\pi C_i} i_{ps} \sin \pi d \tag{4.24}$$

$$\begin{aligned} \frac{di_{pc}}{dt} \cos \omega_s t + \frac{di_{ps}}{dt} \sin \omega_s t &= \left(-\frac{1}{L_2} v_{Cpc} - \frac{1}{L_m} v_{Csc} - i_{ps} \omega_s - \frac{4}{\pi L_m} \frac{i_{sc} v_o}{i_{sp}} \right) \cos \omega_s t \\ &+ \left(\frac{2}{\pi L_2} v_{Ci} \sin \pi d - \frac{1}{L_2} v_{Cps} - \frac{1}{L_m} v_{Css} + i_{pc} \omega_s - \frac{4}{\pi L_m} \frac{i_{ss} v_o}{i_{sp}} \right) \sin \omega_s t \end{aligned} \tag{4.25}$$

$$\begin{aligned} \frac{di_{sc}}{dt} \cos \omega_s t + \frac{di_{ss}}{dt} \sin \omega_s t &= \left(-\frac{1}{L_m} v_{Cpc} - \frac{1}{L_1} v_{Csc} - i_{ss} \omega_s - \frac{4}{\pi L_1} \frac{i_{sc} v_o}{i_{sp}} \right) \cos \omega_s t \\ &+ \left(\frac{2}{\pi L_m} v_{Ci} \sin \pi d - \frac{1}{L_m} v_{Cps} - \frac{1}{L_1} v_{Css} + i_{sc} \omega_s - \frac{4}{\pi L_1} \frac{i_{ss} v_o}{i_{sp}} \right) \sin \omega_s t \end{aligned} \tag{4.26}$$

$$\begin{aligned} \frac{dv_{Cpc}}{dt} \cos \omega_s t + \frac{dv_{Cps}}{dt} \sin \omega_s t &= \left(\frac{1}{C_p} i_{pc} - v_{Cps} \omega_s \right) \cos \omega_s t \\ &+ \left(\frac{1}{C_p} i_{ps} + v_{Cpc} \omega_s \right) \sin \omega_s t \end{aligned} \tag{4.27}$$

$$\begin{aligned} \frac{dv_{Csc}}{dt} \cos \omega_s t + \frac{dv_{Css}}{dt} \sin \omega_s t &= \left(\frac{1}{C_s} i_{sc} - v_{Css} \omega_s \right) \cos \omega_s t \\ &+ \left(\frac{1}{C_s} i_{ss} + v_{Csc} \omega_s \right) \sin \omega_s t \end{aligned} \tag{4.28}$$

$$\frac{dv_o}{dt} = \frac{2}{\pi C_o} i_{sp} - \frac{i_o}{C_o} \tag{4.29}$$

Equating the coefficients of sine, cosine and DC terms in (4.23)–(4.29), the following equations can be derived

$$\frac{di_{Li}}{dt} = \frac{1}{L_i} v_i - \frac{d}{L_i} v_{Ci} \tag{4.30}$$

$$\frac{dv_{Ci}}{dt} = \frac{d}{C_i} i_{Li} - \frac{1}{\pi C_i} i_{ps} \sin \pi d \tag{4.31}$$

$$\frac{di_{ps}}{dt} = \frac{2}{\pi L_2} v_{Ci} \sin \pi d - \frac{1}{L_2} v_{Cps} - \frac{1}{L_m} v_{Css} + i_{pc} \omega_s - \frac{4}{\pi L_m} \frac{i_{ss} v_o}{i_{sp}} \tag{4.32}$$

$$\frac{di_{pc}}{dt} = -\frac{1}{L_2} v_{Cpc} - \frac{1}{L_m} v_{Csc} - i_{ps} \omega_s - \frac{4}{\pi L_m} \frac{i_{sc} v_o}{i_{sp}} \tag{4.33}$$

$$\frac{di_{ss}}{dt} = \frac{1}{L_m} \frac{2}{\pi} v_{Ci} \sin \pi d - \frac{1}{L_m} v_{Cps} - \frac{1}{L_1} v_{Css} + i_{sc} \omega_s - \frac{4}{\pi L_1} \frac{i_{ss} v_o}{i_{sp}} \tag{4.34}$$

$$\frac{di_{sc}}{dt} = -\frac{1}{L_m} v_{Cpc} - \frac{1}{L_1} v_{Csc} - i_{ss} \omega_s - \frac{4}{\pi L_1} \frac{i_{sc} v_o}{i_{sp}} \tag{4.35}$$

$$\frac{dv_{Cps}}{dt} = \frac{1}{C_p} i_{ps} + v_{Cpc} \omega_s \tag{4.36}$$

$$\frac{dv_{Cpc}}{dt} = \frac{1}{C_p} i_{pc} - v_{Cps} \omega_s \tag{4.37}$$

$$\frac{dv_{Css}}{dt} = \frac{1}{C_s} i_{ss} + v_{Csc} \omega_s \tag{4.38}$$

$$\frac{dv_{Csc}}{dt} = \frac{1}{C_s} i_{sc} - v_{Css} \omega_s \tag{4.39}$$

$$\frac{dv_o}{dt} = \frac{2}{\pi C_o} i_{sp} - \frac{i_o}{C_o} \tag{4.40}$$

The equations (4.13), and (4.30)–(4.40) represent the large-signal model of the active-clamped HBBI based SS-IPT charging system. The steady-state model and small-signal model can be extracted from this model.

4.3.4 Steady-state Model

In the steady-state condition, all variables in (4.13), and (4.30)–(4.40) are constant, thus their derivatives equal zero. Upper-case letters are used to denote the steady-state values. The detailed derivation of the steady-state equations can be found in Appendix A. The steady-state solution is given as follows

$$X_{st} = A_{st}^{-1} B_{st} \tag{4.41}$$

$$V_{Ci} = V_i / D \tag{4.42}$$

$$I_{Li} = \frac{I_{ps}}{\pi D} \sin \pi D \tag{4.43}$$

$$I_o = 2 I_{sp} / \pi \tag{4.44}$$

$$V_o = r_b I_o + V_b \tag{4.45}$$

where

$$A_{st} = \begin{bmatrix} 0 & -\Omega_s L_2 & L_2 R_s / L_m & 0 & 1 & 0 & L_2 / L_m & 0 \\ 0 & 0 & L_m R_s / L_1 & -\Omega_s L_m & 1 & 0 & L_m / L_1 & 0 \\ 0 & 0 & \Omega_s L_1 & R_s & 0 & L_1 / L_m & 0 & 1 \\ \Omega_s L_m & 0 & 0 & R_s & 0 & L_m / L_2 & 0 & 1 \\ 0 & 1 & 0 & 0 & -\Omega_s C_p & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & -\Omega_s C_s & 0 \\ 1 & 0 & 0 & 0 & 0 & \Omega_s C_p & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & \Omega_s C_s \end{bmatrix},$$

$$B_{st} = \begin{bmatrix} \frac{2V_i \sin \pi D}{\pi D} & \frac{2V_i \sin \pi D}{\pi D} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T ,$$

$$X_{st} = \begin{bmatrix} I_{ps} & I_{pc} & I_{ss} & I_{sc} & V_{Cps} & V_{Cpc} & V_{Css} & V_{Csc} \end{bmatrix}^T ,$$

$$R_s = \frac{8}{\pi^2}(r_b + \frac{V_b}{I_o}) ,$$

$$I_{sp} = \sqrt{I_{ss}^2 + I_{sc}^2} .$$

4.3.5 Small-signal Model

The small-signal model can be derived by perturbing and linearizing the large-signal model. Firstly, each variable in (4.13), and (4.30)–(4.40) is decomposed in a steady-state value and a small perturbation. Then by linearizing the nonlinear terms (using Taylor's series expansion in Appendix A.1) and separating perturbation terms from the steady-state terms. The detailed derivation of the small-signal equations can be found in Appendix A. The small-signal model in a state-space representation can be expressed as

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} \tag{4.46}$$

$$\hat{y} = C\hat{x} + D\hat{u} \tag{4.47}$$

where the operator $\hat{\bullet}$ denotes the perturbation term, and

$$A=\begin{bmatrix} 0 & -K_1/L_m & \Omega_s & K_2/L_m & 0 & 0 & -1/L_2 & -1/L_m & 0 & K_3/L_2 & -K_4/L_m \\ 0 & -K_1/L_1 & 0 & K_2/L_1+\Omega_s & 0 & 0 & -1/L_m & -1/L_1 & 0 & K_3/L_m & -K_4/L_1 \\ -\Omega_s & K_2/L_m & 0 & -K_5/L_m & -1/L_2 & -1/L_m & 0 & 0 & 0 & 0 & -K_6/L_m \\ 0 & K_2/L_1-\Omega_s & 0 & -K_5/L_1 & -1/L_m & -1/L_1 & 0 & 0 & 0 & 0 & -K_6/L_1 \\ 0 & 0 & 1/C_p & 0 & 0 & 0 & -\Omega_s & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/C_s & 0 & 0 & 0 & -\Omega_s & 0 & 0 & 0 \\ 1/C_p & 0 & 0 & 0 & \Omega_s & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C_s & 0 & 0 & 0 & \Omega_s & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -D/L_i & 0 \\ -K_3/2C_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & D/C_i & 0 & 0 \\ 0 & K_4/2C_o & 0 & K_6/2C_o & 0 & 0 & 0 & 0 & 0 & 0 & -1/r_bC_o \end{bmatrix}$$

$$B=\begin{bmatrix} I_{pc} & 0 & K_7/L_2 & 0 \\ I_{sc} & 0 & K_7/L_m & 0 \\ -I_{ps} & 0 & 0 & 0 \\ -I_{ss} & 0 & 0 & 0 \\ -V_{Cps} & 0 & 0 & 0 \\ -V_{Css} & 0 & 0 & 0 \\ V_{Cpc} & 0 & 0 & 0 \\ V_{\mathrm{Csc}} & 0 & 0 & 0 \\ 0 & 1/L_i & -V_{Ci}/L_i & 0 \\ 0 & 0 & \left(I_{Li}-K_8\right)/C_i & 0 \\ 0 & 0 & 0 & 1/r_bC_o \end{bmatrix},$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/r_b \end{bmatrix},$$

$$D=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/r_b \end{bmatrix},$$

$$\hat{x}=\begin{bmatrix} \hat{i}_{ps} & \hat{i}_{ss} & \hat{i}_{pc} & \hat{i}_{sc} & \hat{v}_{Cpc} & \hat{v}_{\mathrm{Csc}} & \hat{v}_{Cps} & \hat{v}_{Css} & \hat{i}_{Li} & \hat{v}_{Ci} & \hat{v}_o \end{bmatrix}^T,$$

$\hat{u} = \begin{bmatrix} \hat{\omega}_s & \hat{v}_i & \hat{d} & \hat{v}_b \end{bmatrix}^T$, $\hat{y} = \begin{bmatrix} \hat{i}_{Li} & \hat{v}_o & \hat{i}_o \end{bmatrix}^T$,

$K_1 = \dfrac{4I_{sc}^2 V_o}{\pi I_{sp}^3}$, $K_2 = \dfrac{4I_{ss} I_{sc} V_o}{\pi I_{sp}^3}$, $K_3 = \dfrac{2\sin \pi D}{\pi}$,

$K_4 = \dfrac{4I_{ss}}{\pi I_{sp}}$, $K_5 = \dfrac{4I_{ss}^2 V_o}{\pi I_{sp}^3}$, $K_6 = \dfrac{4I_{sc}}{\pi I_{sp}}$,

$K_7 = 2V_{Ci} \cos \pi D$, $K_8 = I_{ps} \cos \pi D$.

Control-to-output transfer functions can be obtained as follows

$$G(s) = \frac{Y(s)}{U(s)} = C(sI - A)^{-1} B + D \tag{4.48}$$

where *s* is the Laplace operator, and *I* is the identity matrix.

4.4 Design Approach for ZVS

In order to reduce the switching losses of the inverter, soft switching is necessary. In this section, a design approach is proposed to achieve ZVS for the active-clamped HBBI based SS-IPT charging system controlled by the fixed-frequency PWM scheme. In the proposed design procedure, the secondary coil is tuned to the switching frequency to maximize the power transfer capability. The design guidelines in [130] are employed to avoid the bifurcation phenomenon.

4.4.1 Boost Inductor (L_i)

Regarding the input voltage and the rating voltage of the inverter switches, the minimum value for duty cycle *D* is obtained using (4.42). It is desirable to restrict V_{Ci} to

50% ~ 70% of the peak device voltage. Once the minimum duty cycle is obtained, the boost inductor is designed to meet the input current ripple requirement

$$L_i \geq \frac{(1-D)V_i}{\Delta I_{Li} f_s} \tag{4.49}$$

where ΔI_{Li} is the input current ripple.

The average input current I_{Li} is given by

$$I_{Li} = \frac{P_o}{\eta V_i} \tag{4.50}$$

where P_o is the output power, and η is the system efficiency.

4.4.2 Mutual Inductance (*M*)

As shown in Figure 4.5, the ZVS for S_1 can be obtained when it is activated during $i_p < i_{Li}$, and their difference is sufficiently large to fully discharge and charge C_{oss1} and C_{oss2} during the dead time. On the other hand, the ZVS for S_2 is achieved when it is activated during $i_p > i_{Li}$, and their difference is sufficiently large to fully charge and discharge C_{oss1} and C_{oss2} during the dead time. Thus, the ZVS conditions for S_1 and S_2 are as follows

$$i_p(T_s/4 - DT_s/2 + t_d) \leq I_{Li} + \Delta I_{Li}/2 \tag{4.51}$$

$$t_d \geq \frac{(C_{oss1} + C_{oss2})V_{Ci}}{(I_{Li} + \Delta I_{Li}/2) - i_p(T_s/4 - DT_s/2)} \tag{4.52}$$

$$i_p(T_s/4 + DT_s/2 + t_d) \geq I_{Li} - \Delta I_{Li}/2 \tag{4.53}$$

$$t_d \geq \frac{(C_{oss1} + C_{oss2})V_{Ci}}{i_p(T_s/4 + DT_s/2) - (I_{Li} - \Delta I_{Li}/2)} \tag{4.54}$$

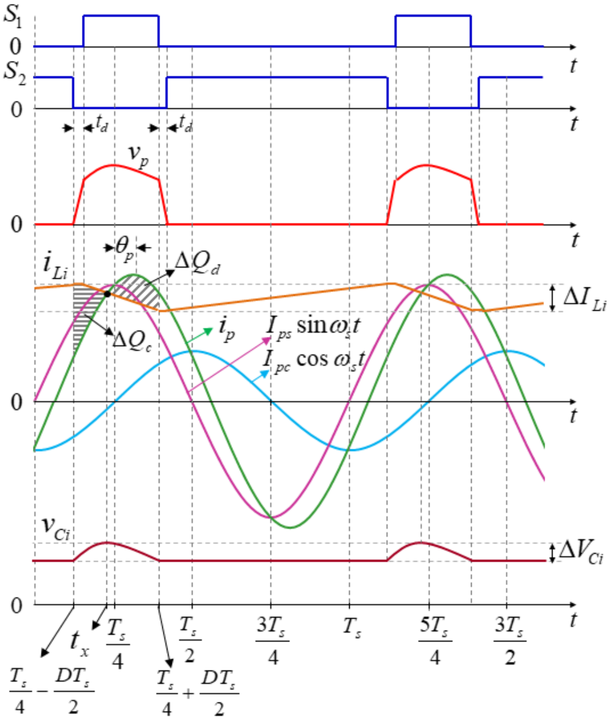


Figure 4.5: Key waveforms of the primary inverter.

In the steady-state condition, the primary current i_p can be represented as

$$i_p(t) = I_{ps}\sin\omega_s t + I_{pc}\cos\omega_s t \tag{4.55}$$

Substituting (4.55) into (4.51)–(4.54), the ZVS conditions for S_1 and S_2 are given as follows

$$I_{pc} \le \frac{I_{Li} + \Delta I_{Li}/2 - I_{ps}\cos(\pi D - 2\pi t_d/T_s)}{\sin(\pi D - 2\pi t_d/T_s)} \tag{4.56}$$

$$I_{pc} \le \frac{I_{Li} + \Delta I_{Li}/2 - (C_{oss1} + C_{oss2})V_{Ci}/t_d - I_{ps}\cos(\pi D)}{\sin(\pi D)} \tag{4.57}$$

$$I_{pc} \le -\frac{I_{Li} - \Delta I_{Li}/2 - I_{ps}\cos(\pi D + 2\pi t_d/T_s)}{\sin(\pi D + 2\pi t_d/T_s)} \tag{4.58}$$

$$I_{pc} \le \frac{-I_{Li} + \Delta I_{Li}/2 - (C_{oss1} + C_{oss2})V_{Ci}/t_d + I_{ps}\cos(\pi D)}{\sin(\pi D)} \tag{4.59}$$

where V_{Ci} and I_{ps} are calculated using (4.42) and (4.43).

To meet all the ZVS conditions of the switches S_1 and S_2, I_{pc} is selected to be less than or equal to the lowest value from (4.56)–(4.59). Once the I_{pc} is selected, the mutual inductance M is designed. Assumed that r_b is small and ignorable, M is obtained as

$$M = \frac{4V_b}{\pi\omega_s I_{pp}} \tag{4.60}$$

where $I_{pp} = \sqrt{I_{ps}^2 + I_{pc}^2}$.

4.4.3 Primary and Secondary Self-inductance (L_p *and* L_s)

The secondary self-inductance L_s is calculated based on secondary quality factor Q_s. The Q_s can be selected in the range of 2 to 10 [150]. The value of L_s is given by

$$L_s = \frac{Q_s R_{eq}}{\omega_0} \tag{4.61}$$

where $R_{eq} = \frac{8}{\pi^2}\frac{V_b^2}{P_o}$ is the AC equivalent resistance seen at the input of the secondary rectifier.

The primary self-inductance L_p is derived as following

$$L_p = \frac{M^2}{k^2 L_s} \tag{4.62}$$

where k is the coupling coefficient. In [130], in order to avoid bifurcation, the k should be

$$k \leq \frac{\sqrt{4Q_s^2 - 1}}{2Q_s^2} \tag{4.63}$$

4.4.4 Primary and Secondary Compensation Capacitors (C_p and C_s)

The secondary compensation capacitor C_s resonates with the secondary self-inductance L_s at the switching frequency, so it is obtained as

$$C_s = \frac{1}{\omega_s^2 L_s} \tag{4.64}$$

The phase angle between v_p and i_p is given by

$$\tan\theta_p = Q_p\left(\frac{\omega_s}{\omega_p} - \frac{\omega_p}{\omega_s}\right) = -\frac{I_{pc}}{I_{ps}} \tag{4.65}$$

where ω_p is primary resonant frequency, and Q_p is the primary quality factor

$$Q_p = \frac{8\omega_p L_p V_b^2}{\pi^2 \omega_s^2 M^2 P_o} \tag{4.66}$$

Substituting (4.66) into (4.65), the primary resonant frequency ω_p can be found

$$\omega_p = \sqrt{\omega_s^2 + \frac{I_{pc}\pi^2\omega_s^3 M^2 P_o}{8I_{ps}L_p V_b^2}} \tag{4.67}$$

Then the primary compensation capacitor C_p is given by

$$C_p = \frac{1}{\omega_p^2 L_p} \tag{4.68}$$

4.4.5 Clamping Capacitor (*C_i*)

To avoid affecting primary resonant tank (L_p and C_p), the clamping capacitor C_i should be sufficiently larger than C_p. Here, C_i is selected to be 50 times the C_p.

$$C_i = 50C_p \tag{4.69}$$

The average voltage across the clamping capacitor is given by (4.42). As shown in Figure 4.5, during $[T_s/4 - DT_s/2,\, t_x]$, i_{Li} is larger than i_p, so C_i is charged, and v_{Ci} gradually increases. Contrarily, during $[t_x,\, T_s/4 + DT_s/2]$, i_{Li} is smaller than i_p, so C_i is discharged, and v_{Ci} decreases. The voltage ripple ΔV_{Ci} across C_i can be approximated as

$$\begin{aligned}\Delta V_{Ci} &\approx \frac{1}{C_i}\int_{t_x}^{\frac{T_s}{4}+\frac{DT_s}{2}} \left(i_p - I_{Li}\right)dt \\ &\approx -\frac{1}{C_i}\left\{\begin{array}{l}\dfrac{I_{pp}}{\omega_s}\left[\cos\left(\omega_s\left(\dfrac{T_s}{4}+\dfrac{DT_s}{2}\right)-\theta_p\right)-\cos\left(\omega_s t_x-\theta_p\right)\right] \\ +I_{Li}\left(\dfrac{T_s}{4}+\dfrac{DT_s}{2}-t_x\right)\end{array}\right\}\end{aligned} \tag{4.70}$$

where $t_x = \dfrac{\arcsin\left(I_{Li}/I_{pp}\right)+\theta_p}{\omega_s}$ is the instant when i_{Li} intersects with i_p.

4.5 Summary

The comprehensive analyses including the operation principles, modeling and ZVS design method for the active-clamped HBBI based SS-IPT charging system under the fixed-frequency control were presented in this chapter. The derivation of the large-signal, steady-state, and small-signal models using the EDF method was provided in detail. The derived steady-state model was employed to develop a design methodology to achieve ZVS and eliminate bifurcation. The derived eleventh-order small-signal model can be used to gain all the transfer functions of the system, which is useful for the system dynamic analysis and controller design. The accuracy and feasibility of the derived models and proposed design methodology will be verified by simulation and experimental results in the next chapter.

Chapter 5. Validation of Soft-Switched, Active-clamped Half-bridge Boost Inverter based Inductive Wireless Charging System

5.1 Hardware Description

To verify the theoretical analysis in Chapter 4, a 1.0-kW laboratory prototype with a closed-loop current controller is designed and implemented as shown in Figure 5.1. The major specifications are as follows: the input voltage V_i = 150 V, the nominal battery voltage V_b = 72 V, and the rated output power P_o = 1 kW. A switching frequency of 85 kHz is selected based on the light-duty EV static wireless charging standard, SAEJ2954. SiC MOSFETs (SCT3060AL) are employed for S_1 and S_2 to enhance the system efficiency. The rated voltage of the switches is 650 V. The proposed design method to obtain ZVS and avoid bifurcation in Section 4.4 in Chapter 4 is utilized to design the prototype. The minimum value of the duty cycle D should be about 0.33 when the voltage V_{Ci} is limited to 70% of the rated device voltage. It is assumed that the overall system efficiency η is 0.9. The output capacitance across the switches ($C_{oss1} = C_{oss2} = C_{oss}$ = 600 pF) includes parasitic output capacitance of the switches (130 pF) and an external capacitor (470 pF). The addition of the external capacitors is to reduce the turn-off losses of the switches. The dead time t_d is 0.4 μs, the secondary quality factor Q_s is 4.4, and the coupling coefficient k is about 0.15. A programmable DC power electronic load (Chroma 63205A-1200-200) at constant voltage mode is utilized to emulate the battery voltage in the experimental verifications. Film capacitors are used to implement the compensation capacitors. They are arranged in array forms to obtain the required capacitance values, voltage and current ratings. A film capacitor (WCAP-FTXX-890334026020) is used for the clamping capacitor. The secondary rectifier is implemented using schottky diodes (APT100S20BG).

The inductive coils are fabricated in a planar circular geometry with 26 turns on the primary side and 6 turns on the secondary side. The outer diameters of the primary and secondary coils are 490 mm and 440 mm, respectively. The litz wire with 1050 strands of AWG 38 is used to fabricate both coils. The nominal air gap between primary and secondary coils is 170 mm, where the mutual inductance is 15 μH. The detailed prototype parameters are listed in Table 5.1. The calculation of these parameters is shown in Appendix B.

Moreover, the dynamic behavior of the designed charging system is investigated, and a digital controller for charging current regulation is developed based on the derived small-signal model. The SmartFusion FPGA, A2F200M3F, is utilized to implement the close-loop control and generate PWM signals driving the inverter.

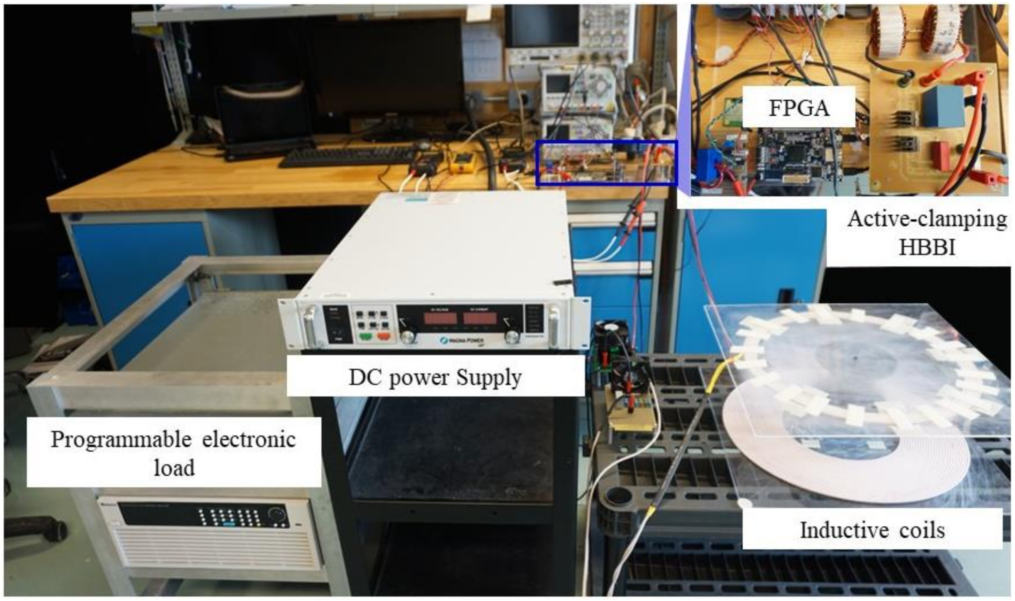


Figure 5.1: Experimental setup.

Table 5.1: IPT charging system specifications

Parameter	**Symbol**	**Value**	**Unit**
Maximum output power	P_o	1	kW
Battery voltage	V_b	72	V
Input voltage	V_i	150	V
Switching frequency	f_s	85	kHz
Maximum input current ripple	ΔI_{Li}	1	A
Peak device voltage	$V_{ds}(max)$	650	V
Output capacitance of switch	C_{oss}	600	pF
Dead time	t_d	0.4	μs
Primary self-inductance	L_p	298	μH
Secondary self-inductance	L_s	35	μH
Mutual inductance	M	15	μH
Primary compensation capacitor	C_p	12.9	nF
Secondary compensation capacitor	C_s	100.2	nF
Boost inductor	L_i	1.36	mH
Clamping capacitor	C_i	0.68	μF
Output capacitor	C_o	520	μF

5.2 Verification of Small-Signal Model

Various control-to-output transfer functions can be derived from the small-signal model presented in Section 4.3.5. Based on the transfer functions, close-loop controllers can be designed to regulate. i.e., the input current, output current and output voltage. In the battery charging applications, the output current and output voltage should be controlled. In this chapter, the fixed-frequency PWM control scheme is employed, thus the duty cycle-to-output current transfer function, $G_{id}(s)$, and duty cycle-to-output voltage transfer function, $G_{vd}(s)$ should be derived. In order to verify the accuracy of the derived transfer functions, their Bode plots are compared with the circuit-based AC-sweep results by using PSIM software. Figure 5.2 and 5.3 illustrate the Bode plots for $G_{io\_d}(s)$ and $G_{vo\_d}(s)$ at D = 0.34 and V_b = 72 V. It can be observed that the AC-sweep results follow closely the Bode plots of the transfer functions. The –180-degree phase angle of $G_{io\_d}(s)$ and $G_{vo\_d}(s)$ at low frequencies indicates that the output current and the output voltage are inversely proportional to the duty cycle.

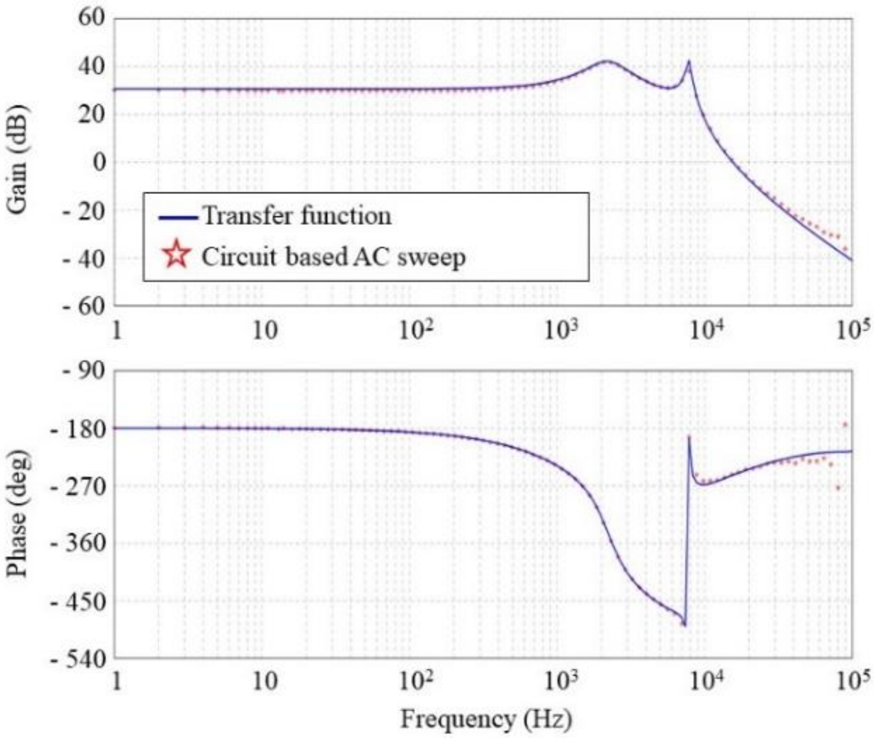


Figure 5.2: Bode plots at D = 0.34 and V_b = 72 V (Simulation results). (a) Duty cycle–to–output current. (b) Duty cycle–to–output voltage.

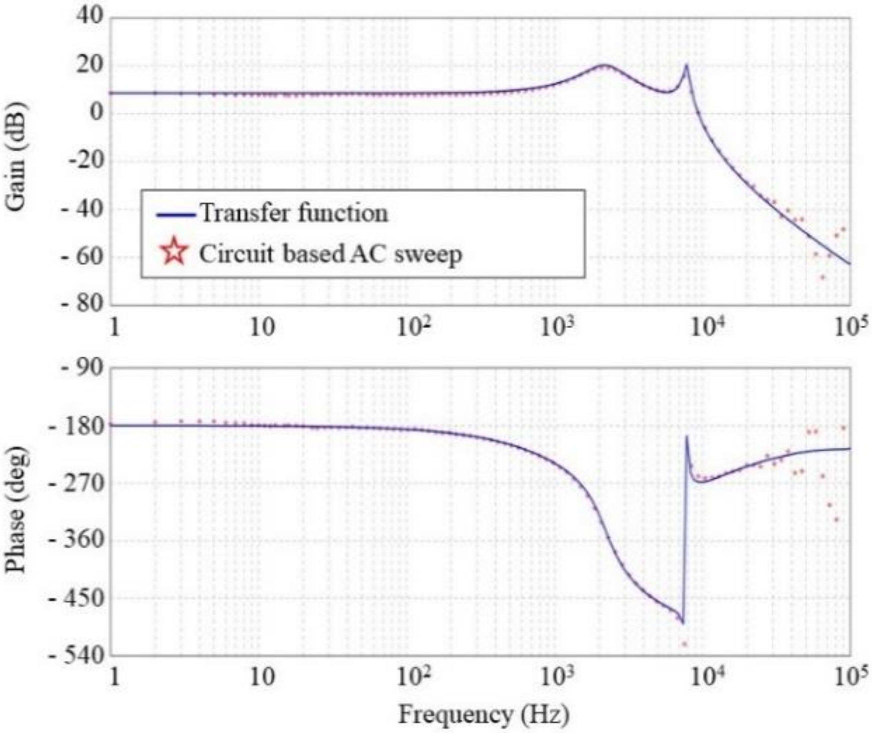


Figure 5.3: Bode plots at $D = 0.34$ and $V_b = 72$ V (Simulation results). (a) Duty cycle–to–output current. (b) Duty cycle–to–output voltage.

5.3 Output Current Controller Design

In the EV applications, the constant-current constant-voltage (CC-CV) charging technique, where both battery current and voltage are controlled, is widely employed [151-153]. Another charging method, namely multi-step constant-current (MCC), was proposed in [154, 155]. Note that, the output voltage controller is not necessary in the MCC method. Instead of that, the magnitude of the charging current in each step is controlled to optimize the charging process. As a result of that, accurately controlling the battery current is essential in this charging technique.

The derived small-signal model in Chapter 4 is used to design a controller regulating the output current. Figure 5.4 shows the block diagram of the current control loop, where K_{PWM} = 1/400 is a PWM gain, K_C = 0.06 is a current sensing gain, and K_{ADC} = 1024/2.56 is a 10-bit analog-to-digital converter gain. As the output current is inversely proportional to the duty cycle, a gain –1 is added in the loop. Since the controller and PWM modulator are digitally implemented on the FPGA platform with the uniform single sampling and single duty update mode as shown in Figure 5.5, a time delay, $1.5T_s$, including the computational delay and the PWM modulator delay is added in the loop [156].

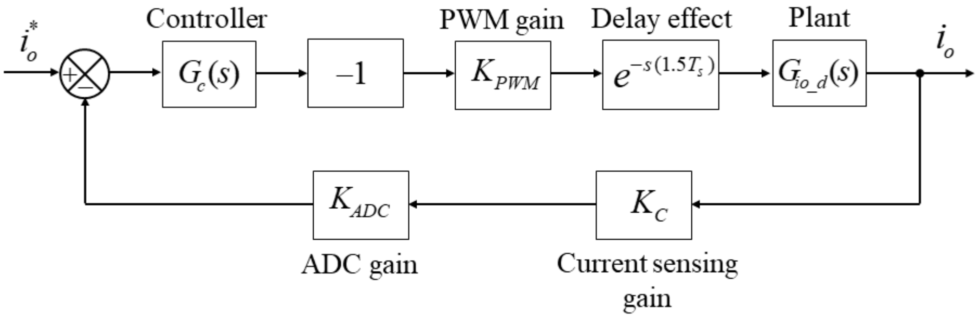


Figure 5.4: Block diagram of the current control loop.

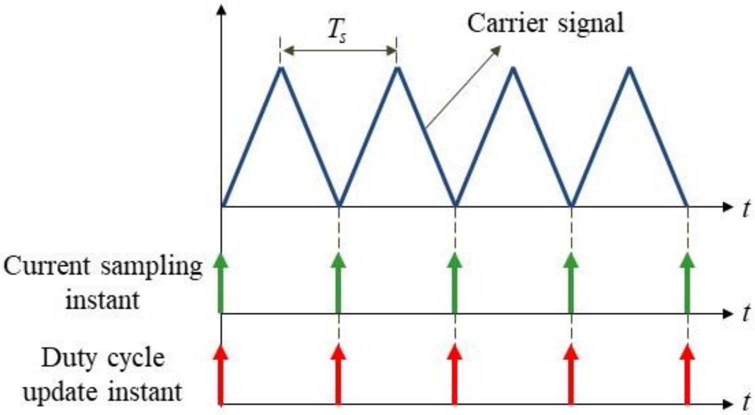


Figure 5.5: Timing diagram of current sampling and duty cycle update.

Dominant pole compensation method is used to design the current controller with two objectives: 1) The loop gain at DC and low frequency is as high as possible to minimize steady-state error, 2) The loop gain at the dominant pole should be less than or equal to 0 dB to ensure a positive phase margin, in turn stability. For those purposes, an integral controller given by (5.1) is employed. The integral controller can help to eliminate the steady-state error.

$$G_c(s) = \frac{830}{s} \tag{5.1}$$

Figure 5.6 shows the Bode plot of the loop gain at the nominal condition (V_i = 150 V, V_b = 72 V and I_o = 14 A). The crossover frequency (f_c) is 300 Hz, the phase margin (PM) is 68^o, the DC gain is infinite, and the gain of the dominant pole at 2000 Hz is – 6 dB.

Once the continuous time controller has been designed, a discretization method is used to transform the controller into the *z* domain. By using the backward Euler method with the sampling frequency equaling to the switching frequency, the discretized controller is given

$$G_c(z) = \frac{0.00976}{1 - z^{-1}} \tag{5.2}$$

The differential algorithm for the digital integral controller is given by

$$u[k] = 0.00976e[k] + u[k-1] \tag{5.3}$$

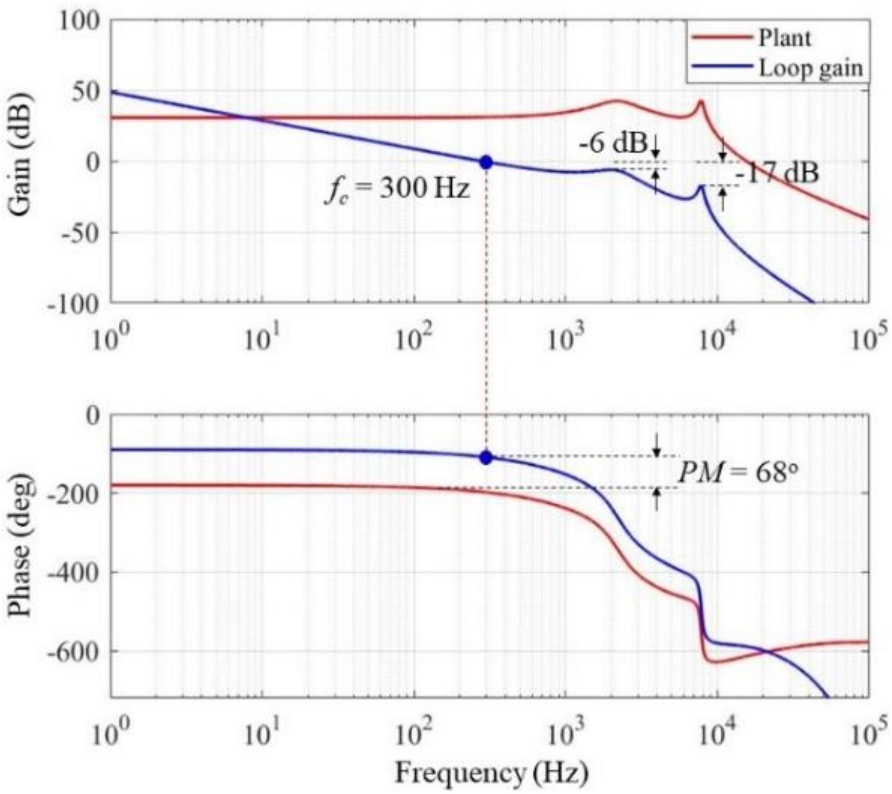


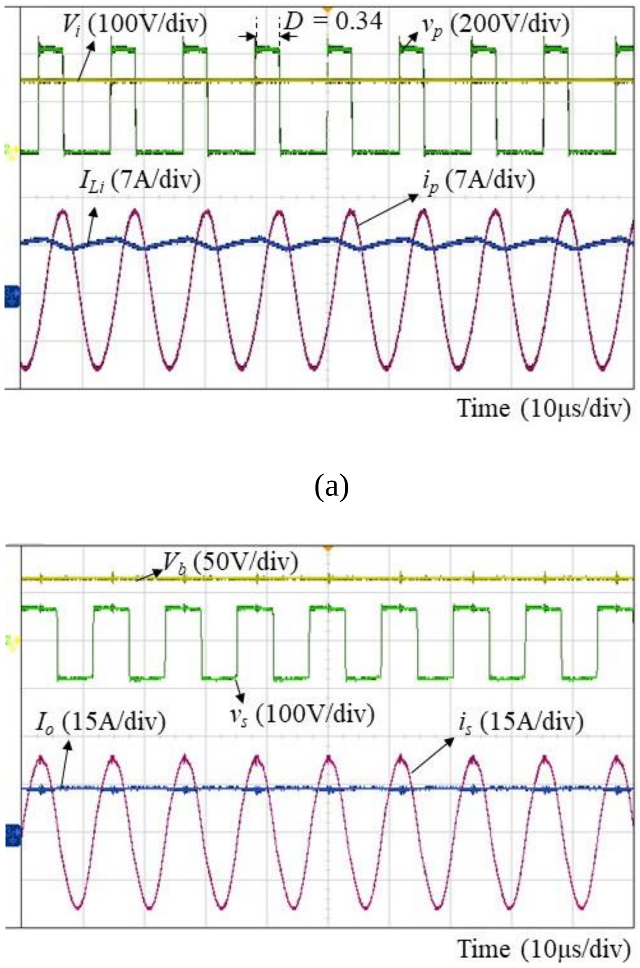
Figure 5.6: Bode plots of the current control loop.

where $e[k]$ is the error between the command and the feedback signal at the sampling instant kth, $u[k]$ and $u[k-1]$ are the outputs of the controller at the sampling instant kth and $(k-1)$th, respectively.

5.4. Verifications and Discussions

5.4.1 Current controller performance

Figure 5.7 shows the steady-state current and voltage waveforms at the input, output, primary and secondary coils when the system is operating at the nominal condition. It can be seen that the output current contains no steady-state error, the converter duty cycle maintains about 0.34, and the input current ripple is 0.9 A. The designed inverter and



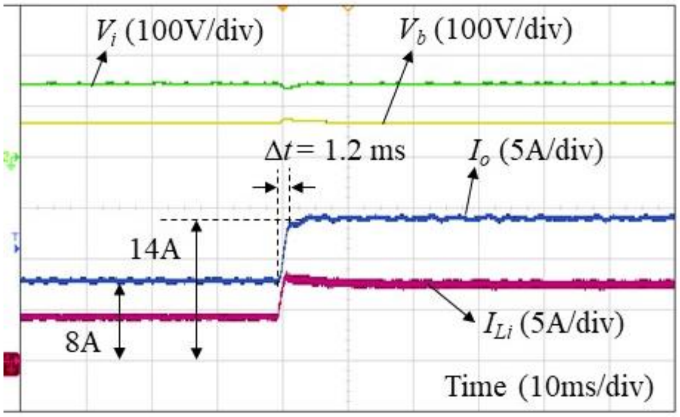
(a)

(b)

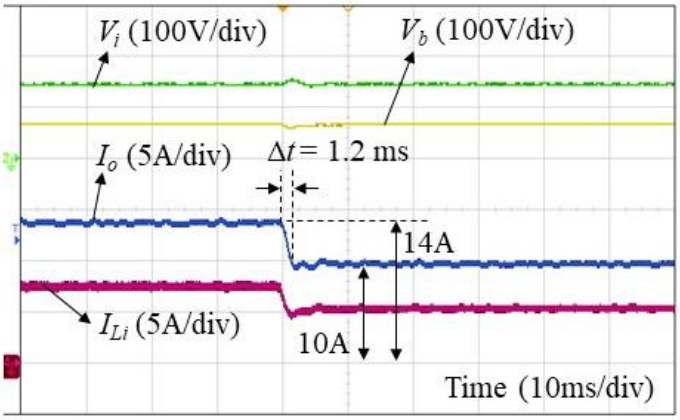
Figure 5.7: Steady-state waveforms at V_i = 150 V, V_b = 72 V and I_o = 14 A (Experimental results). (a) Input voltage, input current, primary voltage and primary current. (b) Battery voltage, battery current, secondary voltage and secondary current.

controller meet the demands of the output current steady-state error, the minimum duty cycle, and the input current ripple.

Figure 5.8 shows the step response of the converter when the output battery voltage maintains 72 V, and the current command changes from 8 A to 14 A and from 14 A to 10



(a)

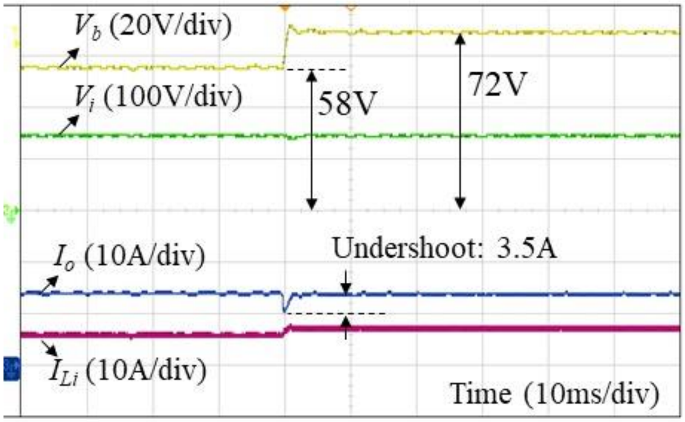


(b)

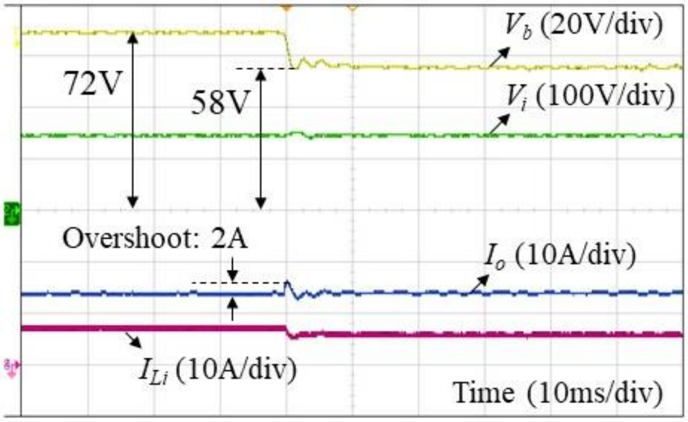
Figure 5.8: Dynamic response with reference current step change (Experiment results). (a) From 8 A to 14 A. (b) From 14 A to 10 A.

A. It is observed that the system retains stability with nearly no overshoot or undershoot, and the rising time and falling time are about 1.2 ms.

Figure 5.9 shows the dynamic response of the converter when the output current command maintains 14A, and the output battery voltage steps from 58 V to 72 V, and *vice versa*. Although the output battery voltage suddenly increases or decreases, the system stability is always obtained, and the output current undershoot and overshoot are 3.5 A and



(a)



(b)

Figure 5.9: Dynamic response with battery voltage step change (Experiment results). (a) From 58 V to 72 V. (b) From 72 V to 58 V.

2 A, respectively. It can be said that the step change of the battery voltage is unrealistic in the charging applications. However, experimental waveforms under the output battery voltage step changes are showed to validate the dynamic performance of the current controller at the worst scenarios.

In order to correctly emulate the battery behavior during the charging process, the experimental waveforms under the linear increase of the battery voltage are shown in Figure 5.10. Figure 5.10 illustrates the ramp response of the system when the output battery

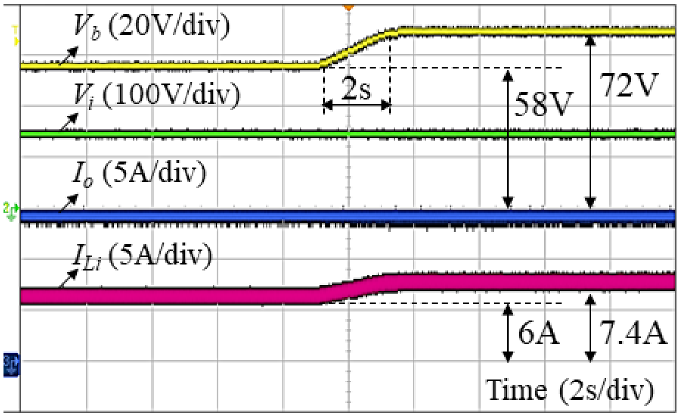
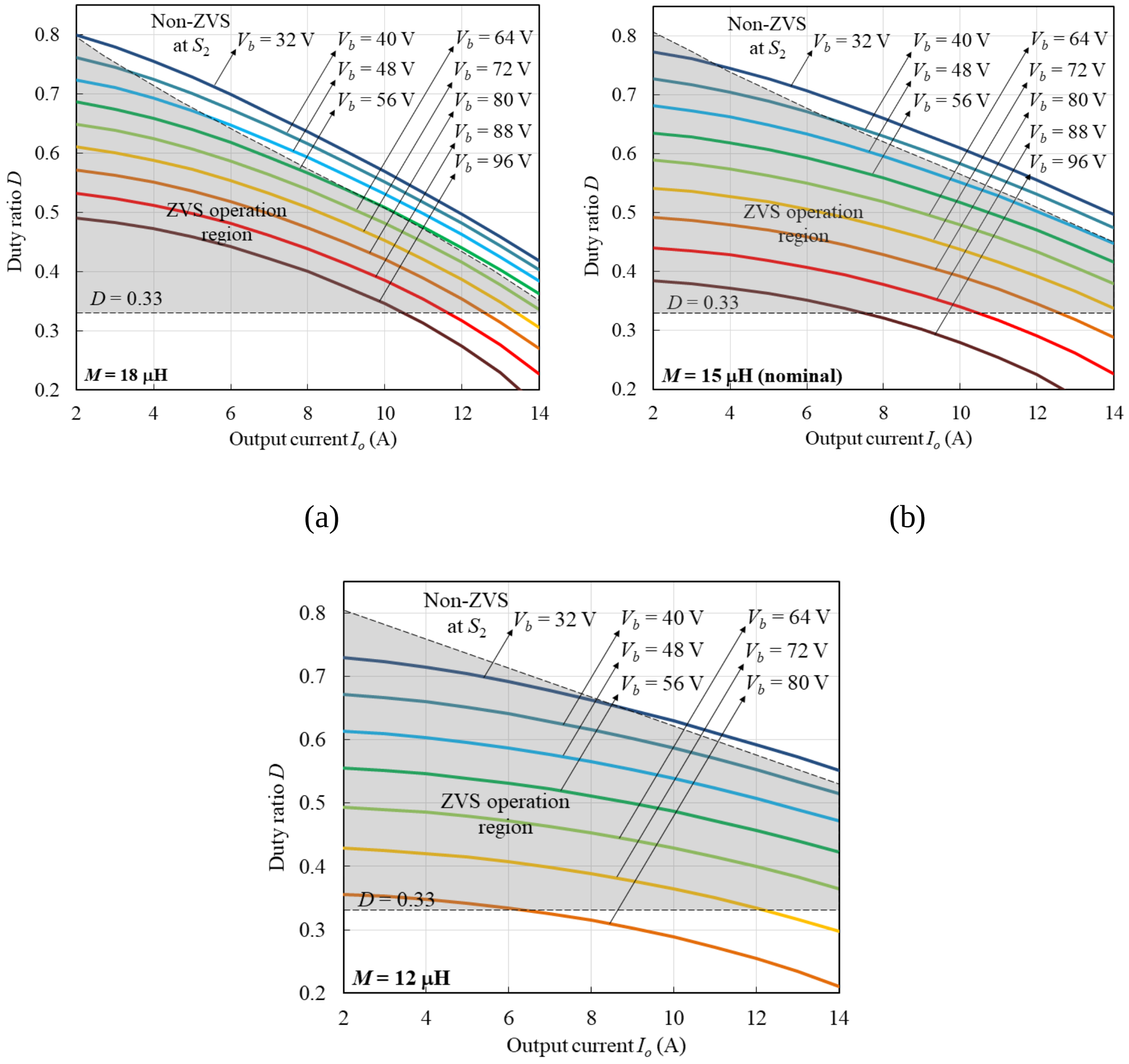


Figure 5.10: Dynamic response with battery voltage linear increase from 58 V to 72V at I_o = 14 A (Experiment results).

voltage linearly increases from 58 V to 72 V with a rising time of 2 s, and the command output current maintains 14 A. Again, the system stability is obtained.

5.4.2 ZVS verification

The ZVS operation of the designed system under the variation of the mutual inductance is depicted in Figure 5.11. It can be seen that the ZVS operation areas (shaded areas) are restricted by the minimum duty cycle and the ZVS conditions of the lower switch S_2. The ZVS for S_2 is more difficult to achieve at the low battery voltages and the high output currents. The switch S_2 loses ZVS at the low battery voltages when the mutual inductance increases. At the low mutual inductance, the ZVS operation area of S_2 is extended to the low battery voltages. It is noted that the maximum output current at the nominal battery voltage, V_b = 72 V, is reduced by the limited duty ratio when the mutual inductance differs from the nominal value, M = 15 μH. Figure 5.12, 5.13 and 5.14 shows the experimental waveforms to verify the ZVS operation of the inverter at the different values of mutual inductance, output current and battery voltage. It can be seen that the drain-to-source voltages v_{ds1} and v_{ds2} of S_1 and S_2 always reach to zero before their driving signals v_{gs1} and v_{gs2} are activated. It means that ZVS is maintained for both the switches.

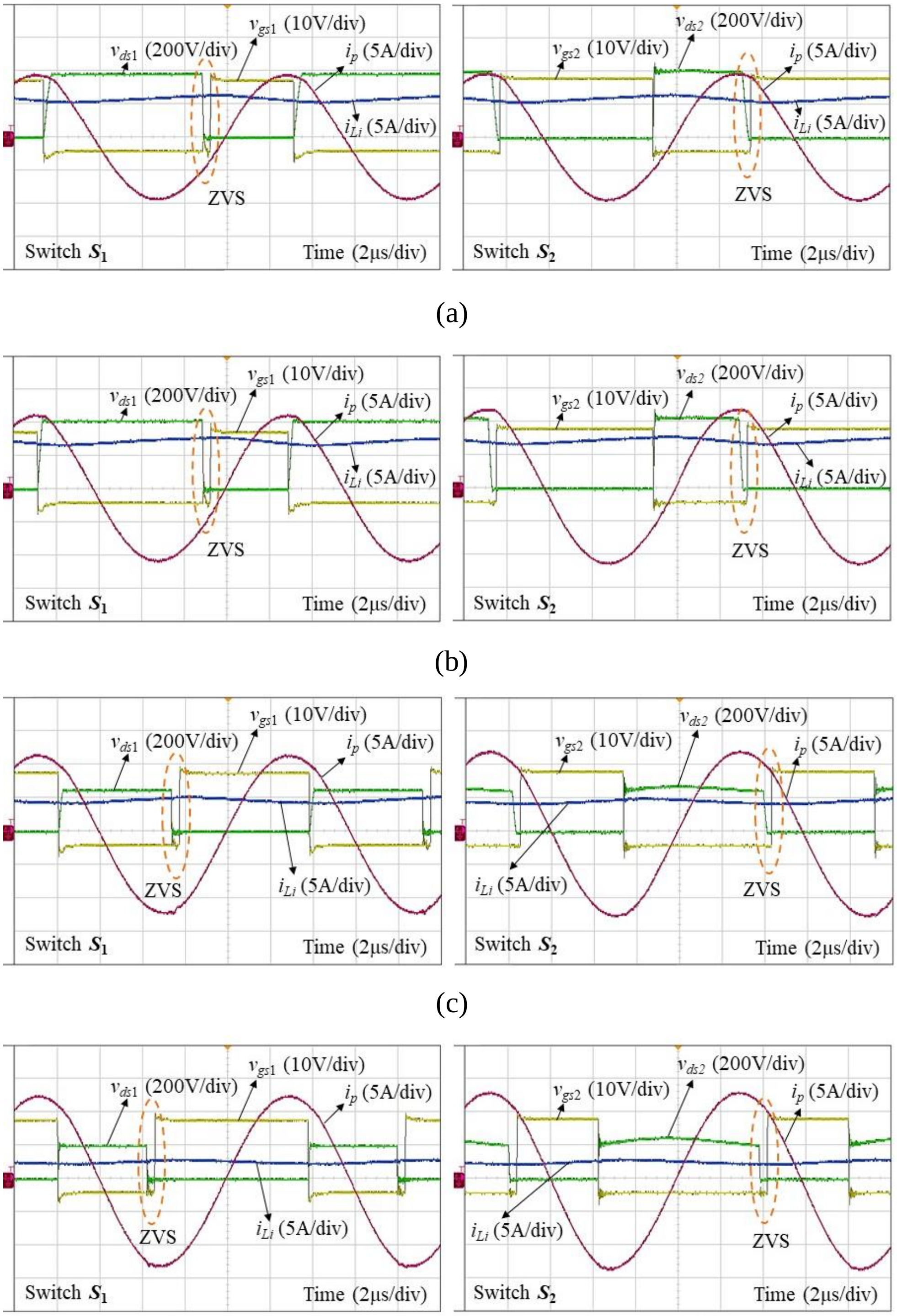


(a)

(b)

(c)

Figure 5.11: ZVS operation region of the converter with different mutual inductance (Calculation results). (a) M = 18 µH. (b) M = 15 µH. (c) M = 12 µH.



(a)

(b)

(c)

(d)

Figure 5.12: Experimental waveforms validating the ZVS operation of the inverter at nominal mutual inductance M = 15 μH. (a) V_b = 58 V and I_o = 14 A. (b) V_b = 72 V and I_o = 14 A. (c) V_b = 80 V and I_o = 8 A. (d) V_b = 88 V and I_o = 4 A.

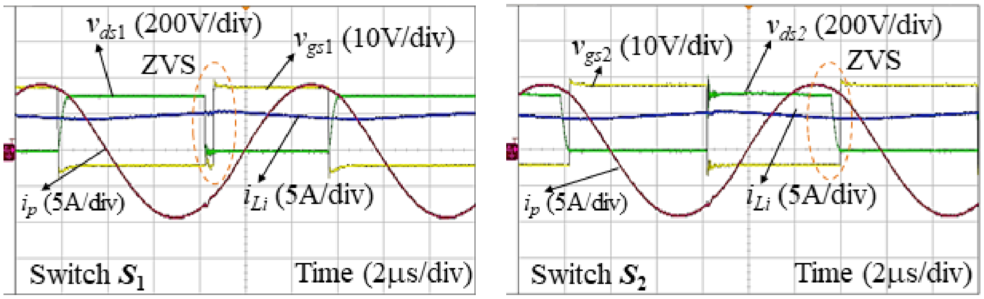


Figure 5.13: Experimental waveforms validating the ZVS operation of the inverter at M = 12 μH, V_b = 46 V, and I_o = 14. A.

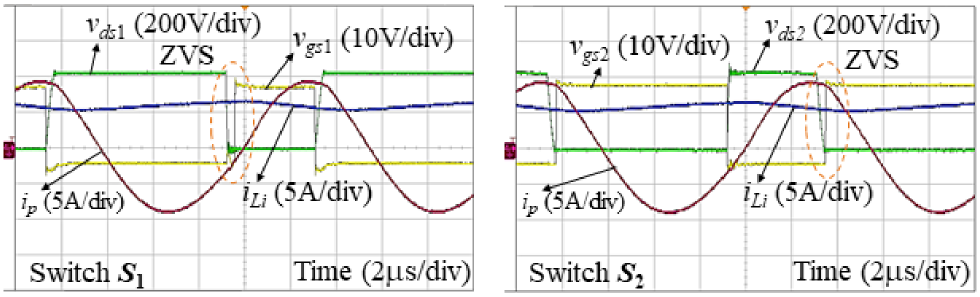


Figure 5.14: Experimental waveforms validating the ZVS operation of the inverter at M = 18 μH, V_b = 64 V and I_o = 14 A.

It is harder to achieve ZVS for S_2 at the low battery voltage and high output current conditions since a small difference between i_p and i_{Li} makes completely charging and discharging C_{oss1} and C_{oss2} more difficult, as shown in Figure 5.12 (a). On the other hand, the large difference between i_p and i_{Li} facilitates ZVS for the upper switch S_1.

The ZVS area extension of S_2 when the mutual inductance decreases is demonstrated in Figure 5.13 and 5.14. The minimum battery voltage to obtain ZVS for S_2 at M = 12 μH (the air gap of 190 mm) is as low as 46 V, whereas it is 64 V at M = 18 μH (the air gap of 150 mm). These values are in a good agreement with the depiction in Figure 5.11.

5.4.3 Clamping voltage variation

The average voltage and voltage ripple across the clamping capacitor at different charging currents are depicted in Figure 5.15. Note that, the battery voltage and mutual inductance are kept at their nominal values. Theoretical calculation from (4.42) and (4.70) and experimental measurement are in a reasonably good agreement. It can be seen that the voltage ripple increases with the output current decrease due to a large difference between i_{Li} and i_p causing a rise in the charging and discharging currents on the clamping capacitor. At I_o = 2 A, the voltage ripple is 39 V, which is 15% of the average voltage.

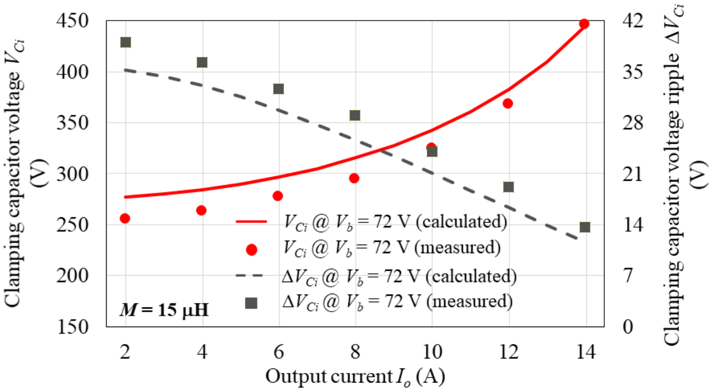


Figure 5.15: Average voltage and voltage ripple across clamping capacitor (Calculation and experimental results).

5.4.4 System efficiency

The overall system (DC-to-DC) efficiency was measured at different operating points to verify the performance of the designed charging system. The efficiency curves of the designed system at the nominal battery voltage, V_b = 72V, at three different mutual inductance values are depicted in Figure 5.16. It is clear that the efficiency is reduced when the mutual inductance decreases. This is because a higher primary current which is required to transfer the same power level at the lower mutual inductance causes more losses on the

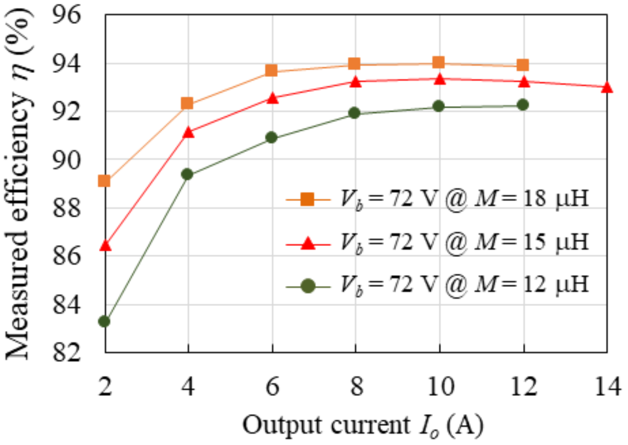


Figure 5.16: Measured efficiency curves of the designed system at different mutual inductance values (Experimental results).

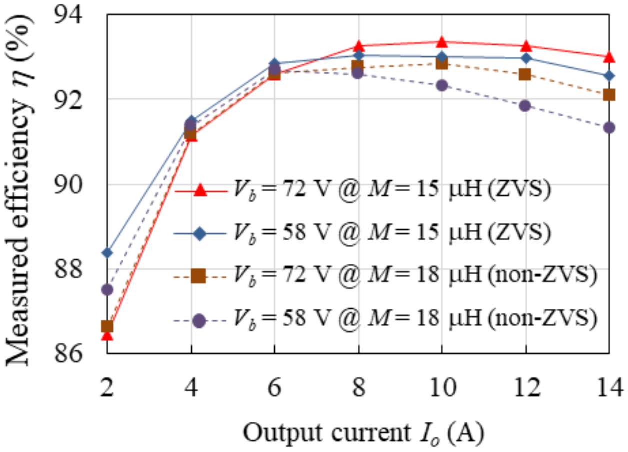


Figure 5.17: Measured efficiency curves of ZVS-designed and non-ZVS-designed systems (Experimental results).

primary coil, compensation capacitor, and switching devices. At M = 15 µH, a peak efficiency of 93.4% is achieved at I_o = 10 A while an efficiency of 93% is measured at the nominal output current, I_o = 14 A.

An efficiency comparison between the charging systems with ZVS and non-ZVS design is shown in Figure 5.17. For the non-ZVS system, it is designed with I_{pc} = 0, at which the mutual inductance is 18 μH and the primary circuit is tuned at the switching frequency (C_p = 11.7 nF). Note that, the mutual inductance is increased by reducing the air gap between the primary and secondary coils. It can be observed that the ZVS-designed system is more efficient than the counterpart at different battery voltage levels. Especially, it has a noticeable improvement at the high output current conditions (1.1 %). Table 5.2 shows a comparison between the proposed active-clamped HBBI based SS-IPT system and various IPT systems in literature. It is clear that the proposed IPT system demonstrates a higher or comparable efficiency compared to the other systems at similar power levels.

Table 5.2: Comparison of various IPT systems

Ref.	Inverter/Switching devices	Rectifier	Coil shape	Air gap (mm)	Coupling coefficient	Control scheme	Switching frequency (kHz)	Power (kW)	Peak efficiency (%)	Soft switching
[157]	HB CSI/ SiC MOSFET	HB diode rectifier	Circular	N/A	0.2	Variable frequency	46-50	1.2	92	ZCS
[158]	FB CSI/ SiC MOSFET	HB diode rectifier	Circular	250	0.22	Fixed frequency	50	1.6	91.5	ZCS
[159]	HB VSI/ GaN	FB diode rectifier	Circular	50	0.36	Variable frequency	85-150	0.7	92.3	ZVS
[152]	FB VSI/ Si MOSFET	FB diode rectifier	Circular	200	0.2	Fixed frequency	85	1.0	92.3	ZVS
[160]	FB VSI/ SiC MOSFET	FB diode rectifier	Circular	150	0.25	Fixed frequency	89	2.0	92.65	No
[161]	FB VSI/ SiC MOSFET	FB diode rectifier	Circular	150	0.18	Fixed frequency	93.5	1.4	94	ZVS
Proposed	HHBI/ SiC MOSFET	FB diode rectifier	Circular	170	0.15	Fixed frequency	85	1.0	93.4	ZVS

5.4.5 Loss distribution

The power losses of the switching devices and passive components are simulated and analyzed using the thermal modules in PSIM simulation. The detailed loss distribution of the designed charging system is shown in Figure 5.18. It can be observed that the rectifier conduction losses and the coil losses dominate the total system losses at the high output current conditions. As S_1 and S_2 are operated in ZVS, their switching losses are well mitigated. The conduction losses of S_2 is much higher than that of S_1 when the output current is high. It can be explained that S_2 carries both i_p and i_{Li} during the large interval of the mode 5 described in Section 4.2, Chapter 4. On the other hand, the conduction losses of S_1 exhibits a high profile at the low output current due to the larger duty cycle D. There is a deviation between the simulated efficiencies and measured efficiencies, especially at the high output currents (1.2 %). The deviation might be caused by ignoring inductor core losses, and PCB copper losses in the simulation.

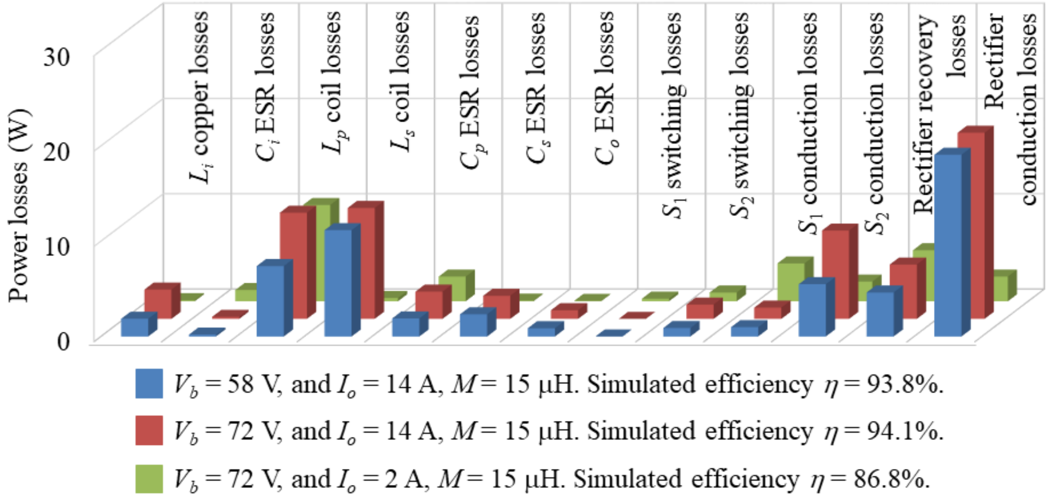


Figure 5.18: Loss distribution of the designed system at different battery voltages and output currents (Simulation results).

5.5 Summary

In this chapter, a 1.0-kW active-clamped HBBI based IPT charging prototype with the charging current controller was designed and implemented to validate the accuracy of the theoretical analyses in Chapter 4. The simulation and experimental results demonstrated the accuracy and the feasibility of the small-signal model and ZVS design approach proposed in Chapter 4. The derived small-signal model was used to investigate system dynamic response and to design the charging current controller. The developed controller was realized on an FPGA (A2F200M3F). It can be seen that the charging current was effectively controlled with fast response and no steady-state errors, and the inverter was operated with ZVS over a wide range of the charging current and the battery voltage. The ZVS operation boundary of the inverter under the variation of the mutual inductance was also successfully investigated by the theoretical analysis and experimental results. An efficiency improvement of 1.1 % was achieved with the proposed ZVS design method compared to non-ZVS design method. Due to ZVS achievement, a maximum efficiency of 93.4% at the nominal coupling coefficient of 0.15 (an air gap of 170 mm) was recorded, which is comparable to other IPT systems at similar power levels in literature.

Chapter 6. Direct AC/AC Active-clamped Half-bridge Converter for Inductive Charging Applications

6.1 Introduction

Recently, the IPT charging systems powered through two power conversion stages (AC/DC/AC) have been widely used because the power converters can be separately controlled to optimize specific performance indices, e.g. input power factor correction and output power regulation. However, the presence of multiple conversion stages and a bulky DC-link capacitor increases the cost, size and weight of the system.

Alternatively, the MCs feeding the IPT systems enable direct conversion of low-frequency AC inputs (50-60 Hz) to high-frequency outputs (up to 85 kHz) without any intermediate conversion stage; they enhance the system performance in terms of power density, losses, and cost. The MC based IPT systems advantageously adopt the SRC charging technique and remove the intermediate DC-link capacitor. The major challenge of using MCs in the IPT charging systems is developing a control scheme for both power regulation and power factor correction. Recently, the buck-derived MC [96] and boost-derived MC [100] have been employed for IPT systems. Moreover, in [102], a single-stage topology integrating bridgeless boost PFC converter and FB VSI was proposed for IPT applications. The detailed description and comparison of the single-stage converters were presented in Chapter 2 and 3.

The main drawbacks of the single-stage conversion topologies are the requirements of many active switches and complex control schemes. To overcome those issues, a new direct AC/AC active-clamped HB converter feeding the IPT charging system is proposed in this chapter. The proposed converter eliminates the front-end rectifier and the electrolytic DC-link capacitor providing a single-stage power conversion and thus improves the system performance regarding efficiency, size, and weight. The output of the proposed converter is high-frequency voltage; therefore, the SS compensation network is utilized. Instead of diode-bridge rectifiers, an active rectifier is used on the battery side to further improve system efficiency and to avoid the discontinuous conduction phenomenon due to the nonlinear characteristic of the diode-bridge rectifiers. The SRC is adopted for the proposed IPT charging system.

6.2 Circuit Configuration of the Proposed Inductive Charging System

The IPT charging system fed by the proposed direct AC/AC active-clamped HB converter is shown in Figure 6.1. The proposed AC/AC converter is the integration of an AC/AC boost converter and HB matrix converter. Two bidirectional switches are employed to configure the AC/AC converter. Each bidirectional switch enabling conducting current and blocking voltage in both directions is formed by an anti-serial connection of two semiconductor switching devices (S_{p1a}/S_{p1b} or $S_{p2\mathrm{a}}/S_{p2b}$). In the proposed IPT system, input current correction and charging current regulation are realized by controlling the duty cycle of the primary AC/AC converter through two control loops. During the positive half cycle of the input voltage, switches S_{p1a} and S_{p2a} are switched complementarily at the switching frequency f_s, while S_{p1b} and S_{p2b} are permanently turned on. Conversely, in the negative half cycle of the input voltage, S_{p1a} and S_{p2a} are always kept conducting, while S_{p1b} and S_{p2b} are driven by complementary pulses at f_s. The duty cycle d_p of the AC/AC converter is defined as the ratio between the on-time of the upper switches S_{p1a}/S_{p1b} and the switching period. The output of the direct AC/AC active-clamped HB

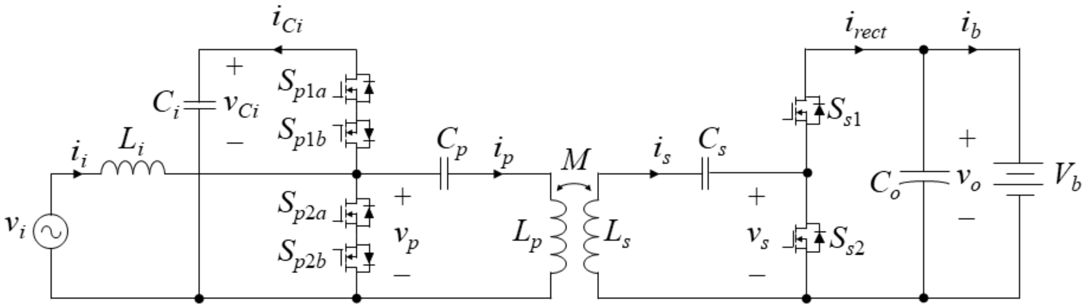


Figure 6.1: Proposed inductive charging system fed by the direct AC/AC active-clamped HB converter.

converter is a high-frequency unipolar-square-wave voltage (v_p), and its amplitude and polarity depend on the clamping voltage (v_{Ci}). As a result, a series compensation circuit is required in the primary side. Here, the SS compensation network is selected due to simplicity, cost-effectiveness, high efficiency, and load-independent compensation. In order to maximize the power transfer capability and minimize the VA rating of the converter, the primary and secondary resonant circuits are tuned to the switching frequency. An active HB rectifier is used on the secondary side circuit, and its switches, S_{s1} and S_{s2}, are operated at f_s with a fixed duty cycle of 0.5. As a result, the secondary voltage v_s is a positive unipolar square wave with duty cycle $d_s = 0.5$. In order to transfer power from the grid to the battery, the phase displacement θ between v_p and v_s must be maintained from 0 to π, which is explained in Section 6.4.

6.3 Operation Principles

Figure 6.2 and 6.3 illustrate the steady-state waveforms of the AC/AC active-clamped HB converter based IPT charging system in one switching cycle. In this section, only the operation modes during the positive half cycle of the input voltage are describe in detail. Similarly, the operation of the charging system during the negative half cycle of the input voltage can be investigated where S_{p1a} and S_{p2a} are always kept conducting, while S_{p1b} and S_{p2b} are driven PWM signals. Note that, during the negative half line cycle voltage, the clamping voltage (v_{Ci}) is negative, resulting in a negative unipolar-square-wave primary voltage (v_p). Therefore, v_p must be shifted 180^0 to remain a fixed phase displacement (θ) between v_p and v_s during the negative half line cycle voltage, as shown in Figure 6.3. During the positive half line cycle, ten operation modes can be categorized based on primary/secondary current directions, and the switching state of the primary AC/AC converter and the secondary rectifier in one switching cycle, as shown in Figure 6.4.

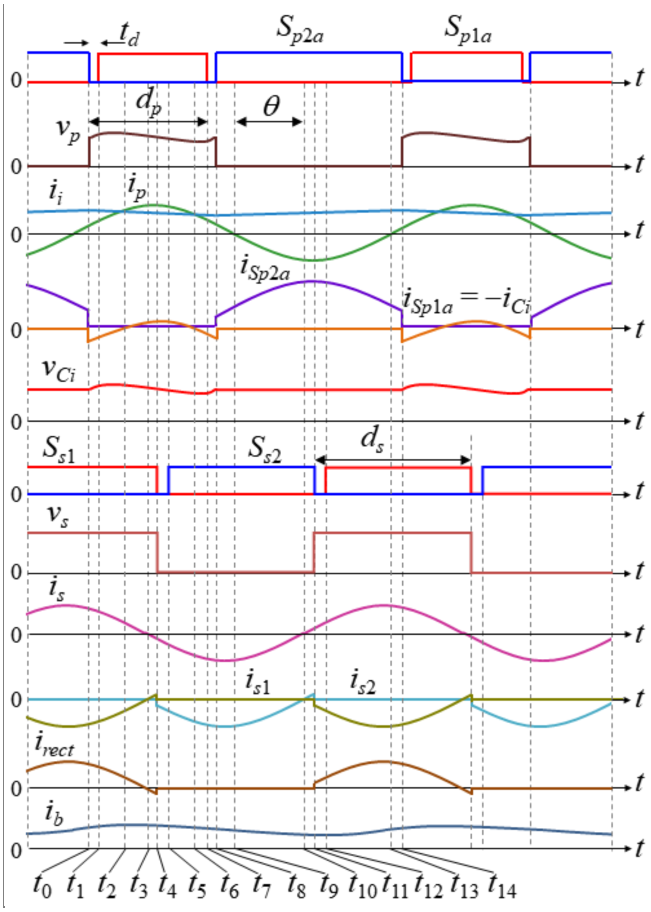


Figure 6.2: One-switching-cycle steady-state operating waveforms of the proposed inductive charging system at $v_i > 0$

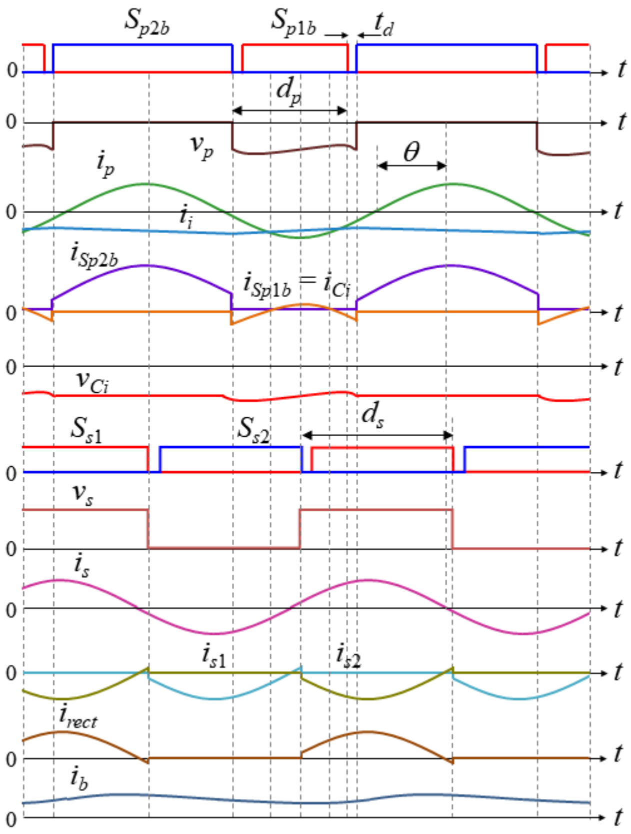


Figure 6.3: One-switching-cycle steady-state operating waveforms of the proposed inductive charging system at $v_i < 0$

Mode 1 ($t_0 - t_1 - t_2$): As soon as S_{p2a} is deactivated at $t = t_0$, the body diode of S_{p1a} starts conducting a current equal $i_i - i_p$. Thus S_{p2a} suffers from hard turn off. After a dead time, at $t = t_1$, S_{p1a} is activated with zero-voltage switching (ZVS) because its body diode has been conducting. During this mode, the input inductor L_i releases its energy through the resonant tank and the clamping capacitor C_i. As a result, the input current i_i starts decreasing whereas the clamping voltage v_{Ci} starts increasing. The secondary current i_s flows to the load through S_{s1} in this mode. This mode is completed at $t = t_2$ when i_i is equal to i_p.

Mode 2 (t_2 – t_3): This mode begins with $i_p > i_i$. The current flowing through S_{p1a} reverses its direction. During this mode, the input inductor L_i and the clamping capacitor C_i release energy into the resonant tank. Therefore, the input current i_i and the clamping voltage v_{Ci} decrease. The secondary current i_s keeps flowing to the load through S_{s1} in this mode. This mode is completed when i_s reaches zero at $t = t_3$.

Mode 3 (t_3 – t_4): This mode begins with $i_s < 0$. The current flowing through S_{s1} reverses its direction. During this mode, the input inductor L_i and the clamping C_i keep releasing energy into the resonant tank.

Mode 4 (t_4 – t_5 – t_6): As soon as S_{s1} is deactivated at $t = t_4$, the body diode of S_{s2} starts conducting the secondary current i_s. Thus S_{s1} suffers from hard turn off. After a dead time, at $t = t_5$, S_{s2} is activated with ZVS because its body diode has been conducting. In this mode, the state of the AC/AC converter is unchanged. This mode is completed at $t = t_6$ when i_p is equal to i_i.

Mode 5 (t_6 – t_7 – t_8): This mode begins with $i_p < i_i$. The current flowing through S_{p1a} reverses its direction. At $t = t_7$, S_{p1a} is deactivated with ZVS because its body diode is still conducting. In this mode, the input inductor L_i releases its energy through the resonant tank and the clamping capacitor C_i. Therefore, the input current i_i keeps decreasing, but the clamping voltage v_{Ci} starts increasing. The secondary current i_s keeps circulating through S_{s2} during this mode. This mode finishes when S_{p2a} is turned on.

Mode 6 (t_8 – t_9): As soon as S_{p2a} is activated at $t = t_8$, a current equal $i_i - i_p$ commutates instantaneously to it. Therefore, S_{p2a} suffers hard turn on. The input current i_i is shared through the resonant tank and S_{p2a} to charge the input inductor L_i, and it starts linearly rising. During this mode, the state of the secondary rectifier is unchanged. This mode is completed when the direction of i_p is reversed at $t = t_9$.

Mode 7 ($t_9 – t_{10}$): This mode begins with $i_p < 0$, and S_{p2a} carries both i_p and i_i. The input inductor L_i keep being charged. During this mode, the state of the secondary rectifier is unchanged. This mode is completed when i_s reaches zero.

Mode 8 ($t_{10} – t_{11}$): This mode begins with $i_s > 0$. The current flowing through S_{s2} reverses its direction. In this mode, the state of the AC/AC converter is unchanged. This mode finishes when S_{s2} is turned off.

Mode 9 ($t_{11} – t_{12} – t_{13}$): As soon as S_{s2} is deactivated, the body diode of S_{s1} starts conducting the secondary current i_s to deliver power to the load. As a result, S_{s2} suffers from hard turn off. After a dead time, at $t = t_{12}$, S_{s1} is activated with ZVS because its body diode has been conducting. This mode is completed when the direction of i_p is reversed.

Mode 10 ($t_{13} – t_{14}$): This mode begins with $i_p > 0$. During this mode, S_{p2a} carries a current equal $i_i – i_p$ only. The input inductor L_i keep being charged until S_{p2a} is deactivated at $t = t_{14}$, and the circuit state returns to mode 1 to restart a new cycle.

It can be seen that S_{p1a} achieves both zero-voltage turn on and turn off whereas S_{p2a} suffers hard turn on and hard turn off during the positive half line cycle. Similarly, during the negative half line cycle, both zero-voltage turn on and turn off are obtained for S_{p1b} whereas S_{p2b} experiences hard turn on and turn off. The secondary rectifier is operated with ZVS in both half line cycles.

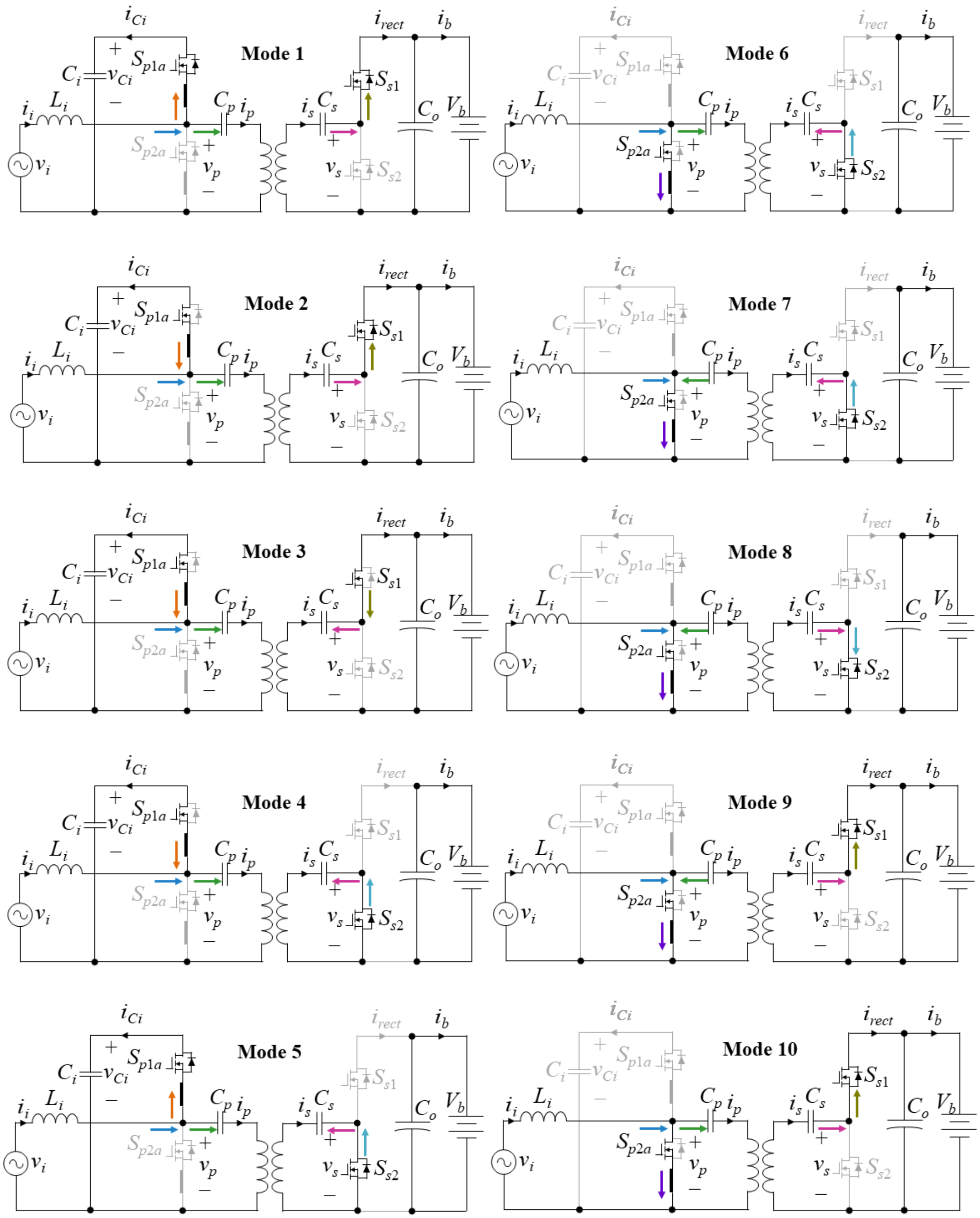


Figure 6.4: Operation modes of the proposed inductive charging system in one switching cycle at $v_i > 0$.

6.4 Mathematical Steady-state Model

In this section, the steady-state model of the proposed charging system is derived. For the analysis of SS compensated IPT systems, the fundamental harmonic model is widely used, and it is adopted to analyse the proposed charging system with some assumptions as follows:

1) The switching frequency is much higher than the line frequency, the input voltage v_i can be considered as constant over a switching period;

2) All switches and diodes are ideal;

3) The dead time is neglected;

4) Parasitic resistances of inductors, capacitors and coils are ignorable;

5) Boost inductor L_i is sufficiently large to maintain a constant low-ripple input current over a switching period;

6) Clamping capacitor C_i is sufficiently large to maintain constant clamping voltage over a switching period;

7) Primary and secondary currents (i_p and i_s) are nearly sinusoidal.

Here, the steady-state analysis is realized in the positive half line cycle. A similar analysis can be done for the negative half line cycle. Figure 6.5 shows the equivalent circuit of the proposed IPT charging system.

In order to maximize the power transfer capability and minimize the VA rating of the converters, the primary and secondary resonant circuits are tuned to the switching frequency.

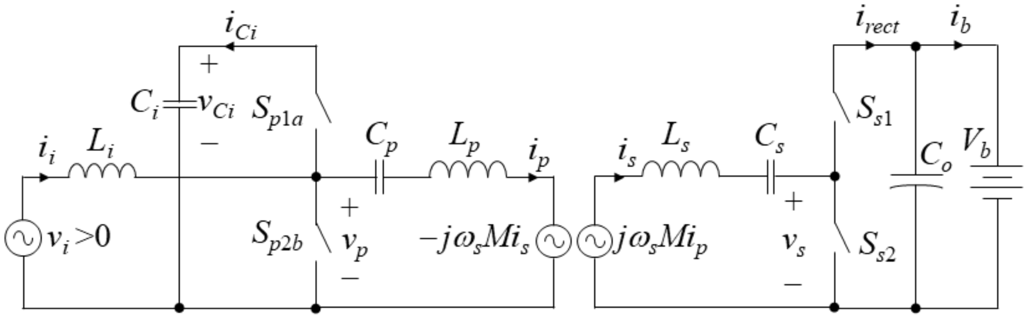


Figure 6.5: Equivalent circuit of the charging system.

$$\omega_s = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{6.1}$$

where L_p and L_s are the primary and secondary self-inductances, C_p and C_s are the primary and secondary compensation capacitances, and $\omega_s = 2\pi f_s$ is the switching angular frequency.

The primary and secondary voltage, v_p and v_s, are unipolar square waves, and they can be approximated to their fundamental components

$$v_p(t) = \frac{2v_{Ci}\sin \pi d_p}{\pi} \sin \omega_s t \tag{6.2}$$

$$v_s\left(t\right) = \frac{2V_b \sin \pi d_s}{\pi} \sin\left(\omega_s t + \theta\right) \tag{6.3}$$

where V_b is the battery voltage, d_p and d_s are the duty cycles of the primary AC/AC converter and secondary rectifier, and θ is the initial phase of the secondary voltage.

As derived in Section 4.3.4, the clamping voltage in steady state is given as

$$v_{Ci} = \frac{v_i}{d_p} \tag{6.4}$$

Substitution of (6.4) in (6.2) results in

$$v_p(t) = \frac{2v_i \sin \pi d_p}{\pi d_p} \sin \omega_s t \tag{6.5}$$

The primary and secondary voltages can be represented in the phasor domain as follows

$$\dot{V}_p = \frac{2v_i \sin \pi d_p}{\pi d_p} \tag{6.6}$$

$$\dot{V}_s = \frac{2V_b \sin \pi d_s}{\pi} \angle \theta \tag{6.7}$$

As both the primary and secondary circuits are turned to the switching frequency, the primary and secondary currents in the phasor domain can be derived as

$$\dot{I}_p = \frac{\dot{V}_s}{j\omega_s M} = \frac{2V_b \sin \pi d_s}{\pi \omega_s M} \angle \left(\theta - \pi/2\right) \tag{6.8}$$

$$\dot{I}_s = \frac{\dot{V}_p}{-j\omega_s M} = \frac{2v_i \sin \pi d_p}{\pi d_p \omega_s M} \angle \pi/2 \tag{6.9}$$

And their time-domain expressions are given as

$$\begin{aligned} i_p(t) &= \frac{2V_b \sin \pi d_s}{\pi \omega_s M} \sin\left(\omega_s t + \theta - \pi/2\right) \\ &= I_{ps} \sin \omega_s t + I_{pc} \cos \omega_s t \end{aligned} \tag{6.10}$$

$$i_s(t) = \frac{2v_i \sin \pi d_p}{\pi d_p \omega_s M} \sin\left(\omega_s t + \pi/2\right) \tag{6.11}$$

where $I_{ps} = \frac{2V_b \sin \pi d_s \sin \theta}{\pi \omega_s M}$, and $I_{pc} = -\frac{2V_b \sin \pi d_s \cos \theta}{\pi \omega_s M}$ are the peaks of the sine and cosine components in the primary current.

According to the analysis in Section 4.3.4, the input current is given as

$$i_i(t) = I_{ps} \frac{\sin \pi d_p}{\pi d_p} = \frac{2V_b \sin \pi d_s \sin \theta}{\pi \omega_s M} \frac{\sin \pi d_p}{\pi d_p} \tag{6.12}$$

It can be seen that the input current i_i(t) can be controlled by primary/secondary duty cycles, and the phase displacement θ. In order to transfer power from the grid to the battery, the input current i_i(t) must be positive during the positive half line cycle, thus the phase displacement θ must be maintained from 0 to π. Here, the input current is controlled by varying d_p while θ and d_s are constant. The secondary duty cycle d_s is fixed at 0.5, and the phase displacement θ is selected to obtain ZVS for the switches of the secondary rectifier. For this purpose, as presented in Section 6.3, the currents flowing the switches S_{s1} and S_{s2} must be negative before they are deactivated. In other words, the secondary current i_s must lead the secondary voltage v_s. From (6.3), (6.5), (6.10), (6.11) and (6.12), θ should be slightly less than $\pi/2$ to achieve ZVS for the secondary rectifier switches and to minimize the VA rating of the converters.

6.5 Design Procedure

The charging system is designed at the peak of the input voltage. It is assumed that the input power factor is unity, thus the input voltage v_i and the input current i_i are as follows

$$v_i = V_m \sin \omega_i t,\ i_i = I_m \sin \omega_i t \tag{6.13}$$

where V_m and I_m are the peak input voltage and the peak input current, and ω_l is the line angular frequency. The peak input current is calculated by

$$I_m = \frac{2P_o}{\eta V_m} \tag{6.14}$$

where P_o is the output power and η is the system efficiency.

A minimum duty cycle D_{pm} is selected to limit the peak clamping voltage at the peak input voltage

$$D_{pm} = \frac{V_m}{V_{cm}} \tag{6.15}$$

where V_{cm} is the peak clamping voltage, and it should be 50% ~ 70% of the peak switching device voltage.

Once the minimum duty cycle is obtained, the input inductor is designed according to the maximum input current ripple requirement, ΔI_m, at the peak input voltage

$$L_i \geq \frac{\left(1-D_{pm}\right)V_m}{\Delta I_m f_s} \tag{6.16}$$

Then the phase displacement θ that is slightly less than $\pi/2$ is selected to achieve ZVS for the secondary rectifier and to minimize the VA rating of the converters. Once θ is selected, the mutual inductance M can be designed. As the primary and secondary resonant circuits are tuned to the switching frequency, the mutual inductance M is obtained from (6.12) at the peak of input current where $i_i = I_m$, $d_p = D_{pm}$, and $d_s = 0.5$.

$$M = \frac{2V_b \sin\theta}{\pi\omega_s I_m}\frac{\sin\pi D_{pm}}{\pi D_{pm}} \tag{6.17}$$

Once the mutual inductance is identified, the coil self-inductances L_p and L_s are determined depending on the coil geometry and power transfer distance (air gap). For a predefined M, a longer air gap results in larger coupling coils with higher self-inductances, and vice versa.

Since primary and secondary resonant circuits are tuned to the switching frequency, the primary and secondary compensation capacitances are obtained as

$$C_p = \frac{1}{\omega_s^2 L_p},\ C_s = \frac{1}{\omega_s^2 L_s} \tag{6.18}$$

The clamping capacitor, C_i, is chosen corresponding to the allowable switching voltage ripple, ΔV_c in the clamping voltage. The maximum value of ΔV_c is reached around the zero-crossing area of the input voltage where the input current i_i reaches zero, and the clamping capacitor C_i is charged and discharged by the primary current during a half switching cycle. The clamping capacitor C_i is obtained by

$$C_i = \frac{\Delta Q}{\Delta V_c} = \frac{1}{\omega_s}\frac{\int_{\pi/2-\theta}^{3\pi/2-\theta} i_p d\omega_s t}{\Delta V_c} = \frac{2I_{pp}}{\omega_s \Delta V_c} \tag{6.19}$$

where ΔQ is the amount of charge injected in (or extracted from) the clamping capacitor C_i, and $T_s = 1/f_s$ is the switching period, and $I_{pp} = \dfrac{2V_b}{\pi\omega_s M}$ is the peak of the primary current.

6.6 Summary

In this chapter, a new direct AC/AC active-clamped HB converter feeding the SS IPT charging system was proposed. The operation principles, switching scheme, steady-state analysis, and design procedure of the proposed charging system were presented in detail. The proposed AC/AC converter has several advantages as follows:

1) The front-end rectifier is eliminated, resulting in an actual single-stage (AC-to-AC) conversion with less the number of semiconductors (only 4 active switches);
2) The use of the life-limited electrolytic DC-link capacitors is avoided;
3) The switching scheme is simple;
4) The ZVS can be achieved for the primary AC/AC converter and secondary rectifier to improve the system efficiency, which will be experimentally verified in the next chapter.

However, the main weakness of the proposed converter is that the lower switches experience the high current stress, and hard switching. By reducing the phase displacement θ, the ZVS operation for all switches of the AC/AC converter and the rectifier can be achieved in constrained operating regions, as demonstrated in Appendix C. However, the significant reduction of θ makes the reactive power circulating in the converters and inductive coils increase, in turn exacerbates their conduction losses. In addition, the power transfer capability of the system decreases with the decrease of θ when the minimum duty cycle of the AC/AC converter is limited, as shown in (6.12). In the next chapter, a hybrid dual-loop control strategy for the proposed charging system will be developed. It enables the unity power factor and charging current regulation.

Chapter 7. Control Design for Direct AC/AC Active-clamped Half-bridge Converter Based Inductive Charging System – Operation Principles, Modeling and Design

7.1 Introduction

In this chapter, a hybrid dual-loop control strategy comprising a predictive dead-beat current controller and a linear average current controller is developed for the direct AC/AC active-clamped HB converter based IPT charging system. This proposed control scheme enables regulating the input power factor and charging current in a single power conversion stage. The detailed control diagram is shown in Figure 7.1. Due to the absence of the DC-link capacitor in the AC/AC converter to absorb double line frequency ripple, the battery current, i_b contains a double line-frequency ripple. The SRC charging technique reported in [107, 108] allows batteries to be charged by double line frequency (100 or 120 Hz) current with minor side effects on their performance. The outer loop is established to regulate the average line-cycle battery current. The average battery current feedback I_b can be obtained using an infinite impulse response (IIR) filter. The output of the outer control loop is the peak input current reference I_m^* which is multiplied by v_i/V_m to generate the sinusoidal reference current i_i^* for the inner current loop. Since a wide bandwidth inner current control loop is required to rapidly track variable current reference, a digital predictive deadbeat controller with a very fast dynamic response is used in the inner control loop. The performance of the deadbeat control is superior to that of the conventional linear controller [162-164]. Another advantage of using the deadbeat control is that the load and coupling coefficient variations are not considered in controller design, and it can be easily

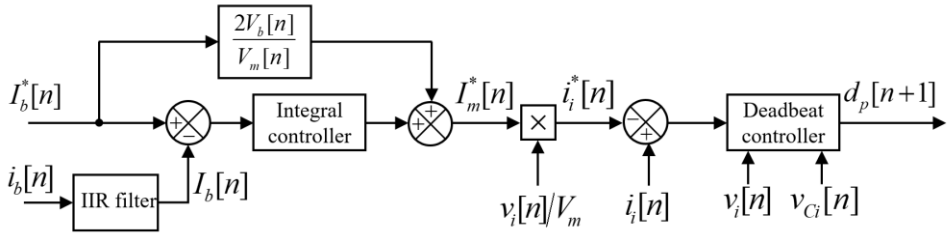


Figure 7.1: Control block diagram.

implemented with the measurement of the input current, input voltage, and clamping voltage.

7.2 Inner Current Control Loop

The inner control loop is implemented to correct the input current following the input voltage, in turn, to obtain unity power factor at the direct AC/AC converter input. In this loop, the average switched input current is controlled using a predictive deadbeat controller. The dual edge/triangle modulation is adopted to generate the PWM signals driving the direct AC/AC converter. For such a PWM generation technique, the average value of the input current can be obtained by synchronizing the sampling at the peak or valley of the carrier signal [165]. Figure 7.2 shows the triangle modulation waveforms and resulting inductor current waveform during positive half line cycle. It is assumed that the input voltage and the clamping voltage are constant during a switching period.

The input current at the instant $(n + 1)T_s$ can be predicted as

$$i_i[n+1] = i_i[n] + \frac{T_s}{L_i} v_i[n] - \frac{T_s}{L_i} d_p[n] v_{Ci}[n] \tag{7.1}$$

where $i_i[n]$, $v_i[n]$, $v_{Ci}[n]$ are the average switched values of input inductor current, input voltage, and clamping voltage at the sampling instant nT_s.

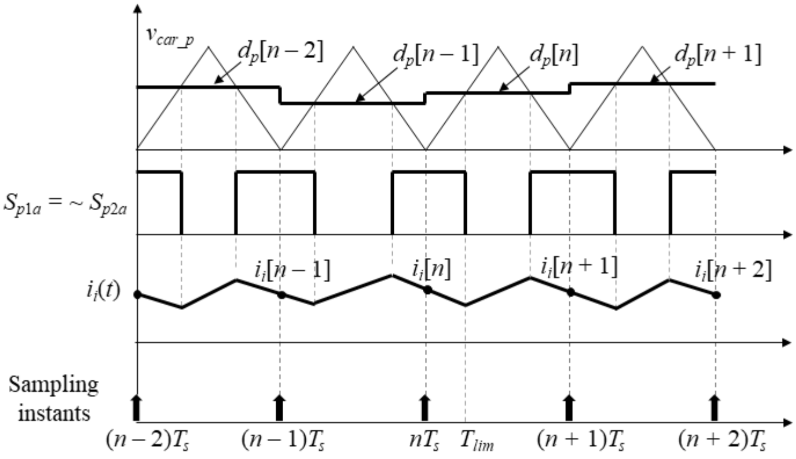


Figure 7.2: Triangle modulation waveforms and sampling instants of input current.

From (7.1), it would be possible to calculate the duty cycle $d_p[n]$ to make $i_i[n + 1]$ reach its reference value by the end of the following modulation period, $(n + 1)T_s$. Therefore, a one-cycle-delay dynamic response for the deadbeat control is achieved. In practice, as sampling required signals, $i_i[n]$, $v_i[n]$, $v_{Ci}[n]$, and calculating duty cycle $d_p[n]$ occupy part of the modulation period. As a result, it cannot guarantee that, in all cases, the duty cycle computation can be completed and updated before the instant T_{lim} when the switches have to change their states, as shown in Figure 7.2. Especially, in the cases of low duty cycles, the instant T_{lim} is very close to the instant nT_s, thus giving a very short time for computation.

In order to mitigate the aforementioned timing problem, the duty cycle can be computed for one step forward. For example, instead of the duty cycle $d_p[n]$, the duty cycle $d_p[n + 1]$ is computed. This allows a whole modulation period to complete the computation. By shifting (7.1) one step forward, the input current at the instant $(n + 2)T_s$ can be predicted as

$$i_i[n+2] = i_i[n+1] + \frac{T_s}{L_i} v_i[n+1] - \frac{T_s}{L_i} d_p[n+1] v_{Ci}[n+1] \tag{7.2}$$

By substituting (7.1) to (7.2), and assuming that $v_i[n+1] = v_i[n]$, $v_{Ci}[n+1] = v_{Ci}[n]$ and $i[n+2] = i_i^*[n]$, the duty cycle $d_p[n+1]$ can be found as

$$d_p[n+1] = \frac{L_i}{T_s v_{Ci}[n]} \left(i_i[n] - i_i^*[n] \right) + 2\frac{v_i[n]}{v_{Ci}[n]} - d_p[n] \tag{7.3}$$

where $i_i^*[n]$ is the input current reference at the instant $(n+2)T_s$,. From (7.3), the duty cycle $d_p[n+1]$ for modulation period $[(n+1)T_s, (n+2)T_s]$ can be determined to make the input current reach its reference at the instant $(n+2)T_s$ with a two-cycle delay.

The main drawback of the current control law (7.3) is the dependency of its gain, $k_c = L_i / T_s\, v_{Ci}[n]$, on parameters such as L_i and v_{Ci}. These parameters can differ from their nominal values due to the operation environment change, aging, or the inaccurate measurement of the converter parameters. Therefore, the controller robustness to the parameter variations must be investigated through a stability analysis. The equation (7.3) can be rewritten as

$$d_p[n+1] = \frac{\alpha L_i}{T_s \beta v_{Ci}[n]} \left(i_i[n] - i_i^*[n] \right) + 2\frac{v_i[n]}{v_{Ci}[n]} - d_p[n] \tag{7.4}$$

where α and β are the mismatch factors of the input inductor and clamping voltage, respectively. Both α and β are unity when the input inductor and clamping voltage perfectly match their actual values.

The impact of the mismatch factors on the system stability can be investigated by applying the *Z*-transform to (7.1) and (7.4), then deriving the closed-loop transfer function,

$i_i(z)/i_i^*(z)$, and determining its poles (the roots of the characteristic equation). The closed-loop transfer function is stable if its poles are inside the unit circle.

The closed-loop transfer function is given as

$$\frac{i_i(z)}{i_i^*(z)} = \frac{\frac{\alpha}{\beta}}{z^2 - 1 + \frac{\alpha}{\beta}} \tag{7.5}$$

Therefore, the poles of the closed-loop transfer function can be found as

$$z_{p1,2} = \pm\sqrt{1 - \frac{\alpha}{\beta}} \tag{7.6}$$

It can be observed that the condition for the closed-loop transfer function to obtain stability is $\alpha < 2\beta$. Therefore, the worse cases of the system stability occurs when the input inductor is overestimated ($\alpha > 1$), and the clamping voltage is underestimated ($\beta < 1$). For example, if the clamping voltage is accurately measured ($\beta = 1$), the maximum input inductor tolerance to keep the system stable is less than 100% ($\alpha < 2$). However, when the measured clamping voltage is 10% less than the actual value ($\beta = 0.9$), the maximum input inductor tolerance for the system stability is less than 80% ($\alpha < 1.8$). The above stability analysis reveals that the controller has a considerable robustness against the parameter mismatches.

7.3 Outer Current Control Loop

The peak input current reference I_m^* is generated the outer current control loop, in which the average battery current over a line cycle is regulated. It is assumed that power losses are ignorable, the peak input current reference I_m^* can be approximated using the average power balance at the input and output.

$$I_m^* = \frac{2V_b}{V_m} I_b^* \tag{7.7}$$

where I_b^* is the average battery current reference.

The peak input current reference I_m^* can be generated using (7.7) without battery current feedback measurement. However, the equation (7.7) is valid only when the system efficiency is unity, which cannot be satisfied in the real system. Therefore, a steady-state error between the actual battery current and its reference is always maintained, and it becomes worse when the efficiency is low or the parameter mismatches happen in the inner control loop.

By adding a variation ΔI_b into battery current term, the equation (7.7) can be rewritten as

$$I_m^* = \frac{2V_b}{V_m} I_b^* + \frac{2V_b}{V_m} \Delta I_b = I_{mn} + \Delta I_m \tag{7.8}$$

As expressed in (7.8), the peak input current reference comprises a nominal term I_{mn} and a variation term ΔI_m as follows

$$I_{mn} = \frac{2V_b}{V_m} I_b^* \tag{7.9}$$

$$\Delta I_m = \frac{2V_b}{V_m} \Delta I_b \tag{7.10}$$

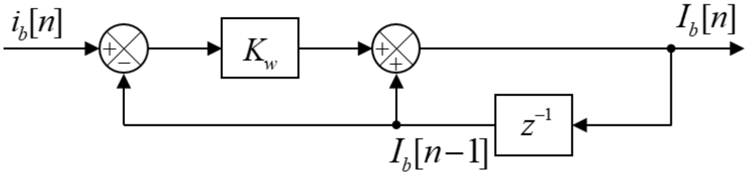


Figure 7.3: Block diagram of the exponential moving average IIR filter.

The feedback controller is designed to nullify the steady-state error based on the variation term. For this purpose, a simple integral controller given by (7.11) can be employed.

$$G_c(s) = \frac{K_i}{s} \tag{7.11}$$

where K_i is the integral gain, and is tuned to provide a very low-bandwidth outer control loop (much slower than double line frequency), which avoids distorting the input current. Once the continuous time controller has been obtained, it can be transformed to the discrete domain using the using the backward Euler method

$$G_c(z) = \frac{K_i T_s}{1 - z^{-1}} \tag{7.12}$$

In order to improve the dynamic response of the outer control loop, the nominal term can be added as a feedforward value, as shown in Figure 7.1.

The outer current control loop requires the average value of the battery current as a feedback signal. An exponential moving average IIR filter is used to obtain the average value of the battery current, a sinusoidal-like DC current with double line frequency. The major advantage of using this filter is less computational requirement with a multiplier and two adders, as shown in Figure 7.3. The *z*-domain transfer function of the filter is given

$$\frac{I_b(z)}{i_b(z)} = \frac{K_w}{1-\left(1-K_w\right)z^{-1}} \tag{7.13}$$

where K_w is the weight coefficient ($0 < K_w < 1$), and is chosen based on the desired cut-off frequency f_c and the sampling frequency $f_s = 1/T_s$.

$$K_w = \frac{2\pi f_c}{f_s} \tag{7.14}$$

7.4 Verifications and Discussions

A 1.0-kW laboratory prototype shown in Figure 7.4 is designed and implemented to verify the theoretical analysis. The prototype is designed by following the procedure in Section 6.5 in Chapter 6 with the major specifications as: the input voltage is 120 V_{rms}/60 Hz, the nominal battery voltage is 250 V, the rated output power is 1 kW, and the switching frequency is 85 kHz. The system efficiency η is assumed to be 0.9. The angle $\theta = 80^0$ is selected to achieve ZVS for the secondary rectifier switches and to minimize the VA rating of the converters. The minimum duty cycle D_{pm} is 0.28 to limit the peak clamping voltage at 600 V. SiC MOSFETs, C2M0040120D (1200 V/60 A), are used to implement the direct AC/AC active-clamped converter, while the secondary rectifier switches are SiC MOSFETs SCT3060AL (650 V/39 A). A film capacitor, F340X153348MPP2T0 (3.3 μF/480 V), is employed for the clamping capacitor. The compensation capacitors are formed by arranging 700-V TDK film capacitors in parallel and series.

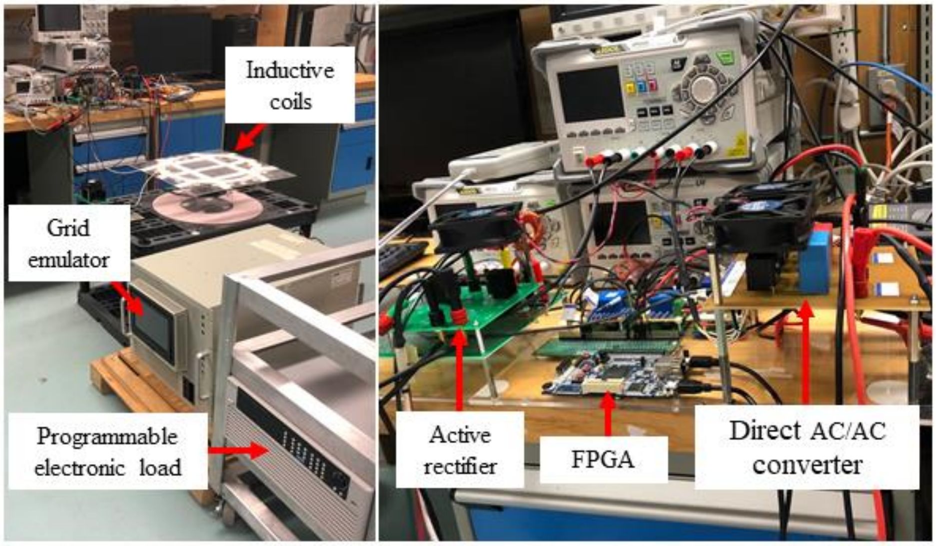


Figure 7.4: Experimental prototype.

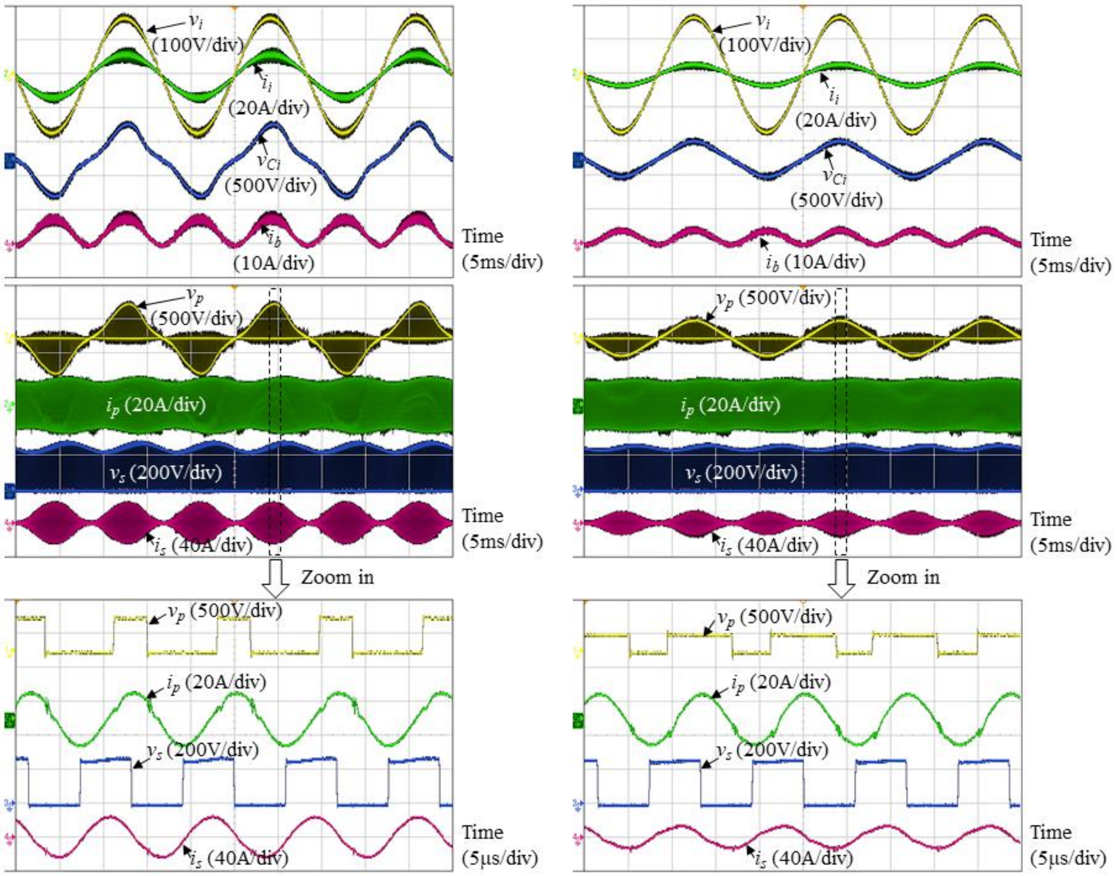
The circular inductive coils are fabricated using the Litz wire with 1050 strands of AWG 38. The primary coil has 26 turns, and its inner and outer diameters are 226 mm and 490 mm, respectively. The secondary coil's turn number, inner and outer diameters are 8 turns, 368 mm and 450 mm. The nominal air gap between primary and secondary coils is 170 mm. An electronic load (Chroma 63205A-1200-200) at constant voltage mode is adopted to emulate the battery. The dual-loop control strategy and PWM generation are implemented in an FPGA (A2F200M3F). The integral gain of the outer loop controller is tuned to 18, and the weight coefficient of the IIR filter is 7.3×10^{-4}. Table 7.1 shows the detailed prototype parameters. The calculation of the parameters is shown in Appendix D.

Figure 7.5 shows the steady-state current and voltage waveforms at the input, output, primary and secondary coils at the full load (V_b = 250 V and I_b = 4 A) and half load (V_b = 250 V and I_b = 2 A) conditions. It can be observed that the input current i_i is sinusoidal and in phase with the input voltage v_i. The absence of a DC-link capacitor in the direct AC/AC

Table 7.1: Charging system specifications

Parameter	**Symbol**	**Value**	**Unit**
Nominal output power	P_o	1.0	kW
Battery voltage	V_b	250	V
Input voltage	V_i	120	Vrms
Line frequency	f_i	60	Hz
Switching frequency	f_s	85	kHz
Maximum input current ripple	ΔI_m	2	A
Maximum clamping voltage ripple	ΔV_c	20	V
Primary self-inductance	L_p	297.2	μH
Secondary self-inductance	L_s	52.8	μH
Mutual inductance	M	20.6	μH
Primary compensation capacitor	C_p	11.88	nF
Secondary compensation capacitor	C_s	66.3	nF
Boost inductor	L_i	1.02	mH
Clamping capacitor	C_i	3.3	μF
Output filter capacitor	C_o	520	μF

converter causes a double line frequency fluctuation in transferred power. This results in a fluctuating battery current and secondary current at double line frequency (120 Hz) as shown in Figure 7.5. The variation of the clamping voltage over a half line cycle can be calculated using (6.4) and (6.12) with the assumption of the unity input power factor. The calculated and measured clamping voltages are depicted in Figure 7.6. There is a good agreement between the theoretical calculation and experimental measurement, which verifies the accuracy of the steady-state analysis in Section 6.4 in Chapter 6.



(a) (b)

Figure 7.5: Experimental steady-state waveforms of the charging system at (a) V_b = 250 V and I_b = 4 A, and (b) V_b = 250 V and I_b = 2 A.

Figure 7.7 shows the experimental waveforms to verify the ZVS of the AC/AC converter and the rectifier. On the AC/AC converter, it can be seen that the primary voltage v_p is unchanged when S_{p1a} is activated or deactivated, whereas the primary voltage v_p changes its status whenever S_{p2a} is turned on or turned off. Therefore, S_{p1a} obtains both zero-voltage turn on and turn off whereas S_{p2a} suffers hard turn on and hard turn off. On the secondary rectifier, the secondary voltage v_s does not change its status when S_{s1} or S_{s2} is turned on. It means that zero-voltage turn on is maintained for both the switches.

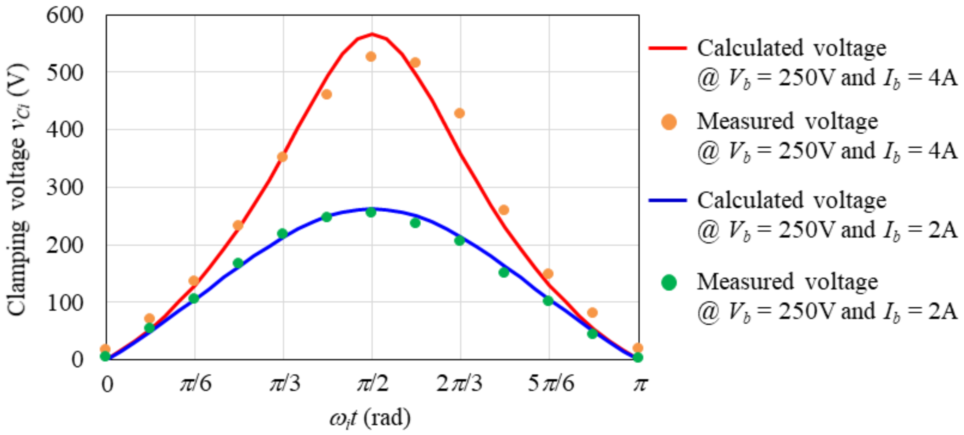


Figure 7.6: Analytical and experimental comparison of clamping voltage over half line voltage (Calculation and experimental results).

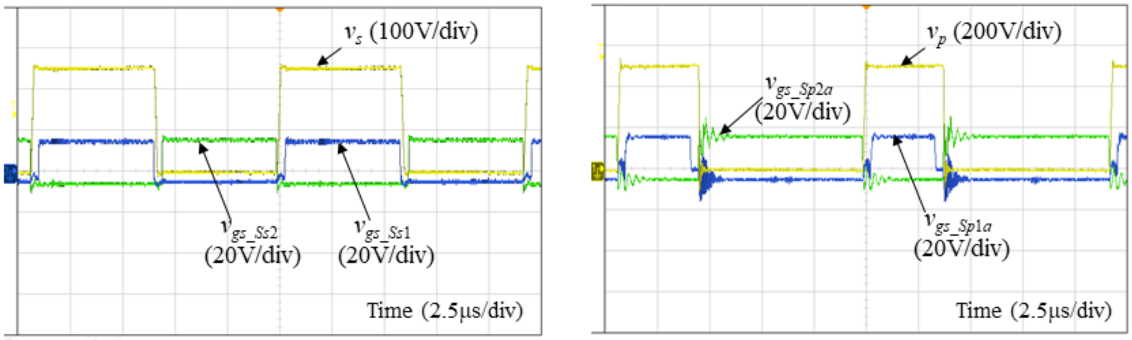


Figure 7.7: Experimental waveforms validating the ZVS of the AC/AC converter and rectifier.

Figure 7.8 shows the dynamic response of the charging system under the step change of the average battery current reference. It is observed that the system obtains a fast response and retains stability even when the current command steps from 100% load (4 A) to 50% load (2 A) at the peak of the input voltage. Moreover, the average battery current follows the command values after and before the transition time. Figure 7.9 shows the dynamic response of the charging system when the average battery current command maintains 4 A, and the output battery voltage steps from 200 to 250 V. Although the step

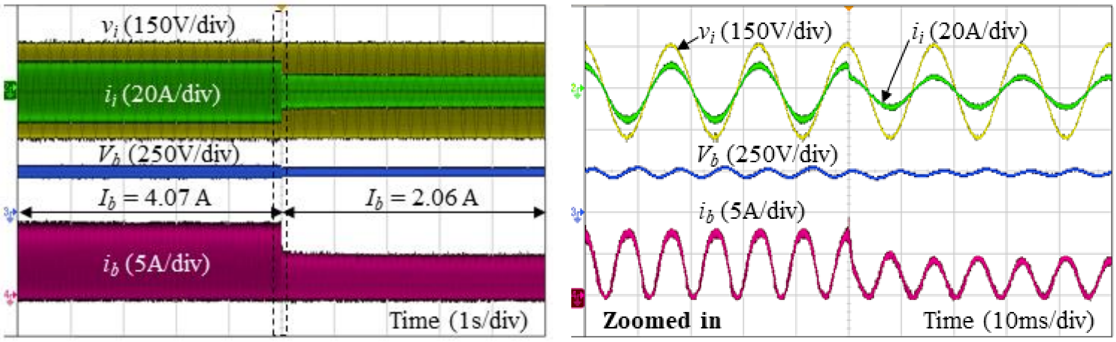


Figure 7.8: Dynamic response of the proposed charging system under the average battery current command step change from 4 A to 2 A at V_b = 250 V (Experimental results).

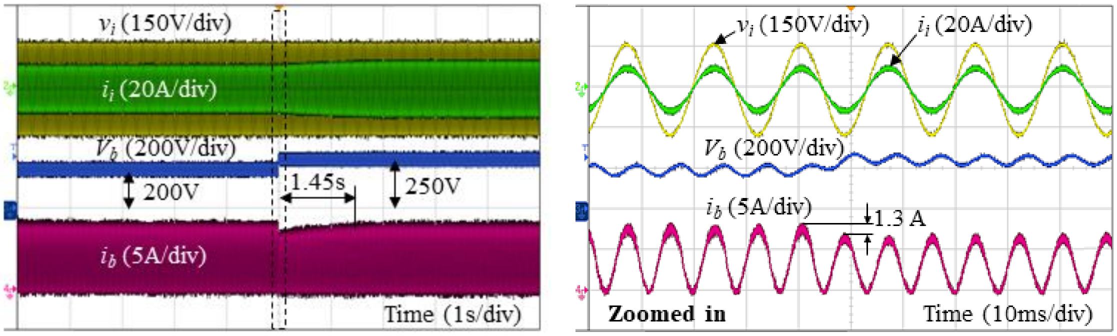


Figure 7.9: Dynamic response of the charging system under the battery voltage step change from 200 V to 250 V at I_b = 4 A (Experimental results).

change of the battery voltage is unrealistic in the charging applications, the experimental waveforms under its step change are showed to validate he dynamic performance of the controller at the worst scenarios. It can be seen that the system stability is still obtained even when the output battery voltage suddenly increases. The battery current drops by 1.3 A, then recovering back to initial value after 1.45 s.

Figure 7.10 illustrates the input current total harmonic distortion (THD) and system efficiency at the nominal battery voltage, V_b = 250 V, but at different average charging

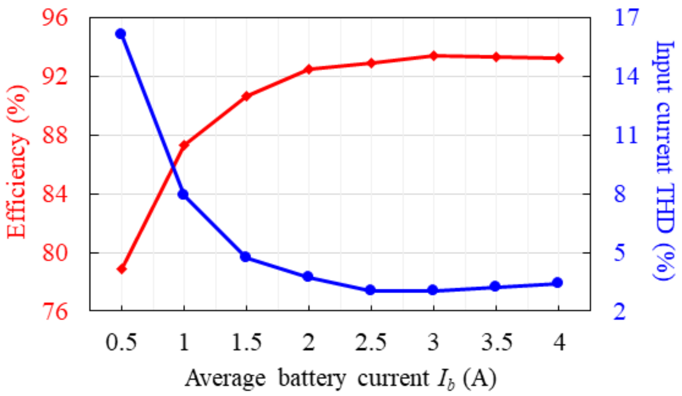
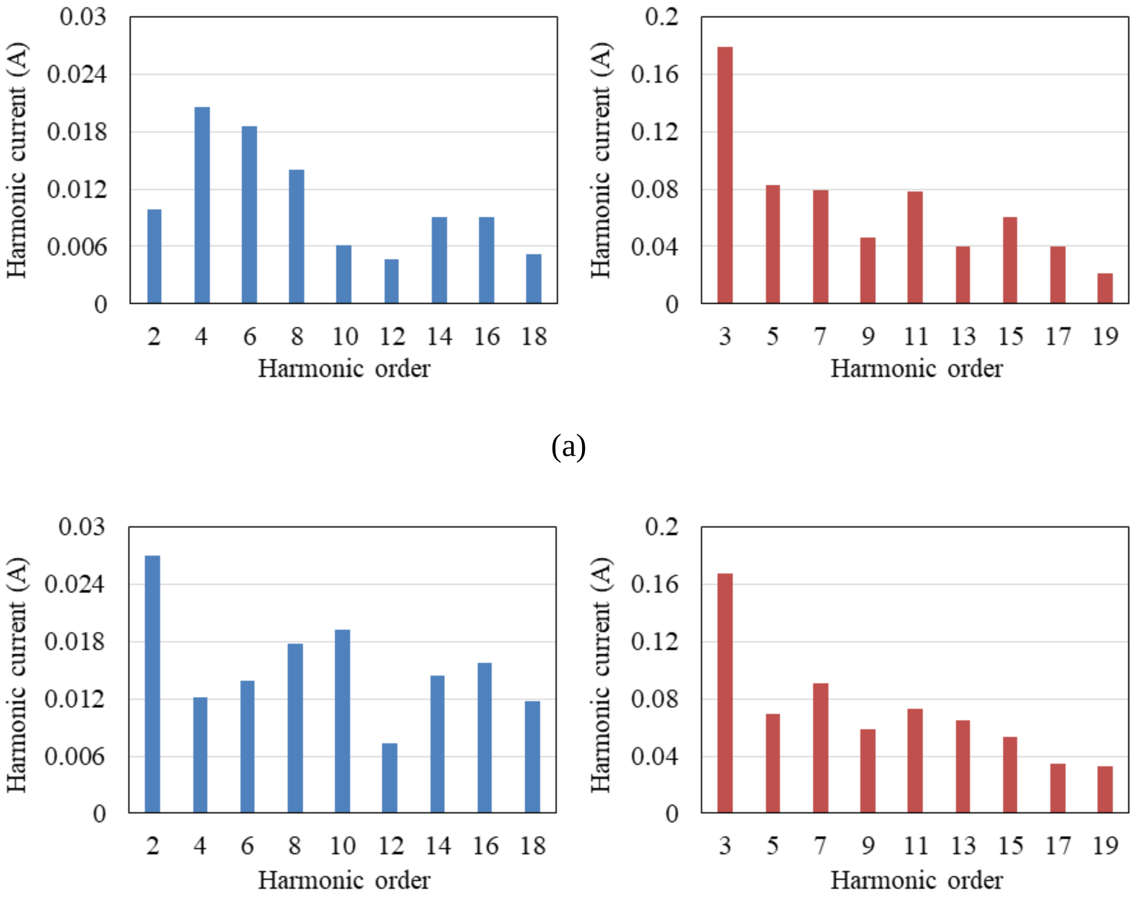


Figure 7.10: Input current THD and system efficiency at different charging currents (Experimental results).

current values. The input current quality and efficiency are evaluated using Fluke 438-II Power Analyzer. The THD of the input current is 3.4% at the full load condition (I_b = 4 A), it achieves the minimum value of 3% at I_b = 3 A, and then it increases with the decrease of the charging current. The input power factor remains at 0.99 or above in a wide charging current range from 1.5 A to 4 A. Figure 7.11 shows the harmonic contents of the input current at the full load (V_b = 250 V and I_b = 4 A) and half load (V_b = 250 V and I_b = 2 A) conditions. It can be seen that input current harmonic contents comply with the IEC 61000-3-2 Class A standard [166]. The classification and current harmonic limit in the IEC 61000-3-2 are provided in Appendix F.

For the system efficiency, as shown in Figure 7.10, a peak efficiency of 93.4% is achieved at I_b = 3 A while an efficiency of 93.2% is measured at the nominal charging current, I_b = 4 A. Table 7.2 shows a comparison between the proposed direct AC/AC active-clamped HB converter based SS-IPT system and various single-stage converter based IPT systems in literature. It is clear that the proposed IPT system demonstrates a higher performance compared to the other systems regarding component count, input current quality, and efficiency.

Figure 7.12 shows the detailed loss distribution of the designed charging system. The system loss distribution is simulated by using PSIM. It can be observed that the primary coil losses dominate the total system losses. The conduction losses of S_{p2a} and S_{p2b} are significantly high when the charging current is high. This is due to the fact that they carries both i_p and i_{Li} during the large interval of the modes 7, 8 and 9 as shown in Figure 6.2.



(a)

(b)

Figure 7.11: Input current harmonic contents at (a) V_b = 250 V and I_b = 4 A, and (b) V_b = 250 V and I_b = 2 A (Experiment results).

Table 7.2: Comparison of various single-stage converter based IPT systems

Ref.	Coupling coefficient	Number of semiconductor devices	Switching frequency (kHz)	Power (kW)	Input current THD (%)	Peak efficiency (%)
Buck-derived MC [96]	0.29	12 switches	20	1.0	3.3 (with input *LC* filter)	89.6
Boost-derived MC [100]	0.22	4 diodes + 8 switches	48	1.2	4.5 (with input capacitor filter)	N/A
Bridgeless boost PFC converter and FB-VSI [102]	0.19	6 diodes + 4 switches	111.6	2.56	15.4 (with input *LC* filter)	90.1
Proposed	0.16	6 switches	85	1.0	3.4 (without input filter)	93.4

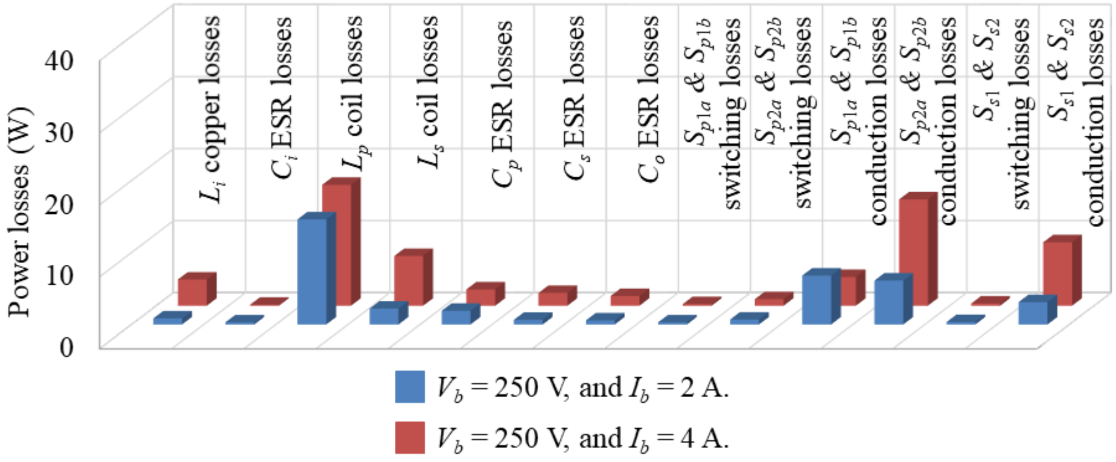


Figure 7.12: Loss distribution of the proposed charging system (Simulation results).

Some simulation results are given to evaluate the performance of the charging system under the variation of the mutual inductance and compensation capacitors. Note that, the simulation validation is realized by a PSIM-ModelSim co-simulation with PSIM simulating the power stage and ModelSim running Verilog code implemented in FPGA (controllers and PWM generation).

Figure 7.13, 7.14, and 7.15 show the steady-state waveforms of the currents and voltages in the charging system at the different conditions of tuning and misalignment when V_b is 250 V and I_b is 4 A. It can be observed that the charging current and input current are effectively controlled, the input current remains sinusoidal and in phase with the input voltage in all conditions of the parameter variations. The simulating input current THD is in the range of 3.2 % - 4.0%, and the simulating input power factor is always higher than 0.99.

Figure 7.13 shows that the higher primary current is required to maintain the output power when the mutual inductance is reduced, causing higher losses on the primary coil, the primary capacitor and the switches of the AC/AC converter, as illustrated in Figure 7.16. Note that the thermal modules in PSIM are utilized to simulate the power losses of the switching devices and passive components, and the internal resistances of the primary and secondary coils are also included in simulation to evaluate their losses.

The secondary current is sensitive to the reduction of the primary capacitance. Particularly, the secondary current increases by 30% when the primary capacitance decreases by 5%, as shown in Figure 7.14 (b). As a result, the losses of the secondary coil, the secondary capacitor and the rectifier increase, as shown in Figure 7.16. In this simulation, the variation of the primary capacitance is limited at 5% to prevent exceeding the current rating of the rectifier's switches (Rohm SCT3060AL 650V/39A). On the other hand, the primary current is sensitive to the variation of the secondary capacitance. A double line frequency fluctuation can be observed in the primary current when the secondary circuit is in the off-resonance condition, as depicted in Figure 7.15. That is because the fluctuation of the voltage across the secondary coil is not cancelled by the voltage of the secondary compensation capacitor. As can be seen in Figure 7.16, the primary current increases significantly when the secondary capacitance reduces, which causes more losses on the primary side.

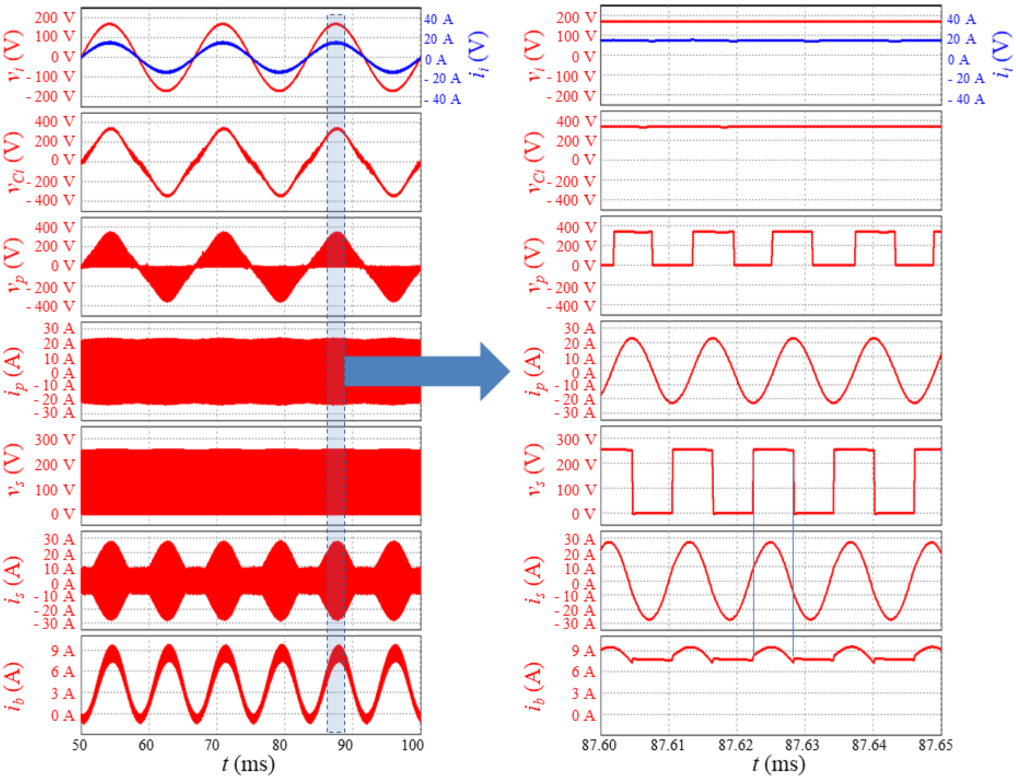
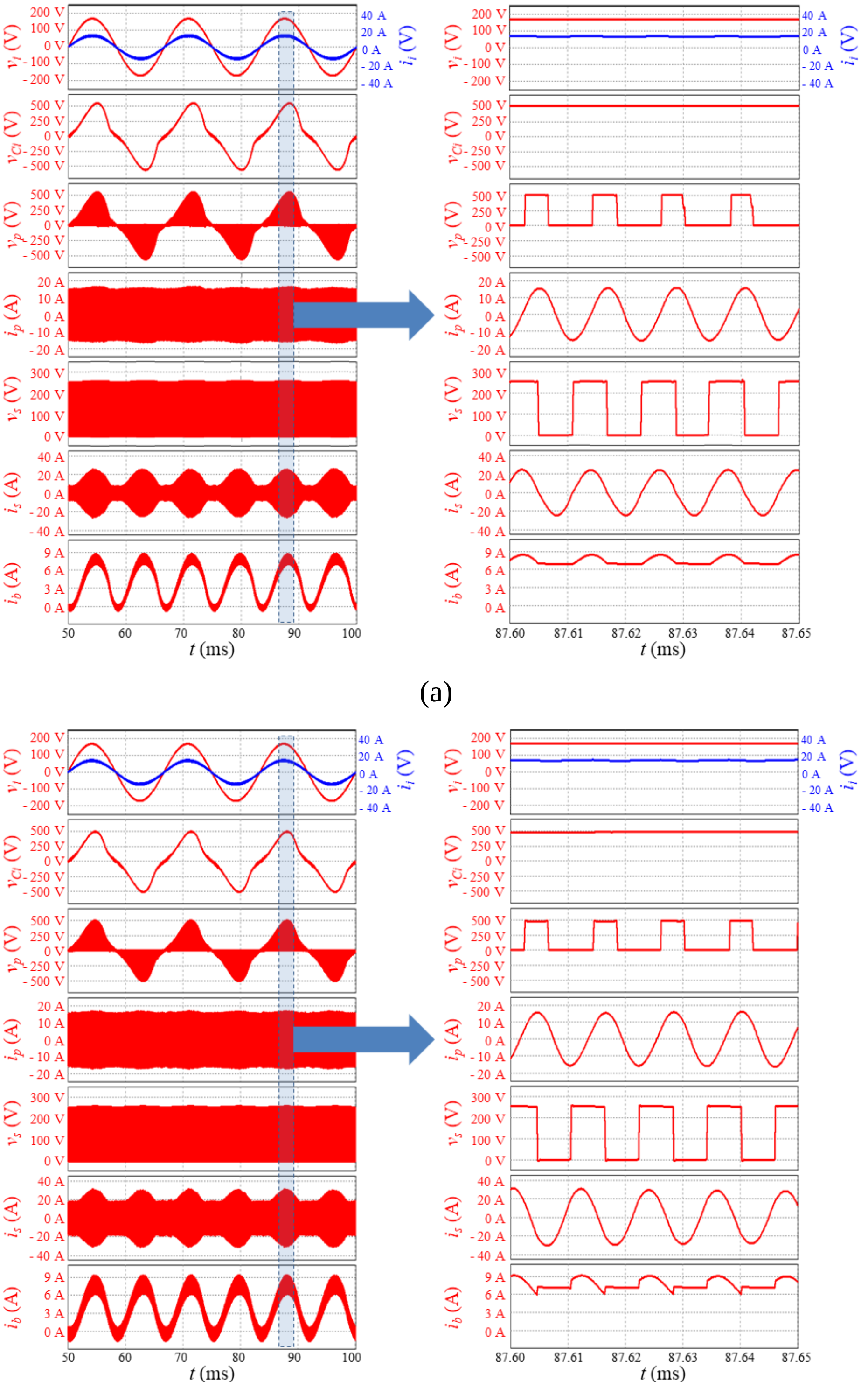


Figure 7.13: Simulation steady-state waveforms in the charging system when M decreases



(a)

(b)

Figure 7.14: Simulation steady-state waveforms in the charging system (a) when C_p increases by 5%, and (b) when C_p decreased by 5%.

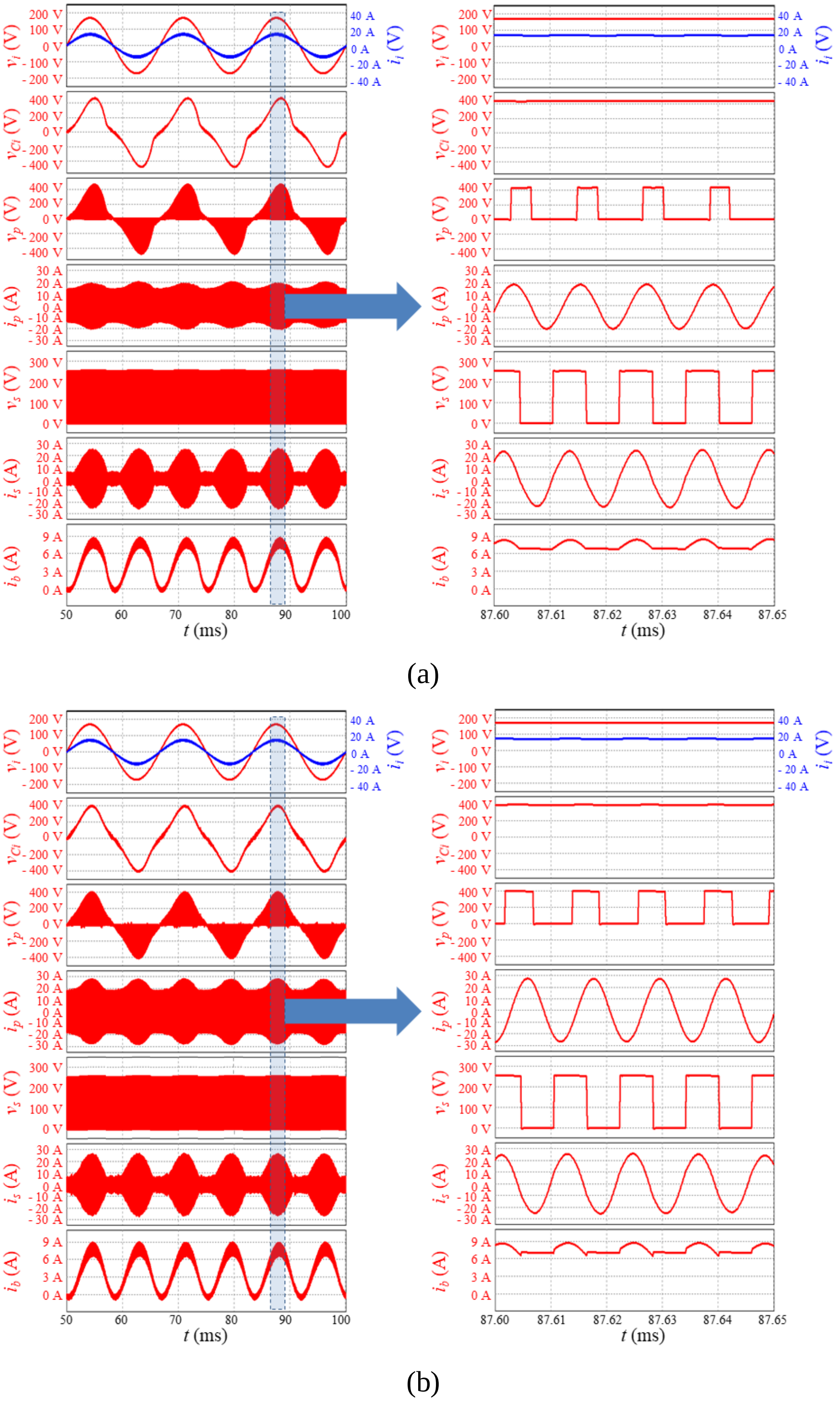


Figure 7.15: Simulation steady-state waveforms in the charging system (a) when C_s increases by 20%, and (b) when C_s decreased by 20%.

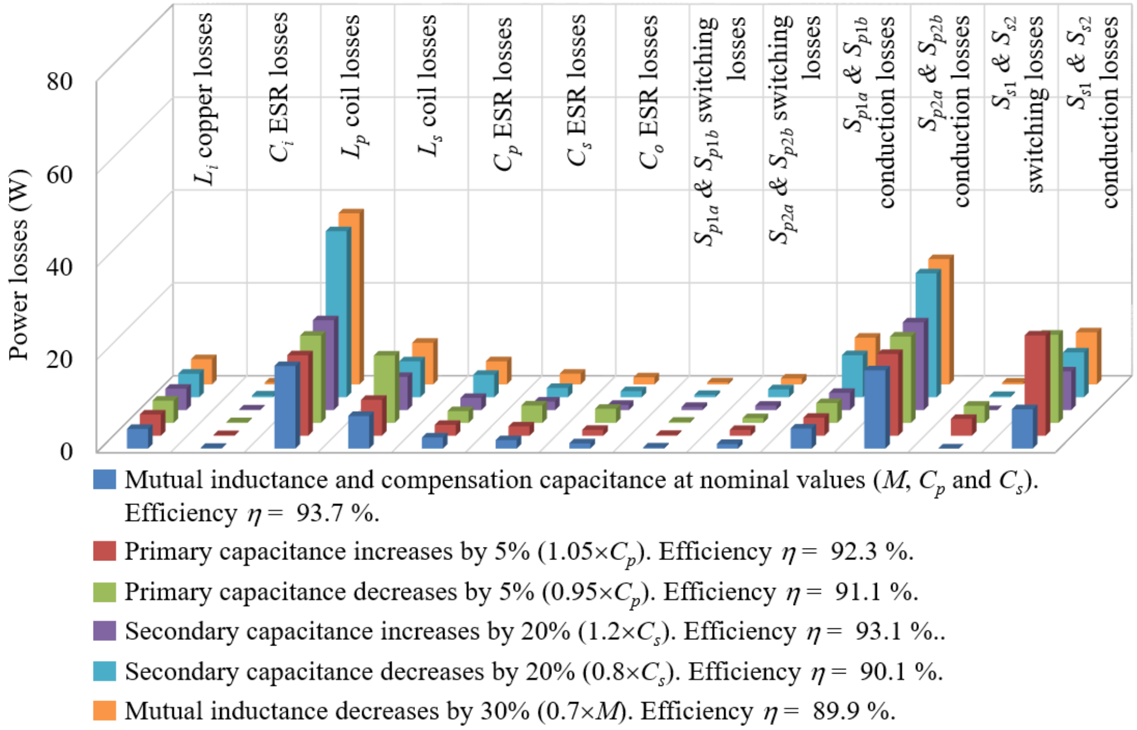


Figure 7.16: Loss distribution at the different conditions of tuning and misalignment (Simlation results).

7.5 Summary

In this chapter, a hybrid dual-loop control scheme which enables the input power factor correction and the average charging current regulation was proposed. A 1.0-kW SiC-based prototype was designed and implemented to verify the feasibility of the proposed control scheme and the theoretical analyses in Chapter 6. The controller is realized on an FPGA controller (A2F200M3F). The experimental results showed that the battery charging current is effectively controlled, and a unity power factor is achieved over a wide range of the charging current command and the battery voltage. All input current harmonics are in compliance with the IEC 61000-3-2 Class A standard. Due to single-stage-power-conversion and soft-switching features, the proposed charging system obtained the maximum efficiency of 93.4 %, which is higher than that of other single-stage converter based IPT systems reported in literature. However, the high current stress and hard switching on the lower switches of the AC/AC converter are the weaknesses of the proposed charging system, and they might become worse at lower input voltage where a higher input current is required to provide the same output power. These issues can be overcome by paralleling switches. The performance of the charging system at different conditions of tuning and misalignment are also evaluated by simulation. It can be observed that the input and charging currents are still effectively controlled under the parameter variations.

Chapter 8. Conclusions and Future Work

8.1 Conclusions

A comprehensive study on power supply converter topologies for EV IPT charging applications has been undertaken in this thesis. Initially, Chapter 1 presented a general introduction to the WPT technologies such as APT, RFPT, OPT, CPT, and IPT. It is found that the IPT has been widely accepted in for many practical WPT applications, especially for the EV charging applications. The IPT-based EV chargers bring several benefits such as safety, convenience, flexibility, weather immunity, as well as possibility of range extension and cost reduction for the EVs. Among various research topics, the development of the high-frequency power supply converters is a primary importance for the IPT charging systems. The dual-stage and single-stage power conversion topologies for the IPT systems were overviewed in Chapter 2. The commonly used CSIs and VSIs in the dual-stage topologies were presented, followed by the exhibition of the single-stage topologies including matrix and integrated structures that enable providing a direct AC/AC conversion. In addition, the compatibility of the power converters, compensation topologies and power control schemes in the IPT applications was discussed.

In Chapter 3, a comprehensive comparison of the conventional dual-stage power conversion topology (boost PFC and FB VSI) and the potential single-stage counterparts including the buck-derived FBMC and boost-derived FBMC was carried out. The performance of the power converters was assessed regarding input current quality, switching stresses, efficiency, and cost. The simulation results revealed that all of the power conversion topologies have advantages and constraints. Particularly, the conventional dual-stage topology has the lowest stress on switching devices, and the boost-derived FBMC provides the greatest input current quality. On the other hand, the superiorities of the buck-derived FBMC over the other topologies are high efficiency, low component count and cost. Despite eliminating the bulky DC-capacitors, the single-stage MCs still have many switching devices, and require complex control schemes. A novel direct AC/AC active-clamped HB converter was proposed in Chapter 6 to address these issues.

The exploration of the proposed AC/AC converter was initialized by investigating the active-clamped HBBI based IPT system. A comprehensive analysis of the soft-switched, active-clamped HBBI in the IPT battery charging applications was performed in Chapter 4. Since its output is a high-frequency voltage, thus it can feed the SS-IPT system with the benefits of simplicity, cost-effectiveness, high efficiency, constant output current, and load-independent compensation. The active-clamped HBBI based SS-IPT charging system was mathematically modeled using the EDF technique. This has resulted in the steady-state and dynamic models that are useful for the system design and analysis. The ZVS mechanism of the fixed-frequency-controlled active-clamped HBBI based SS-IPT charging system was described in detail through the circuit operation modes. Then, the ZVS design methodology that was formulated based on the derived steady-state model equations. In the proposed design approach, the secondary circuit was tuned to the switching frequency to maximize the power transfer capability, whereas the primary circuit was tuned to a resonant frequency that slightly deviates from the switching frequency to obtain ZVS. With the proposed design approach, the bifurcation phenomenon that can cause the loss of ZVS is also eliminated.

In Chapter 5, the theoretical analyses on the active-clamped HBBI based IPT charging system presented in Chapter 4 were validated by the simulation and experimental results. A 1.0-kW prototype with an FPGA based charging current controller was developed. The derived small-signal model was used to design the charging current controller after having been successfully validated using the AC-sweep analysis in the PSIM simulation software. The controller was realized on an FPGA (SmartFusion A2F200M3F). The experimental results showed that the controller tightly regulated the charging current even with the variations of the charging current command, battery voltage, and mutual inductance. The feasibility of the proposed ZVS design approach was also proven through investigating the effect of the mutual coupling on the ZVS boundary of the inverter. It noted that the ZVS region is extended when the mutual inductance reduces. The experimental results revealed that the theoretical analyses are correct. In comparison with the non-ZVS system, the ZVS system is more efficient with an efficiency improvement of 1.1 %. A maximum DC-to-DC efficiency of 93.4% was measured at the nominal coupling coefficient of 0.15 (an air gap of 170 mm), which is comparable to other IPT systems at similar power levels in literature.

Based on the analysis in Chapter 4 and 5, the novel direct AC/AC active-clamped HB converter proposed for the IPT charging applications was studied in Chapter 6. It possesses many appealing features such as less switching devices (only 4 switches), continuous sinusoidal input current, electrolytic DC-link capacitor elimination, simple switching scheme, and ZVS operation. Moreover, the proposed AC/AC converter adopting the SS compensation topology is suitable for the static IPT charging applications. The operation principles were illustrated. A mathematical steady-state modeling and ZVS conditions of the converter were explored. Based on the steady-state analysis, a basic ZVS design procedure for this converter was developed with the necessary design equations being presented in detail.

In Chapter 7, a hybrid control strategy to achieve the unity power factor and the average charging current regulation was proposed for the IPT charging system fed by the direct AC/AC active-clamped HB converter. It consists of two control loops, a linear outer control loop and a nonlinear inner control loop. In the proposed charging system, the SRC charging technique where the battery current contains a double line frequency ripple was adopted. The outer control loop including an integral feedback controller and a feedforward controller was designed to regulate the average battery current with the fast dynamic response and steady-state error elimination. The feedback average battery current for the outer control loop was obtained using the IIR filter that has less computational effort. The output of the outer control loop is the peak input current reference that was consequently synchronized with the input voltage to generate the grid current command for the inner control loop. A digital predictive deadbeat controller with a very fast dynamic response was used in the inner control loop. The implementation of the inner controller is simple with measuring the input current, input voltage, and clamping voltage, but not considering the load and coupling coefficient variations. The stability analysis revealed a considerable robustness of the controller to parameter mismatches. The experimental verifications of the whole charging system with the proposed control scheme were conducted through a 1.0-kW laboratory prototype. The SmartFusion A2F200M3F FPGA was utilized as the core control unit. Experimental results showed that the battery charging current was effectively controlled, and a unity power factor was achieved under the variations of the charging current command and the battery voltage. The input current harmonic emissions complied with the IEC 61000-3-2 Class A standard. Due to less component count and soft-switching features, the proposed charging system obtained the maximum efficiency of 93.4 % at the air gap of 170 mm, which is higher than that of other single-stage converter based IPT systems reported in literature. However, the high current stress and hard switching on the lower switches of the AC/AC converter are the weaknesses of the proposed charging system. They might be overcome by paralleling switches.

8.2 Future Work

Active power-decoupling circuits

The proposed direct AC/AC active-clamped HB converter based IPT charging system adopts the low-frequency (120 Hz) SRC charging technique with a negligible negative impact on the battery performance [101, 106, 108, 109, 167-169]. In the case of requiring charging current ripple reduction, active power-decoupling topologies presented [170-172] can be utilized with the minimized capacitance requirement and no additional power switches, enhancing the performance of the charging system in terms of efficiency, power density, and cost.

Bidirectional IPT systems

For the active-clamped HBBI fed IPT system presented in Chapter 4 and 5, the bidirectional power transfer can be implemented by replacing the diode rectifier on the battery side with the active rectifiers. The modelling analysis, ZVS investigation, and control strategies for the system can be developed in the future research work.

The structure of the direct AC/AC active-clamped HB converter based IPT system proposed in Chapter 6 enables the bidirectional power transfer capability; however, only the gird-to-vehicle (G2V) operation mode was explored. The reverse operation mode, vehicle-to-grid (V2G), can be studied in the future. Particularly, the primary duty cycle-to-input current transfer functions, derived in Appendix E, show right-hand-plane (RHP) zeros when the system is operated in the V2G mode, which requires advanced control strategies. The developed controllers must insure the system stability, fast dynamic response and grid power quality.

Solar-powered IPT charging systems

The wireless charging systems powered by solar energy sources possibly provide a zero-emission solution for the transportation sector. The features of the continuous input current and galvanic isolation make the active-clamped HBBI based IPT system suitable for photovoltaic (PV) applications. The research on the solar-powered IPT charging system using the active-clamped HBBI can be carried out. The system can be analyzed and modeled to develop the effective maximum power point tracking (MPPT) and maximum efficiency point tracking (MPET) control strategies under the influences of shading, panel mismatch, and general variance.

Interleaved structure

The power converter can be modularized as multi-parallel-interleaved converter modules with identical technology to enhance power transfer capability of the IPT systems. As a result of the interleaving configuration, the current stress on each module, input current ripple, and EMI filter size are significantly reduced.

Appendix A. Modelling Equation Derivation of Active-clamped Half-bridge Boost Inverter Based IPT Charging System

A.1 Basic Taylor’s Series Expansion Equations

$$f(x) = f(X + \hat{x}) = f(X) + \hat{x}\frac{df(X)}{dX} \tag{A.1}$$

$$f(x, y) = f(X + \hat{x}, Y + \hat{y}) = f(X, Y) + \hat{x}\frac{df(X, Y)}{dX} + \hat{y}\frac{df(X, Y)}{dY} \tag{A.2}$$

$$\begin{aligned} f(x, y, z) &= f(X + \hat{x}, Y + \hat{y}, Z + \hat{z}) \\ &= f(X, Y, Z) + \hat{x}\frac{df(X, Y, Z)}{dX} + \hat{y}\frac{df(X, Y, Z)}{dY} + \hat{z}\frac{df(X, Y, Z)}{dZ} \end{aligned} \tag{A.3}$$

A.2 Linearization of Nonlinear Equations

The nonlinear equations (4.13), and (4.30)–(4.40) by using (A.1)–(A.3)

$$\begin{aligned} \frac{di_{ps}}{dt} = \frac{d(I_{ps} + \hat{i}_{ps})}{dt} &= \frac{1}{L_2}\left(\frac{2V_{Ci}}{\pi}\sin\pi D + \frac{2}{\pi}\sin\pi D \times \hat{v}_{Ci} + 2V_{Ci}\cos\pi D \times \hat{d}\right) \\ &\quad - \frac{1}{L_2}(V_{Cps} + \hat{v}_{Cps}) - \frac{1}{L_m}(V_{Css} + \hat{v}_{Css}) \\ &\quad + (I_{pc}\Omega_s + \Omega_s\hat{i}_{pc} + I_{pc}\hat{\omega}_s) \\ &\quad - \frac{4}{\pi L_m}\left(\frac{I_{ss}V_o}{I_{sp}} + \frac{I_{ss}}{I_{sp}}\hat{v}_o + \frac{I_{sc}^2 V_o}{I_{sp}^3}\hat{i}_{ss} - \frac{I_{ss}I_{sc}V_o}{I_{sp}^3}\hat{i}_{sc}\right) \end{aligned} \tag{A.4}$$

$$\begin{aligned} \frac{di_{pc}}{dt} = \frac{d(I_{pc} + \hat{i}_{pc})}{dt} &= -\frac{1}{L_2}(V_{Cpc} + \hat{v}_{Cpc}) - \frac{1}{L_m}(V_{Csc} + \hat{v}_{Csc}) \\ &\quad - (I_{ps}\Omega_s + \Omega_s\hat{i}_{ps} + I_{ps}\hat{\omega}_s) \\ &\quad - \frac{4}{\pi L_m}\left(\frac{I_{sc}V_o}{I_{sp}} + \frac{I_{sc}}{I_{sp}}\hat{v}_o - \frac{I_{ss}I_{sc}V_o}{I_{sp}^3}\hat{i}_{ss} + \frac{I_{ss}^2 V_o}{I_{sp}^3}\hat{i}_{sc}\right) \end{aligned} \tag{A.5}$$

$$\begin{aligned}\frac{di_{ss}}{dt}=\frac{d(I_{ss}+\hat{i}_{ss})}{dt}=&\frac{1}{L_m}(\frac{2V_{Ci}}{\pi}\sin\pi D+\frac{2}{\pi}\sin\pi D\times\hat{v}_{Ci}+2V_{Ci}\cos\pi D\times\hat{d})\\&-\frac{1}{L_m}(V_{Cps}+\hat{v}_{Cps})-\frac{1}{L_1}(V_{Css}+\hat{v}_{Css})\\&+(I_{sc}\Omega_s+\Omega_s\hat{i}_{sc}+I_{sc}\hat{\omega}_s)\\&-\frac{4}{\pi L_1}(\frac{I_{ss}V_o}{I_{sp}}+\frac{I_{ss}}{I_{sp}}\hat{v}_o+\frac{I_{sc}^2V_o}{I_{sp}^3}\hat{i}_{ss}-\frac{I_{ss}I_{sc}V_o}{I_{sp}^3}\hat{i}_{sc})\end{aligned}\tag{A.6}$$

$$\begin{aligned}\frac{di_{sc}}{dt}=\frac{d(I_{sc}+\hat{i}_{sc})}{dt}=&-\frac{1}{L_m}(V_{Cpc}+\hat{v}_{Cpc})-\frac{1}{L_1}(V_{Csc}+\hat{v}_{Csc})\\&-(I_{ss}\Omega_s+\Omega_s\hat{i}_{ss}+I_{ss}\hat{\omega}_s)\\&-\frac{4}{\pi L_1}(\frac{I_{sc}V_o}{I_{sp}}+\frac{I_{sc}}{I_{sp}}\hat{v}_o-\frac{I_{ss}I_{sc}V_o}{I_{sp}^3}\hat{i}_{ss}+\frac{I_{ss}^2V_o}{I_{sp}^3}\hat{i}_{sc})\end{aligned}\tag{A.7}$$

$$\frac{dv_{Cps}}{dt}=\frac{d(V_{Cps}+\hat{v}_{Cps})}{dt}=\frac{1}{C_p}(I_{ps}+\hat{i}_{ps})+(V_{Cpc}\Omega_s+\Omega_s\hat{v}_{Cpc}+V_{Cpc}\hat{\omega}_s)\tag{A.8}$$

$$\frac{dv_{Cpc}}{dt}=\frac{d(V_{Cpc}+\hat{v}_{Cpc})}{dt}=\frac{1}{C_p}(I_{pc}+\hat{i}_{pc})-(V_{Cps}\Omega_s+\Omega_s\hat{v}_{Cps}+V_{Cps}\hat{\omega}_s)\tag{A.9}$$

$$\frac{dv_{Css}}{dt}=\frac{d(V_{Css}+\hat{v}_{Css})}{dt}=\frac{1}{C_s}(I_{ss}+\hat{i}_{ss})+(V_{Csc}\Omega_s+\Omega_s\hat{v}_{Csc}+V_{Csc}\hat{\omega}_s)\tag{A.10}$$

$$\frac{dv_{Csc}}{dt}=\frac{d(V_{Csc}+\hat{v}_{Csc})}{dt}=\frac{1}{C_s}(I_{sc}+\hat{i}_{sc})-(V_{Css}\Omega_s+\Omega_s\hat{v}_{Css}+V_{Css}\hat{\omega}_s)\tag{A.11}$$

$$\begin{aligned}\frac{dv_o}{dt}=\frac{d(V_o+\hat{v}_o)}{dt}=&\frac{2}{\pi C_o}(I_{sp}+\frac{I_{ss}}{I_{sp}}\hat{i}_{ss}+\frac{I_{sc}}{I_{sp}}\hat{i}_{sc})-\frac{1}{r_bC_o}(V_o+\hat{v}_o)\\&+\frac{1}{r_bC_o}(V_b+\hat{v}_b)\end{aligned}\tag{A.12}$$

$$\frac{di_{Li}}{dt}=\frac{d(I_{Li}+\hat{i}_{Li})}{dt}=\frac{1}{L_i}(V_i+\hat{v}_i)-\frac{1}{L_i}(DV_{Ci}+D\hat{v}_{Ci}+V_{Ci}\hat{d})\tag{A.13}$$

$$\frac{dv_{Ci}}{dt} = \frac{d(V_{Ci} + \hat{v}_{Ci})}{dt} = \frac{1}{C_i}(DI_{Li} + D\hat{i}_{Li} + I_{Li}\hat{d})$$
$$- (\frac{1}{\pi C_i} I_{ps} \sin \pi D + \frac{1}{\pi C_i} \sin \pi D \times \hat{i}_{ps} + \frac{1}{C_i} I_{ps} \cos \pi D \times \hat{d})$$

(A.14)

$$i_o = (I_o + \hat{i}_o) = \frac{1}{r_b}(V_o + \hat{v}_o) - \frac{1}{r_b}(V_b + \hat{v}_b) \qquad \text{(A.15)}$$

A.3 Steady-State Model Equations

In the steady-state equations can be derived by separating steady-state terms, upper-case letters, from (A.14)–(A.15), and then nullifying the derivative terms. The steady-state equations are given as follows

$$\frac{2V_i}{\pi D} \sin \pi D = -\Omega_s L_2 I_{pc} + \frac{8L_2}{\pi^2 L_m}(r_b + \frac{V_b}{I_o})I_{ss} + V_{Cps} + \frac{L_2}{L_m} V_{Css} \qquad \text{(A.16)}$$

$$\frac{2V_i}{\pi D} \sin \pi D = \frac{8L_m}{\pi^2 L_1}(r_b + \frac{V_b}{I_o})I_{ss} - \Omega_s L_m I_{sc} + V_{Cps} + \frac{L_m}{L_1} V_{Css} \qquad \text{(A.17)}$$

$$0 = \Omega_s L_1 I_{ss} + \frac{8}{\pi^2}(r_b + \frac{V_b}{I_o})I_{sc} + \frac{L_1}{L_m} V_{Cpc} + V_{Csc} \qquad \text{(A.18)}$$

$$0 = \Omega_s L_m I_{ps} + \frac{8}{\pi^2}(r_b + \frac{V_b}{I_o})\, I_{sc} + \frac{L_m}{L_2} V_{Cpc} + V_{Csc} \qquad \text{(A.19)}$$

$$0 = I_{pc} - \Omega_s C_p V_{Cps} \qquad \text{(A.20)}$$

$$0 = I_{sc} - \Omega_s C_s V_{Css} \qquad \text{(A.21)}$$

$$0 = I_{ps} + \Omega_s C_p V_{Cpc} \qquad \text{(A.22)}$$

$$0 = I_{ss} + \Omega_s C_s V_{Csc} \qquad \text{(A.23)}$$

$$0 = -\frac{1}{\pi}\sin \pi D \times I_{ps} + DI_{Li} \tag{A.24}$$

$$\frac{1}{D}V_i = V_{Ci} \tag{A.25}$$

$$r_b I_o + V_b = V_o \tag{A.26}$$

A.4 Small-Signal Model Equations

The small-signal equations can be derived by separating perturbation terms from (A.14)–(A.15). The small-signal equations are given as follows

$$\begin{aligned}\frac{d\hat{i}_{ps}}{dt} = {} & \Omega_s \hat{i}_{pc} - \frac{4}{\pi L_m}\frac{I_{sc}^2 V_o}{I_{sp}^3}\hat{i}_{ss} + \frac{4}{\pi L_m}\frac{I_{ss} I_{sc} V_o}{I_{sp}^3}\hat{i}_{sc} - \frac{1}{L_2}\hat{v}_{Cps} - \frac{1}{L_m}\hat{v}_{Css} \\ & + \frac{2}{\pi L_2}\sin \pi D \times \hat{v}_{Ci} - \frac{4}{\pi L_m}\frac{I_{ss}}{I_{sp}}\hat{v}_o + I_{pc}\hat{\omega}_s + \frac{2V_{Ci}}{L_2}\cos \pi D \times \hat{d}\end{aligned} \tag{A.26}$$

$$\begin{aligned}\frac{d\hat{i}_{ss}}{dt} = {} & -\frac{4}{\pi L_1}\frac{I_{sc}^2 V_o}{I_{sp}^3}\hat{i}_{ss} + (\frac{4}{\pi L_1}\frac{I_{ss} I_{sc} V_o}{I_{sp}^3} + \Omega_s)\hat{i}_{sc} - \frac{1}{L_m}\hat{v}_{Cps} - \frac{1}{L_1}\hat{v}_{Css} \\ & + \frac{2}{\pi L_m}\sin \pi D \times \hat{v}_{Ci} - \frac{4}{\pi L_1}\frac{I_{ss}}{I_{sp}}\hat{v}_o + I_{sc}\hat{\omega}_s + \frac{2V_{Ci}}{L_m}\cos \pi D \times \hat{d}\end{aligned} \tag{A.27}$$

$$\begin{aligned}\frac{d\hat{i}_{pc}}{dt} = {} & -\Omega_s \hat{i}_{ps} + \frac{4}{\pi L_m}\frac{I_{ss} I_{sc} V_o}{I_{sp}^3}\hat{i}_{ss} - \frac{4}{\pi L_m}\frac{I_{ss}^2 V_o}{I_{sp}^3}\hat{i}_{sc} - \frac{1}{L_2}\hat{v}_{Cpc} - \frac{1}{L_m}\hat{v}_{Csc} \\ & - \frac{4}{\pi L_m}\frac{I_{sc}}{I_{sp}}\hat{v}_o - I_{ps}\hat{\omega}_s\end{aligned} \tag{A.28}$$

$$\begin{aligned}\frac{d\hat{i}_{sc}}{dt} = {} & (\frac{4}{\pi L_1}\frac{I_{ss} I_{sc} V_o}{I_{sp}^3} - \Omega_s)\hat{i}_{ss} - \frac{4}{\pi L_1}\frac{I_{ss}^2 V_o}{I_{sp}^3}\hat{i}_{sc} - \frac{1}{L_m}\hat{v}_{Cpc} - \frac{1}{L_1}\hat{v}_{Csc} \\ & - \frac{4}{\pi L_1}\frac{I_{sc}}{I_{sp}}\hat{v}_o - I_{ss}\hat{\omega}_s\end{aligned} \tag{A.29}$$

$$\frac{d\hat{v}_{Cpc}}{dt} = \frac{1}{C_p}\hat{i}_{pc} - \Omega_s \hat{v}_{Cps} - V_{Cps}\hat{\omega}_s \tag{A.30}$$

$$\frac{d\hat{v}_{Csc}}{dt} = \frac{1}{C_s}\hat{i}_{sc} - \Omega_s \hat{v}_{Css} - V_{Css}\hat{\omega}_s \tag{A.31}$$

$$\frac{d\hat{v}_{Cps}}{dt} = \frac{1}{C_p}\hat{i}_{ps} + \Omega_s \hat{v}_{Cpc} + V_{Cpc}\hat{\omega}_s \tag{A.32}$$

$$\frac{d\hat{v}_{Css}}{dt} = \frac{1}{C_s}\hat{i}_{ss} + \Omega_s \hat{v}_{Csc} + V_{Csc}\hat{\omega}_s \tag{A.33}$$

$$\frac{d\hat{i}_{Li}}{dt} = \frac{1}{L_i}\hat{v}_i - \frac{1}{L_i}D\hat{v}_{Ci} - \frac{1}{L_i}V_{Ci}\hat{d} \tag{A.34}$$

$$\frac{d\hat{v}_{Ci}}{dt} = -\frac{1}{\pi C_i}\sin\pi D \times \hat{i}_{ps} + \frac{1}{C_i}D\hat{i}_{Li} + \frac{1}{C_i}(I_{Li} - I_{ps}\cos\pi D)\hat{d} \tag{A.35}$$

$$\frac{d\hat{v}_o}{dt} = \frac{2}{\pi C_o}\frac{I_{ss}}{I_{sp}}\hat{i}_{ss} + \frac{2}{\pi C_o}\frac{I_{sc}}{I_{sp}}\hat{i}_{sc} - \frac{1}{r_b C_o}\hat{v}_o + \frac{1}{r_b C_o}\hat{v}_b \tag{A.36}$$

$$\hat{i}_o = \frac{1}{r_b}\hat{v}_o - \frac{1}{r_b}\hat{v}_b \tag{A.37}$$

Appendix B. Detailed Parameter Calculation of 1.0-kW Active-clamped Half-bridge Boost Inverter based Inductive Wireless Charger

Minimum Duty Cycle

$$D = \frac{V_i}{0.7 \times V_{ds}(\max)} = \frac{150}{0.7 \times 650} = 0.329$$

***D* = 0.33** is selected.

Boost Inductor (*L_i*)

$$L_i \geq \frac{(1-D)V_i}{\Delta I_{Li} f_s} = \frac{(1-0.33) \times 150}{1 \times 85000} = 1.18 \text{ (mH)}$$

L_i = 1.36 mH is selected.

Mutual Inductance (*M*)

- ☐ The average clamping voltage

$$V_{Ci} = \frac{V_i}{D} = \frac{150}{0.33} = 454.54 \text{ (V)}$$

- ☐ The average input current

$$I_{Li} = \frac{P_o}{\eta V_i} = \frac{1000}{0.9 \times 150} = 7.41 \text{ (A)}$$

- ☐ The sine component magnitude of the primary current

$$I_{ps} = I_{Li}\frac{\pi D}{\sin \pi D} = 7.41\times\frac{\pi\times 0.33}{\sin\left(\pi\times 0.33\right)} = 8.92\ (\mathrm{A})$$

- The cosine component magnitude of the primary current, which is designed to obtain ZVS for S_1 and S_2

$$\begin{aligned} I_{pc} &\le \frac{I_{Li} + \Delta I_{Li}/2 - I_{ps}\cos\left(\pi D - 2\pi t_d/T_s\right)}{\sin\left(\pi D - 2\pi t_d/T_s\right)} \\ &= \frac{7.41 + 1/2 - 8.92\times\cos\left(\pi\times 0.33 - 2\pi\times 0.4\times 10^{-6}\times 85000\right)}{\sin\left(\pi\times 0.33 - 2\pi\times 0.4\mu\times 85000\right)} \\ &= 2.52\ (\mathrm{A}) \end{aligned}$$

$$\begin{aligned} I_{pc} &\le \frac{I_{Li} + \Delta I_{Li}/2 - (C_{oss1} + C_{oss2})V_{Ci}/t_d - I_{ps}\cos\left(\pi D\right)}{\sin\left(\pi D\right)} \\ &= \frac{7.41 + 1/2 - (600 + 600)\times 10^{-12}\times 454.54/\left(0.4\times 10^{-6}\right) - 8.92\cos\left(\pi\times 0.33\right)}{\sin\left(\pi\times 0.33\right)} \\ &= 2.33\ (\mathrm{A}) \end{aligned}$$

$$\begin{aligned} I_{pc} &\le -\frac{I_{Li} - \Delta I_{Li}/2 - I_{ps}\cos\left(\pi D + 2\pi t_d/T_s\right)}{\sin\left(\pi D + 2\pi t_d/T_s\right)} \\ &= -\frac{7.41 - 1/2 - 8.92\times\cos\left(\pi\times 0.33 + 2\pi\times 0.4\times 10^{-6}\times 85000\right)}{\sin\left(\pi\times 0.33 + 2\pi\times 0.4\mu\times 85000\right)} \\ &= -4.32\ (\mathrm{A}) \end{aligned}$$

$$\begin{aligned} I_{pc} &\le \frac{-I_{Li} + \Delta I_{Li}/2 - (C_{oss1} + C_{oss2})V_{Ci}/t_d + I_{ps}\cos\left(\pi D\right)}{\sin\left(\pi D\right)} \\ &= \frac{-7.41 + 1/2 - (600 + 600)\times 10^{-12}\times 454.54/\left(0.4\times 10^{-6}\right) + 8.92\cos\left(\pi\times 0.33\right)}{\sin\left(\pi\times 0.33\right)} \\ &= -4.34\ (\mathrm{A}) \end{aligned}$$

I_{pc} = – 7 A is selected.

- The mutual inductance

$$M = \frac{4V_b}{\pi\omega_s I_{pp}} = \frac{4V_b}{\pi\omega_s\sqrt{I_{ps}^2 + I_{pc}^2}} = \frac{4\times 72}{\pi\times 2\pi\times 85000\times\sqrt{8.92^2+7^2}} = 15.14\ (\mu\text{H})$$

The actual value of the mutual inductance is ***M* = 15 μH**.

Primary and Secondary Self-Inductance (L_p and L_s)

- The secondary self-inductance

$$L_s = \frac{Q_s R_{eq}}{\omega_0} = \frac{Q_s\left(\frac{8}{\pi^2}\frac{V_b^2}{P_o}\right)}{\omega_0} = \frac{4.4\times\left(\frac{8}{\pi^2}\frac{72^2}{1000}\right)}{2\pi\times 85000} = 34.62\ (\mu\text{H})$$

The actual value of the secondary self-inductance is **L_s = 35 μH**, and then the actual value of the secondary quality factor is **Q_s = 4.45**.

- The coupling coefficient

$$k \le \frac{\sqrt{4Q_s^2 - 1}}{2Q_s^2} = \frac{\sqrt{4\times 4.45^2 - 1}}{2\times 4.45^2} = 0.22$$

***k* = 0.15** is selected.

- The primary self-inductance

$$L_p = \frac{M^2}{k^2 L_s} = \frac{\left(15\times 10^{-6}\right)^2}{0.15^2\times 35\times 10^{-6}} = 285.71\ (\mu\text{H})$$

The actual value of the primary self-inductance is **L_p = 298 μH**, and then the actual value of the coupling coefficient is ***k* = 0.147**.

Primary and Secondary Compensation Capacitors (C_p and C_s)

- ☐ The secondary compensation capacitor

$$C_s = \frac{1}{\omega_s^2 L_s} = \frac{1}{\left(2\pi \times 85000\right)^2 \times 35 \times 10^{-6}} = 100.17 \text{ (nF)}$$

The actual value of the secondary compensation capacitor is **C_s = 100.2 nF**.

- ☐ The primary resonant frequency

$$\begin{aligned}\omega_p &= \sqrt{\omega_s^2 + \frac{I_{pc}\pi^2\omega_s^3 M^2 P_o}{8 I_{ps} L_p V_b^2}} \\ &= \sqrt{\left(2\pi \times 85000\right)^2 + \frac{(-7)\times\pi^2\times\left(2\pi\times 85000\right)^3\left(15\times 10^{-6}\right)^2\times 1000}{8\times 8.92\times 298\times 10^{-6}\times 72^2}} \\ &= 513567.19 \text{ (rad/s)}\end{aligned}$$

- ☐ The primary compensation capacitor

$$C_p = \frac{1}{\omega_p^2 L_p} = \frac{1}{\left(513567.19\right)^2 \times 298 \times 10^{-6}} = 12.72 \text{ (nF)}$$

The actual value of the primary compensation capacitor is **C_p = 12.9 nF**.

Clamping Capacitor (C_i)

$$C_i = 50 C_p = 50 \times 13 \times 10^{-9} = 0.65 \text{ (μF)}$$

C_i = 0.68 μF is selected.

Table B.1: Component specifications of the 1.0-kW active-clamped HBBI based IPT charger

Circuit configuration	Components	Part Number	Rating	Quantity
Active-clamped HHBI	SiC MOSFETs	Rohm SCT3060AL	650 V/39 A	2
Secondary rectifier	Schottky diodes	Microsemi APT100S20BG	200 V/120 A	4
Boost inductor (L_i)	Unshielded toroidal inductors	Wurth Elektronik 750343810	340 μH/15 A	4 × 340 μH
Clamping capacitor (C_i)	Metallized polypropylene film capacitor	Wurth Elektronik WCAP-FTXX 890334026020	0.68 μF/300 VAC/ 630 VDC	1
Primary compensation capacitor (C_p)	Metallized polypropylene film capacitors	TDK B32652A2472K000	4.7 nF/700 VAC/ 2000 VDC	11 × 4.7 nF/4
Secondary compensation capacitor (C_s)	Metallized polypropylene film capacitors	TDK B32652A2472K000 & TDK B32652A2152J000	4.7 nF/700 VAC/ 2000 VDC 1.5 nF/700 VAC/ 2000 VDC	21 × 4.7 nF + 1 × 1.5 nF
Output capacitor (C_o)	Metallized polypropylene film capacitors	Kemet C4DEFPQ6260A 8TK	260 μF/600 VDC	2 × 260 μF
Gate driver	Gate driver power management evaluation boards	Texas Instruments UCC5390SCDEV M-010	+18 V/-4 V/0.8 W	2

Appendix C. All-switch ZVS Operation of Direct AC/AC Active-clamped Half-bridge Converter Based Inductive Wireless Charger

Since only the duty cycle d_p of the primary AC/AC converter is manipulated for the input current and charging current regulation, the switches of the proposed AC/AC converter cannot achieve ZVS in the whole line cycle, especially the lower switches. In order to simplify the ZVS analysis, the output parasitic capacitors of the switches are assumed small and ignorable. Due to the symmetry of the configuration and operation of the charging system, only the ZVS of the switches during the positive half cycle of the line voltage are derived in detail. Similarly, their ZVS operation during the negative half cycle of the line voltage can be analyzed.

As demonstrated in Chapter 6 and 7, the ZVS condition for the switches of the secondary rectifier is that the secondary current i_s must lead the secondary voltage v_s, $0 < \theta < \pi/2$. However, in order to minimize the VA rating of the primary and secondary converters, the θ should be slightly less than $\pi/2$. For the primary AC/AC converter, according to Section 4.4 in Chapter 4, during the positive half line cycle, S_{p1a} can be turned on with ZVS if it is activated at $i_p < i_i$. On the other hand, S_{p2a} can be turned on with ZVS if it is activated at $i_p > i_i$. As shown in Figure C.1, the ZVS conditions of S_{p1a} and S_{p2a} during the positive half line cycle can be formulated as (C.1) and (C.2), respectively.

$$i_p\left(T_s/4 - d_pT_s/2 + t_d\right) \le i_i + \Delta i_i \tag{C.1}$$

$$i_p\left(T_s/4 + d_pT_s/2 + t_d\right) \ge i_i - \Delta i_i \tag{C.2}$$

where $i_p(t) = \frac{2V_b}{\pi\omega_s M}\sin(\omega_s t + \theta - \pi/2)$, $i_i = \frac{2V_b \sin\theta}{\pi\omega_s M}\frac{\sin\pi d_p}{\pi d_p}$, $\Delta i_i = \frac{(1-d_p)v_i}{L_i f_s}$,

and t_d is the dead time.

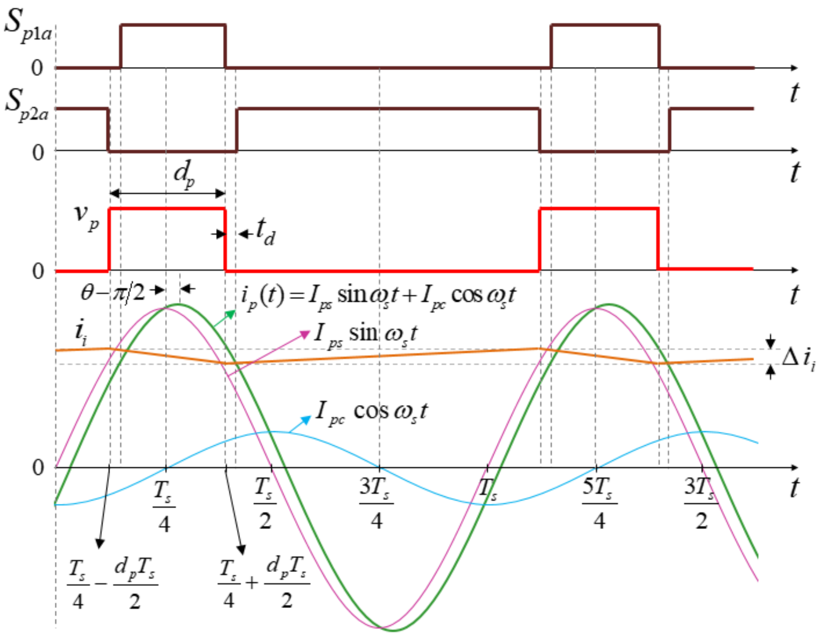


Figure C.1: Key operating waveforms on the primary side.

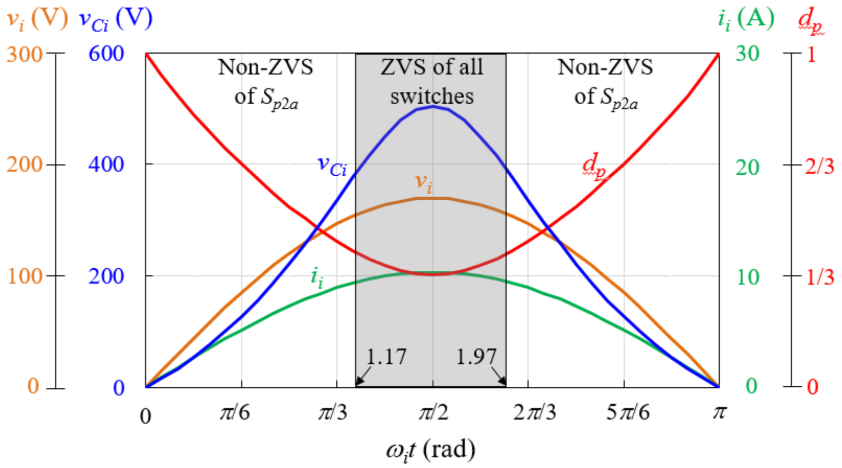
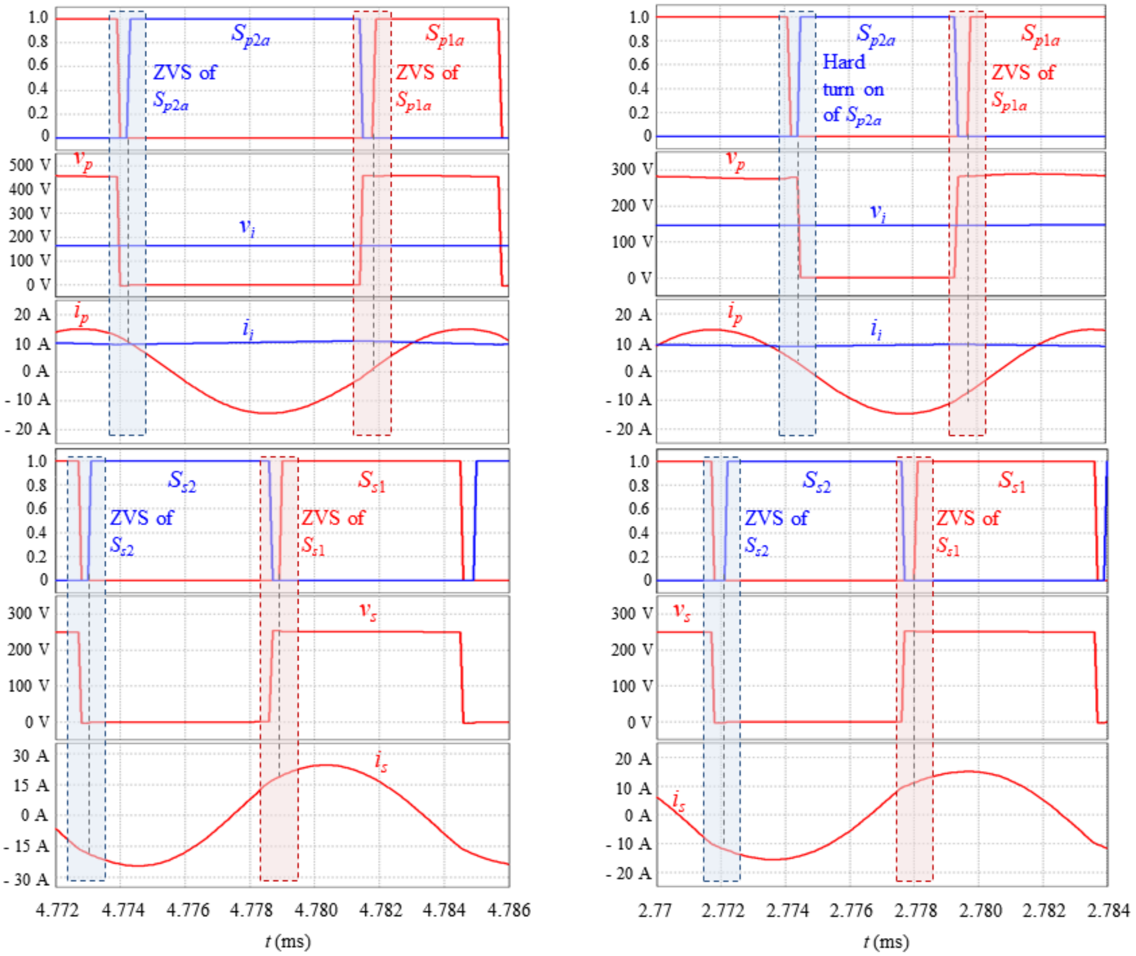


Figure C.2: All-switch ZVS operation region of the charging system at $\theta = 60^{\circ}$, $V_b = 250$ V and $I_b = 3.5$ A during the positive half line cycle.

For the charging system given in Table 7.1 in Chapter 7, $\theta = 80^0$ is selected, the lower switches of the AC/AC converter, S_{p2a} and S_{p2b}, always suffer hard turn-on and hard turn-off while the other switches are operated with ZVS. However, when θ reduces to 60^0 with $t_d = 0.4$ μs, the ZVS for the all the switches of the charging system can be achieved in the certain areas over the line cycle. The theoretical all-switch ZVS region of the charging system at $\theta = 60^0$, $V_b = 250$ V and $I_b = 3.5$ A during the positive half line cycle is depicted in Figure C.2. It can be observed that the ZVS region (shaded areas, 1.17 rad $\leq \omega_l t \leq$ 1.97 rad) is constrained by the ZVS condition (C.2) of the lower switch S_{p2a}. The ZVS of S_{p2a} cannot be maintained in the whole line cycle, especially in the low grid voltage area.

Figure C.3 shows the simulation waveforms verifying the ZVS of the switches in the charging system. At $\omega_l t = 1.8$ rad, the primary and secondary voltages are unchanged when the switches are turned on as shown in Figure C.3 (a). Therefore, all the switches are operated with ZVS. On the other hand, at $\omega_l t = \pi/3$ rad, the primary voltage v_p changes its status whenever S_{p2a} is turned on or turned off, so it loses ZVS as shown in Figure C.3 (b), which agrees with the theoretical analysis.



(a)

(b)

Figure C.3: Simulation waveforms of ZVS verification at $\theta = 60^{\circ}$, V_b = 250 V and I_b = 3.5 A. (a) $\omega_l t$ = 1.8 rad. (b) $\omega_l t = \pi/3$ rad.

Appendix D. Detailed Parameter Calculation of 1.0-kW Direct AC/AC Active-clamped Half-bridge Converter Based Inductive Wireless Charger

Minimum Duty Cycle

$$D_{pm} = \frac{V_m}{V_{cm}} = \frac{120\sqrt{2}}{600} = 0.282$$

D_{pm} **= 0.28** is selected.

Boost Inductor (L_i)

$$L_i \geq \frac{\left(1-D_{pm}\right)V_m}{\Delta I_m f_s} = \frac{\left(1-0.28\right)\times 120\sqrt{2}}{2\times 85000} = 0.72 \text{ (mH)}$$

L_i **= 1.02 mH** is selected.

Mutual Inductance (M)

- ☐ The input current peak

$$I_m = \frac{2P_o}{\eta V_m} = \frac{2\times 1000}{0.9\times 120\sqrt{2}} = 13.09 \text{ (A)}$$

- ☐ The mutual inductance

$$M = \frac{2V_b \sin\theta}{\pi\omega_s I_m}\frac{\sin\pi D_{pm}}{\pi D_{pm}} = \frac{2\times 250\times \sin 80^o}{\pi\times 2\pi\times 85000\times 13.09}\frac{\sin\left(\pi\times 0.28\right)}{\pi\times 0.28} = 19.64 \text{ (μH)}$$

The actual value of the mutual inductance is M **= 20.6 μH**.

Primary and Secondary Self-Inductance (L_p and L_s)

The inductive coupling coils are designed to obtained the desired mutual inductance at the air gap of 170 mm. The primary and secondary self-inductance values are **297.2 μH** and **52.8 μH**, respectively.

Primary and Secondary Compensation Capacitors (*C_p* and *C_s*)

☐ The primary compensation capacitor

$$C_p = \frac{1}{\omega_s^2 L_p} = \frac{1}{\left(2\pi \times 85000\right)^2 \times 297.2 \times 10^{-6}} = 11.8\ (\text{nF})$$

The actual value of the primary compensation capacitor is ***C_p* = 11.88 nF**.

☐ The secondary compensation capacitor

$$C_s = \frac{1}{\omega_s^2 L_s} = \frac{1}{\left(2\pi \times 85000\right)^2 \times 52.8 \times 10^{-6}} = 66.4\ (\text{nF})$$

The actual value of the secondary compensation capacitor is ***C_s* = 66.3 nF**.

Clamping Capacitor (*C_i*)

$$C_i = \frac{2I_{pp}}{\omega_s \Delta V_c} = \frac{\dfrac{4V_b}{\pi \omega_s M}}{\omega_s \Delta V_c} = \frac{\dfrac{4 \times 250}{\pi \times 2\pi \times 85000 \times 20.6 \times 10^{-6}}}{2\pi \times 85000 \times 20} = 2.7\ (\mu\text{F})$$

***C_i* = 3.3 μH** is selected.

Table D.1: Component specifications of the 1.0-kW AC/AC active-clamped HB converter based IPT charger

Circuit configuration	**Components**	**Part Number**	**Rating**	**Quantity**
Active-clamped HHBI	SiC MOSFETs	Cree C2M0040120D	1200 V/60 A	4
Secondary rectifier	SiC MOSFETs	Rohm SCT3060AL	650 V/39 A	2
Boost inductor (L_i)	Unshielded toroidal inductors	Wurth Elektronik 750343810	340 μH/15 A	3 (series)
Clamping capacitor (C_i)	Metallized polypropylene film capacitor	Vishay F340X153348MPP2T0	3.3 μF/480 VAC/ 800 VDC	1 × 3.3 μF
Primary compensation capacitor (C_p)	Metallized polypropylene film capacitors	TDK B32652A2472K000 & TDK B32652A2332J000	4.7 nF/700 VAC/ 2000 VDC 3.3 nF/700 VAC/ 2000 VDC	8 × 4.7 nF/4 + 3 × 3.3 nF/4
Secondary compensation capacitor (C_s)	Metallized polypropylene film capacitors	TDK B32652A2472K000 & TDK B32652A2332J000	4.7 nF/700 VAC/ 2000 VDC 3.3 nF/700 VAC/ 2000 VDC	12 × 4.7 nF + 3 × 3.3 nF
Output capacitor (C_o)	Metallized polypropylene film capacitors	Kemet C4DEFPQ6260A8TK	260 μF/600 VDC	2 (parallel)
Gate driver	Gate driver power management evaluation boards	Texas Instruments UCC5390SCDEVM-010	+18 V/-4 V/0.8 W	6

Appendix E. Duty Cycle–to–Input Current Transfer Function Derivation of Direct AC/AC Active-clamped Half-bridge Converter Based Inductive Wireless Charger

In this Appendix, the derivation of the duty cycle-to-input current transfer function of the direct AC/AC active-clamped half-bridge converter based IPT charging system will be provided in detail. Figure E.1 shows the equivalent circuit of the AC/AC conversion stage and its typical waveforms during the positive half line cycle. In order to simplify the analysis, some assumptions are made as follows:

1) The switching frequency is much higher than the line frequency, the input voltage v_i can be considered as constant over a switching period;

2) All switches and diodes are ideal;

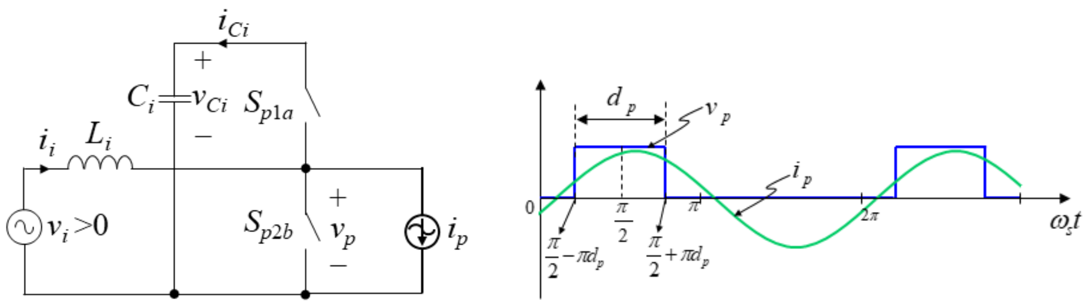
3) The dead time is neglected;

4) Parasitic resistances of inductors, capacitors and coils are ignorable;

5) Boost inductor L_i is sufficiently large to maintain a constant low-ripple input current over a switching period;

6) Clamping capacitor C_i is sufficiently large to maintain constant clamping voltage over a switching period;

7) Primary current i_p is nearly sinusoidal.



(a) (b)

Figure E.1: (a) Equivalent circuit of AC/AC conversion stage, and (b) Its typical waveforms over the positive half line cycle.

During the turn-on period of S_{p1a} with duty cycle d_p, the nonlinear state equations are given by

$$\frac{di_i}{dt} = \frac{1}{L_i}\left(v_i - v_{Ci}\right) \tag{E.1}$$

$$\frac{dv_{Ci}}{dt} = \frac{1}{C_i}\left(i_i - i_p\right) \tag{E.2}$$

where i_p is given by (6.10).

During the turn-off period of S_{p1a}, the nonlinear state equations are given as follows

$$\frac{di_i}{dt} = \frac{v_i}{L_i} \tag{E.3}$$

$$\frac{dv_{Ci}}{dt} = 0 \tag{E.4}$$

The input current (i_i) and clamping voltage (v_{Ci}) are approximated to DC values over a switching period, thus their average rate of change over a full switching period can be derived as follows:

$$\begin{aligned}\frac{di_i}{dt} &= \frac{1}{2\pi L_i}\left[\int_{\frac{\pi}{2}-\pi d_p}^{\frac{\pi}{2}+\pi d_p}(v_i - v_{Ci})d\omega_s t + \int_{0}^{\frac{\pi}{2}-\pi d_p} v_i d\omega_s t + \int_{\frac{\pi}{2}+\pi d_p}^{2\pi} v_i d\omega_s t\right] \\ &= \frac{1}{L_i}v_i - \frac{1}{L_i}d_p v_{Ci}\end{aligned} \tag{E.5}$$

$$\frac{dv_{Ci}}{dt} = \frac{1}{2\pi C_i}\left[\int_{\frac{\pi}{2}-\pi d_p}^{\frac{\pi}{2}+\pi d_p}(i_i - i_p)d\omega_s t\right] = \frac{1}{C_i}i_i d_p - \frac{1}{\pi C_i}I_{ps}\sin\pi d_p \tag{E.6}$$

where $I_{ps} = \dfrac{2V_b \sin\pi d_s \sin\theta}{\pi\omega_s M}$.

The nonlinear differential equations (E.5) and (E.6) contain the steady-state and small-signal model of the AC/AC conversion stage. The steady-state equations are given as

$$i_i = I_{ps}\frac{\sin\pi d_p}{\pi d_p} \tag{E.7}$$

$$v_{Ci} = \frac{v_i}{d_p} \tag{E.8}$$

By perturbing and linearizing (E.5) and (E.6), the small small-signal equations can be obtained as

$$\frac{d\hat{i}_i}{dt} = \frac{1}{L_i}\hat{v}_i - \frac{d_p}{L_i}\hat{v}_{Ci} - \frac{v_{Ci}}{L_i}\hat{d}_p \tag{E.9}$$

$$\frac{d\hat{v}_{Ci}}{dt} = \frac{D_p}{C_i}\hat{i}_i + \frac{1}{C_i}\left(i_i - I_{ps}\cos\pi d_p\right)\hat{d}_p \tag{E.10}$$

The duty cycle-to-input current transfer function can be derived by rearranging (E.9) and (E.10) in the state-space matrix representation, and then taking the Laplace transform

$$\frac{i_i(s)}{d_p(s)} = -\frac{v_{Ci}}{L_i}\frac{s + K_p d_p / v_{Ci}}{s^2 + d_p^2 / L_i C_i} \tag{E.11}$$

where $K_p = \frac{1}{C_i}\left(i_i - I_{ps}\cos\pi d_p\right)$.

Similarly, the duty cycle-to-input current transfer function during the negative half line cycle can be derived as

$$\frac{i_i(s)}{d_p(s)} = -\frac{v_{Ci}}{L_i}\frac{s + K_n d_p / v_{Ci}}{s^2 + d_p^2 / L_i C_i} \tag{E.12}$$

where $K_n = \frac{1}{C_i}\left(i_i + I_{ps}\cos\pi d_p\right)$.

It can be seen that the transfer functions (E.11) and (E.12) contain RHP zeros when the direct AC/AC active-clamped HB converter based IPT system is operated in the V2G mode.

Appendix F. Classification and Current Harmonic Limits in IEC 61000-3-2

Table F.1: Classification of IEC 61000-3-2

Classes	Applications
A	• Balanced three-phase equipment • Household appliances excluding equipment identified as class D • Tools, excluding portable tools • Dimmers for incandescent lamps • Audio equipment • Other equipment, except that stated in classes B, C, and D
B	• Portable tools • Arc welding equipment which is not professional equipment
C	• Lighting equipment
D	• PCs, PC monitors, radio, or TV receivers with Input power P ≤ 600W • Refrigerators and freezers having one or more variable-speed drives (VDS) to control compressor motor(s)

Table F.2: Current harmonic limits for class A equipment

Harmonic orders ***n***		**Maximum permissible harmonic current** **(A)**
Odd harmonics	3	2.30
	5	1.14
	7	0.77
	9	0.40
	11	0.33
	13	0.21
	$15 \leq n \leq 39$	$0.15 \times 15/n$
Even harmonics	2	1.08
	4	0.43
	6	0.30
	$8 \leq n \leq 40$	$0.23 \times 8/n$

Table F.3: Current harmonic limits for class B equipment

Harmonic orders **n**		**Maximum permissible harmonic current** **(A)**
Odd harmonics	3	2.30×1.5
	5	1.14×1.5
	7	0.77×1.5
	9	0.40×1.5
	11	0.33×1.5
	13	0.21×1.5
	$15 \leq n \leq 39$	$0.15 \times 15/n \times 1.5$
Even harmonics	2	1.08×1.5
	4	0.43×1.5
	6	0.30×1.5
	$8 \leq n \leq 40$	$0.23 \times 8/n \times 1.5$

Table F.4: Current harmonic limits for class C equipment

Harmonic orders n	**Maximum permissible harmonic current expressed as the percentage of the input current at the fundamental frequency (%)**
2	2
3	30 × PF (PF is the circuit power factor)
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonic only)	3

Table F.5: Current harmonic limits for class D equipment

Harmonic orders n	**Maximum permissible harmonic current per watt (mA/W)**	**Maximum permissible harmonic current (A)**
3	3.40	2.30
5	1.90	1.14
7	1.00	0.77
9	0.50	0.40
11	0.35	0.33
$13 \leq n \leq 39$ (odd harmonic only)	$3.85/n$	See Table F.2

Appendix G. Printed Circuit Board of Direct AC/AC Active-clamped Half-bridge Converter

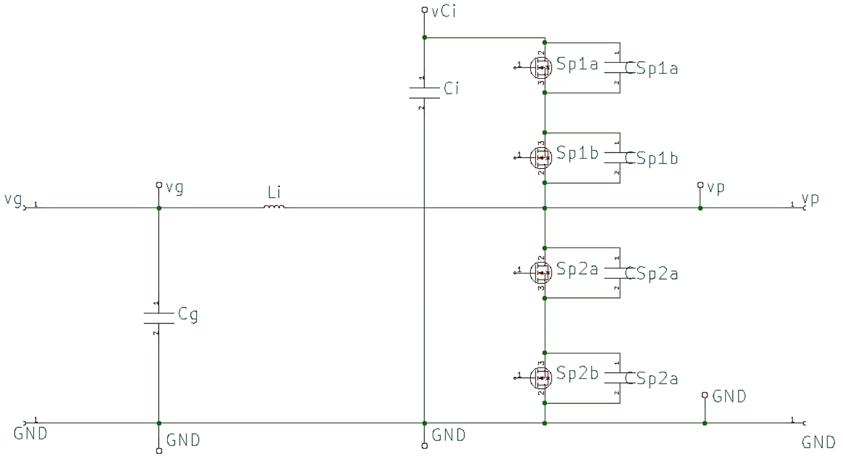


Figure G.1: Schematic diagram of the direct AC/AC active-clamped half-bridge converter.

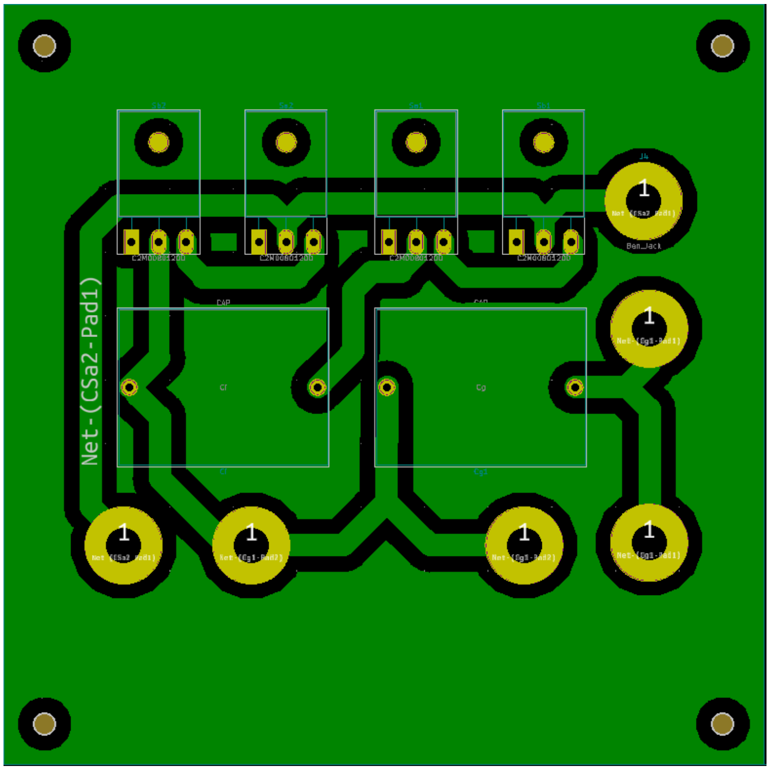


Figure G.2: PCB layout of the direct AC/AC active-clamped half-bridge converter.

Appendix H. Publications

Journals

- **P. S. Huynh** and S. S. Williamson, "Analysis and design of soft-switching active clamping half-bridge boost inverter for inductive wireless charging applications," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 1027-1039, Dec. 2019.

- **P. S. Huynh**, D. Ronanki, D. Vincent, and S. S. Williamson "Overview and comparative assessment of single-phase power converter topologies of inductive wireless charging systems," *Energies.* (Accepted)

- **P. S. Huynh**, D. Ronanki, D. Vincent, and S. S. Williamson "Direct AC-AC active-clamped half-bridge converter for inductive charging applications," *IEEE Trans. Power Electron.* (Early Access)

- D. Vincent, **P. S. Huynh**, L. Patnaik, David Capano, and S.S. Williamson, "Accelerating the autonomous electric transportation revolution: Wireless charging and advanced battery management systems" *IEEE Transportation Electrification Community (TEC)*, e-newsletter, Feb.2018.

- I. U. Castillo-Zamora, **P. S. Huynh**, D. Vincent, F. J. Perez-Pinal, M. A. Rodriguez-Licea, and S. S. Williamson, "Hexagonal geometry coil for a WPT high-power fast charging application," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 946-956, Dec. 2019.

- D. Vincent, **P. S. Huynh**, N. A. Azeez, L. Patnaik and S. S. Williamson, "Evolution of hybrid inductive and capacitive AC links for wireless EV charging—A comparative overview," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 1060-1077, Dec. 2019.

Conferences

- **P. S. Huynh**, D. Vincent, L. Patnaik, and S. S. Williamson, "FPGA-based PWM implementation of matrix converter in inductive wireless power transfer systems," *2018 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (Wow),* Montréal, QC, 2018, pp. 1-6.

- **P. S. Huynh**, D. Vincent, N. Abdul Azeez, L. Patnaik, and S. S. Williamson, "Performance analysis of a single-stage high-frequency AC-AC buck converter for a series-series compensated inductive power transfer system," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, 2018, pp. 347-352.

- **P. S. Huynh** and S. S. Williamson, "A soft-switched active clamped half-bridge current source inverter for wireless inductive power transfer," *2019 IEEE Energy Conversion Congress and Exposition (ECCE),* Baltimore, MD, USA, 2019, pp. 2129-2134.

- **P. S. Huynh** and S. S. Williamson, "An inductive power transfer system using soft-switched AC/AC active-clamped half-bridge converter with predictive dead-beat grid current control," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. (Accepted)

- D. Vincent, **P. S. Huynh**, and S. S. Williamson, "A novel three leg inverter for high power hybrid inductive and capacitive wireless power transfer system," *IECON*

2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 1544-1548.

- D. Vincent, S. Chakraborty, **P. S. Huynh**, and S. S. Williamson, “Efficiency analysis of a 7.7kW inductive wireless power transfer system with parallel displacement,” *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Hamilton, 2018, pp. 409-414.

Book chapter

- S. S. Williamson, D. Vincent, A. V. J. S. Praneeth, and **P. S. Huynh**, “Charging strategies for electrified transport” in Advances in Carbon Management Technologies, *CRC press*. (Accepted)

- **P. S. Huynh**, D. Ronanki, S. S. Williamson, “Power electronics for wireless charging of future electric vehicles” in Emerging power converters for renewable energy and electric vehicles, *CRC press.* (Accepted)

Bibliography

[1] M. G. L. Roes, J. L. Duarte, M. A. M. Hendrix, and E. A. Lomonova, "Acoustic energy transfer: A review," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 242-248, Jan. 2013.

[2] Y. Hu, X. Zhang, J. Yang, and Q. Jiang, "Transmitting electric energy through a metal wall by acoustic waves using piezoelectric transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control,* vol. 50, no. 7, pp. 773-781, July 2003.

[3] E. Y. Chow, "Wireless powering and the study of RF propagation through ocular tissue for development of implantable sensors," *IEEE Trans. Antennas Propag.*, vol. 59, no. 6, pp. 2379–2387, Jun 2011.

[4] S. Sasaki, K. Tanaka, and K. i. Maki, "Microwave power transmission technologies for solar power satellites," in *Proc. IEEE*, June 2013, vol. 101, no. 6, pp. 1438-1447.

[5] N. Wang *et al.*, "One-to-multipoint laser remote power supply system for wireless sensor networks," *IEEE Sensors J.,* vol. 12, no. 2, pp. 389–396, Feb. 2012.

[6] A. Sahai and D. Graham, "Optical wireless power transmission at long wavelengths," in *Proc. International Conference on Space Optical Systems and Applications*, Santa Monica, CA, 2011, pp. 164-170.

[7] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "Capacitive power transfer for contactless charging," presented at the Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC), Fort Worth, TX, 2011.

[8] G. A. Covic and J. T. Boys, "Inductive Power Transfer," in *Proc. IEEE*, 2013, vol. 101, no. 6, pp. 1276–1289.

[9] J. L. Villa, J. Sallan, J. F. S. Osorio, and A. Llombart, "High-misalignment tolerant compensation topology for ICPT systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 945–951, Feb. 2012.

[10] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A double-sided LCLC-compensated capacitive power transfer system for electric vehicle charging," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6011–6014, Nov. 2015.

[11] A. Kumar, S. Sinha, A. Sepahvand, and K. Afridi, "Improved design optimization for high-efficiency matching networks," *IEEE Trans. Power Electron.*, pp. 1-1, 2017.

[12] A. Sanni, A. Vilches, and C. Toumazou, "Inductive and ultrasonic multi-tier interface for low-power, deeply implantable medical devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 297-308, Aug. 2012.

[13] S. Shin, M. Choi, S. Jung, H. Lee, and G. Cho, "A time-interleaved resonant voltage mode wireless power receiver with delay-based tracking loops for implantable medical devices," *IEEE J. Solid-State Circuits,* vol. 55, no. 5, pp. 1374-1385, May 2020.

[14] D. Li, Y. Zhou, Y. Cui, S. Huang, and D. Deng, "A wireless power transmission system with load regulation for implantable devices," *IEEE Instrum. Meas. Mag.*, vol. 23, no. 4, pp. 68-76, 2020.

[15] S. Y. R. Hui and W. W. C. Ho, "A new generation of universal contactless battery charging platform for portable consumer electronic equipment," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 620-627, May 2005.

[16] X. Liu and S. Y. Hui, "Simulation study and experimental verification of a universal contactless battery charging platform with localized charging features," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2202-2210, Nov. 2007.

[17] C. G. Kim, D. H. Seo, J. S. You, J. H. Park, and B. H. Cho, "Design of a contactless battery charger for cellular phone," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1238-1247, Dec. 2001.

[18] B. Choi, J. Nho, H. Cha, T. Ahn, and S. Choi, "Design and implementation of low-profile contactless battery charger using planar printed circuit board windings as energy transfer device," *IEEE Trans. Ind. Electron.*, vol. 51, no. 1, pp. 140-147, Feb. 2004.

[19] M. P. Kazmierkowski and A. J. Moradewicz, "Unplugged but connected: Review of contactless energy transfer systems," *IEEE Ind. Electron. Mag.*, vol. 6, no. 4, pp. 47-55, Dec. 2012.

[20] V. Cirimele, M. Diana, F. Freschi, and M. Mitolo, "Inductive power transfer for automotive applications: State-of-the-art and future trends," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4069-4079, Sept.-Oct. 2018.

[21] (2019). DRIVE 11 evaluation system: Wireless charging for EV & PHEV platforms [Online]. Available: https://witricity.com/wp-content/uploads/2019/11/DRIVE 11_20191104-1.pdf

[22] (2018). From wireless to dynamic electric vehicle charging: The evolution of Qualcomm Halo [Online]. Available: https://www.qualcomm.com/news/onq/2017/05/18/wireless-dynamic-ev-charging-evolution-qualcomm-halo

[23] (2016). 2nd generation plugless technical specifications [Online]. Available: https://www.pluglesspower.com/gen2-tech-specs/

[24] (2014). ICS - Inductive charging system ICS115 [Online]. Available: https://www.brusa.biz/fileadmin/Diverses/Download/Datenblaetter/BRUSA_DB_EN_ICS115.pdf

[25] (2019). Momentum Dynamics - Fully automated inductive charging for all types of electric buses [Online]. Available: https://www.tesc.psu.edu/assets/docs/momentum-dynamics-wireless-vehicle-charging.pdf

[26] (2019). J2954: Wireless power transfer for light-duty plug-in/electric vehicles and alignment methodology - SAE International [Online]. Available: http://standards.sae.org/wip/j2954/

[27] (2017). J1772: SAE electric vehicle and plug in hybrid electric vehicle conductive charge coupler - SAE International [Online]. Available: https://www.sae.org/standards/content/j1772_201710/

[28] (2015). IEC 61980-1: Electric vehicle wireless power transfer (WPT) systems - Part 1: General requirements, IEC Std. [Online]. Available: https://webstore.iec.ch/publication/22951

[29] (2020). ISO/PAS 19363:2020: Electrically propelled road vehicles - Magnetic field wireless power transfer - Safety and interoperability requirements, ISO Std. [Online]. Available: https://www.iso.org/standard/73547.html

[30] (2019). Canadian environmental sustainability indicators: Greenhouse gas missions [Online]. Available: https://www.canada.ca/content/dam/eccc/documents/pdf/cesindicators/ghg-emissions/2019/national-GHG-emissions-en.pdf

[31] (2020). The 2020 fuel consumption guide [Online]. Available: https://www.nrcan.gc.ca/sites/www.nrcan.gc.ca/files/oee/pdf/transportation/tools/fuelratings/2020%20Fuel%20Consumption%20Guide.pdf

[32] (2019). Canada’s energy future 2019 [Online]. Available: https://www.cer-rec.gc.ca/nrg/ntgrtd/ftr/2019/2019nrgftr-eng.pdf

[33] (2020). Canada’s long-term infrastructure plan [Online]. Available: https://www.infrastructure.gc.ca/alt-format/pdf/plan/icp-pic/IC-InvestingInCanadaPlan-ENG.pdf

[34] (2019). Nissan LEAF first electric car to pass 400,000 sales [Online]. Available: https://global.nissannews.com/en/releases/release-5227ef5dbab9f1e0871062f0c003e618-nissan-leaf-first-electric-car-to-pass-400k-sales

[35] D. Vincent, P. S. Huynh, L. Patnaik, D. Capano, and S. S. Williamson, "Accelerating the autonomous electric transportation revolution: Wireless charging and advanced battery management systems," *IEEE Transport. Electrific. Community (TEC)*, e-newsletter, 2018.

[36] A. Khaligh and S. Dusmez, "Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3475-3489, Oct. 2012.

[37] C. S. Wang, O. H. Stielau, and G. A. Covic, "Design considerations for acontactless electric vehicle battery charger," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1308–1314, Oct. 2005.

[38] S. Y. R. Hui and W. W. C. Ho, "A new generation of universal contactless battery charging platform for portable consumer electronic equipment," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 620–627, May 2005.

[39] A. Daga, J. M. Miller, B. R. Long, R. Kacergis, P. Schrafel, and J. Wolgemuth, "Electric fuel pumps for wireless power transfer: Enabling rapid growth in the electric vehicle market," *IEEE Power Electron. Mag.*, vol. 4, no. 2, pp. 24-35, June 2017.

[40] R. Bosshard and J. W. Kolar, "Inductive power transfer for electric vehicle charging: Technical challenges and tradeoffs," *IEEE Power Electron. Mag.*, vol. 3, no. 3, pp. 22-30, Sept. 2016.

[41] S. Y. Choi, B. W. Gu, S. Y. Jeong, and C. T. Rim, "Advances in wireless power transfer systems for roadway-powered electric vehicles," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 1, pp. 18–36, Mar. 2015.

[42] A. Ahmad, M. S. Alam, and R. Chabaan, "A comprehensive review of wireless charging technologies for electric vehicles," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 38-63, March 2018.

[43] C. C. Mi, G. Buja, S. Y. Choi, and C. T. Rim, "Modern advances in wireless power transfer systems for roadway powered electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6533-6545, Oct. 2016.

[44] S. A. Birrell, D. Wilson, C. P. Yang, G. Dhadyalla, and P. Jennings, "How driver behaviour and parking alignment affects inductive charging systems for electric vehicles," *Transportation Research Part C Emerging Technololgy,* vol. 58, no. PD, pp. 721–731, 2015.

[45] G. A. Covic and J. T. Boys, "Modern trends in inductive power transfer for transportation applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 1, pp. 28-41, Mar. 2013.

[46] F. Musavi and W. Eberle, "Overview of wireless power transfer technologies for electric vehicle battery charging," *IET Power Electron.*, vol. 7, no. 1, pp. 60-66, Jan. 2014.

[47] C. Panchal, S. Stegen, and J. Lu, "Review of static and dynamic wireless electric vehicle charging system," *Eng. Sci. Technol. Int. J.*, vol. 21, no. 5, pp. 922-937, 2018.

[48] A. A. S. Mohamed, C. R. Lashway, and O. Mohammed, "Modeling and feasibility analysis of quasi-dynamic WPT system for EV applications," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 2, pp. 343–353, Jun. 2017.

[49] S. Lukic and Z. Pantic, "Cutting the cord: Static and dynamic inductive wireless charging of electric vehicles," *IEEE Electrific. Mag.*, vol. 1, no. 1, pp. 57-64, Sept. 2013.

[50] J. M. M. e. al., "Demonstrating dynamic wireless charging of an electric vehicle: The benefit of electrochemical capacitor smoothing," *IEEE Power Electron. Mag.*, vol. 1, no. 1, pp. 12–24, Mar. 2014.

[51] V. Cirimele *et al.*, "The fabric ICT platform for managing wireless dynamic charging road lanes," *IEEE Trans. Veh. Technol.*, vol. 69, no. 3, pp. 2501-2512, Mar. 2020.

[52] G. Guidi, A. M. Lekkas, J. E. Stranden, and J. A. Suul, "Dynamic wireless charging of autonomous vehicles: Small-scale demonstration of inductive power transfer as

an enabling technology for self-sufficient energy supply," *IEEE Electrific. Mag.*, vol. 8, no. 1, pp. 37-48, March 2020.

[53] L. Siqi and C. C. Mi, "Wireless power transfer for electric vehicle applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 4-17, Mar. 2015.

[54] A. A. S. Mohamed, L. Zhu, A. Meintz, and E. Wood, "Planning optimization for inductively charged on-demand automated electric shuttles project at Greenville, South Carolina," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1010-1020, 2020.

[55] Y. D. Ko and Y. J. Jang, "The optimal system design of the online electric vehicle utilizing wireless power transmission technology," *IEEE Trans. Intell. Transp. Syst.*, vol. 14, no. 3, pp. 1255-1265, Sept. 2013.

[56] D. Patil, M. K. McDonough, J. M. Miller, B. Fahimi, and P. T. Balsara, "Wireless power transfer for vehicular applications: Overview and challenges," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 3-37, Mar. 2018.

[57] Z. Zhang, H. Pang, A. Georgiadis, and C. Cecati, "Wireless power transfer - An overview," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2018.2835378.

[58] S. Li, Z. Liu, H. Zhao, L. Zhu, and Z. Chen, "Wireless power transfer by electric field resonance and its application in dynamic charging," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6602-6612, 2016.

[59] K. Aditya and S. S. Williamson, "Design guidelines to avoid bifurcation in a series-series compensated inductive power transfer system," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2018.2851953.

[60] C. T. Rim and C. Mi, "Coupled coil model," in *Wireless power transfer for electric vehicles and mobile devices*: IEEE, 2017, pp. 53-65.

[61] C. S. Wang, O. H. Stielau, and G. A. Covic, "Design considerations for a contactless electric vehicle battery charger," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1308–1314, Oct. 2005.

[62] T. D. Yeo, D. Kwon, S. T. Khang, and J. W. Yu, "Design of maximum efficiency tracking control scheme for closed-loop wireless power charging system employing series resonant tank," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 471-478, 2017.

[63] K. Aditya and S. S. Williamson, "A review of optimal conditions for achieving maximum power output and maximum efficiency for a series–series resonant inductive link," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 2, pp. 303-311, June 2017.

[64] W. Zhang, S.-C. Wong, C. K. Tse, and Q. Chen, "Analysis and comparison of secondary series- and parallel-compensated inductive power transfer systems operating for optimal efficiency and load-independent voltage-transfer ratio," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2979–2990, Jun. 2014.

[65] J. Kim, D. Kim, and Y. Park, "Analysis of capacitive impedance matching network for simultaneous wireless power transfer to multiple devices," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2807–2813, May 2015.

[66] D. J. Thrimawithana and U. K. Madawala, "A generalized steady-state model for bidirectional IPT systems," *IEEE Trans. Power Electron.*, vol. 28, no. 20, pp. 4681-4689, Oct. 2013.

[67] U. K. Madawala, M. Neath, and D. J. Thrimawithana, "A power–frequency controller for bidirectional inductive power transfer systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 310-317, Jan. 2013.

[68] F. Lu, H. Zhang, H. Hofmann, and C. C. Mi, "An inductive and capacitive combined wireless power transfer system with LC-compensated topology," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8471-8482, Dec. 2016.

[69] U. K. Madawala and D. J. Thrimawithana, "A bidirectional inductive power interface for electric vehicles in V2G systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4789-4796, Oct. 2011.

[70] W. Li, H. Zhao, S. Li, J. Deng, and T. Kan, "Integrated LCC compensation topology for wireless charger in electric and plug-in electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4215-4225, July 2015.

[71] S. Li, W. Li, J. Deng, T. D. Nguyen, and C. Mi, "A double-sided LCC compensation network and its tuning method for wireless power transfer," *IEEE Trans. Veh. Technol.*, vol. 64, no. 6, pp. 2261–2273, June 2015.

[72] S. Samanta, A. K. Rathore, and D. J. Thrimawithana, "Bidirectional current-fed half-bridge (C) (LC)–(LC) configuration for inductive wireless power transfer system," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 4053-4062, July-Aug. 2017.

[73] S. Samanta and A. K. Rathore, "A new current-fed CLC transmitter and LC receiver topology for inductive wireless power transfer application: Analysis, design, and experimental results," *IEEE Trans. Transport. Electrific.*, vol. 1, no. 4, pp. 357-368, Dec. 2015.

[74] H. Feng, T. Cai, S. Duan, J. Zhao, X. Zhang, and C. Chen, "An LCC-compensated resonant converter optimized for robust reaction to large coupling variation in dynamic wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6591-6601, Oct. 2016.

[75] Q. Zhu, L. Wang, Y. Guo, C. Liao, and F. Li, "Applying LCC compensation network to dynamic wireless EV charging system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6557-6567, Oct. 2016.

[76] A. A. S. Mohamed, A. Berzoy, F. G. N. d. Almeida, and O. Mohammed, "Modeling and assessment analysis of various compensation topologies in bidirectional IWPT system for EVapplications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4973-4984, Sept.-Oct. 2017.

[77] Y. Song, U. K. Madawala, D. J. Thrimawithana, and M. Vilathgamuwa, "Three-phase bi-directional wireless EV charging system with high tolerance to pad misalignment," *IET Power Electron.*, vol. 12, no. 10, pp. 2697-2705, 2019.

[78] G. R. Kalra, D. J. Thrimawithana, B. S. Riar, C. Huang, and M. Neuburger, "A novel boost active bridge-based inductive power transfer system," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1103-1112, Feb. 2020.

[79] N. A. Keeling, G. A. Covic, and J. T. Boys, "A unity-power-factor IPT pickup for high-power applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 744-751, Feb. 2010.

[80] W. Zhang and C. C. Mi, "Compensation topologies of high-power wireless power transfer systems," *IEEE Trans. Veh. Technol.*, vol. 65, no. 6, pp. 4768-4778, June 2016.

[81] J. M. Miller, O. C. Onar, and M. Chinthavali, "Primary-side power flow control of wireless power transfer for electric vehicle charging," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 147-162, Mar. 2015.

[82] D. Vincent, P. S. Huynh, N. A. Azeez, L. Patnaik, and S. S. Williamson, "Evolution of hybrid inductive and capacitive AC links for wireless EV charging - A comparative overview," *IEEE Trans. Transport. Electrific.* , vol. 5, no. 4, pp. 1060-1077, 2019.

[83] M. Budhia, G. A. Covic, and J. T. Boys, "Design and optimization of circular magnetic structures for lumped inductive power transfer systems," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 1115-1123, Nov. 2011.

[84] M. Budhia, J. T. Boys, G. A. Covic, and C.-Y. Huang, "Development of a single-sided flux magnetic coupler for electric vehicle IPT charging systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 318–328, Jan. 2013.

[85] D. Vincent, S. Chakraborty, P. S. Huynh, and S. S. Williamson, "Efficiency analysis of a 7.7 kW inductive wireless power transfer system with parallel displacement," presented at the 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Hamilton, 2018.

[86] W. Chen, C. Liu, C. Lee, and Z. Shan, "Cost-effectiveness comparison of coupler designs of wireless power transfer for electric vehicle dynamic charging," *Energies*, vol. 9, no. 11, p. 906, 2016.

[87] A. Zaheer, H. Hao, G. A. Covic, and D. Kacprzak, "Investigation of multiple decoupled coil primary pad topologies in lumped IPT systems for interoperable

electric vehicle charging," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1937–1955, 2015.

[88] J. Everts, F. Krismer, J. V. d. Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954-3970, Aug. 2014.

[89] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm3 On-Board Power Electronics for 50 kW/85 kHz Automotive IPT System," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419-431, Mar. 2017.

[90] R. B. a. J. W. Kolar, "Multi-objective optimization of 50 kW/85 kHz IPT system for public transport," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1370-1382, Dec. 2016.

[91] B. Koushki, P. Jain, and A. Bakhshai, "A bi-directional AC-DC converter for electric vehicle with no electrolytic capacitor," in *Proc. IEEE 7th Int. Symp. Power Electron. Distributed Generation Syst. (PEDG)*, Vancouver, BC, 2016, pp. 1-8.

[92] D. S. B. Weerasinghe, U. K. Madawala, D. J. Thrimawithana, and D. M. Vilathgamuwa, "A three-phase to single-phase matrix converter based bi-directional IPT system for charging electric vehicles," in *Proc. IEEE ECCE Asia Downunder*, VIC, 2013, pp. 1240-1245.

[93] M. Moghaddami, A. Anzalchi, and A. I. Sarwat, "Single-stage three-phase AC–AC matrix converter for inductive power transfer systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6613-6622, Oct. 2016.

[94] N. X. Bac, D. M. Vilathgamuwa, and U. K. Madawala, "A SiC-based matrix converter topology for inductive power transfer system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4029-4038, Aug. 2014.

[95] A. Ecklebe, A. Lindemann, and S. Schulz, "Bidirectional switch commutation for a matrix converter supplying a series resonant load," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1173-1181, May 2009.

[96] S. Weerasinghe, U. K. Madawala, and D. J. Thrimawithana, "A matrix converter-based bidirectional contactless grid interface," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1755-1766, Mar. 2017.

[97] B. Koushki, A. Safaee, P. Jain, and A. Bakhshai, "A bi-directional single-stage isolated AC-DC converter for EV charging and V2G," in *Proc. IEEE Elect. Power Energy Conf. (EPEC)*, London, ON, 2015, pp. 36-44.

[98] H. L. Li, A. P. Hu, and G. A. Covic, "A direct AC–AC converter for inductive power-transfer systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 661-668, Feb. 2012.

[99] W. Sulistyono and P. Enjeti, "A series resonant AC-to-DC rectifier with high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 784-790, Nov. 1995.

[100] S. Samanta and A. K. Rathore, "A new inductive power transfer topology using direct ac–ac converter with active source current waveshaping," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5565-5577, July 2018.

[101] J. Shin and J. Y. Lee, "An electrolytic capacitor-less bi-directional EV onboard charger using harmonic modulation technique," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5195–5203, Oct. 2014.

[102] J. Liu, K. W. Chan, C. Y. Chung, N. H. L. Chan, M. Liu, and W. Xu, "Single-stage wireless-power-transfer resonant converter with boost bridgeless power-factor-correction rectifier," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2145-2155, March 2018.

[103] M. Kwon and S. Choi, "An electrolytic capacitorless bidirectional EV charger for V2G and V2H applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6792-6799, Sept. 2017.

[104] M. Rosekeit, C. Broeck, and R. W. D. Doncker, "Dynamic control of a dual active bridge for bidirectional ac charging," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2015, pp. 2085–2091.

[105] R. Prasad, C. Namuduri, and P. Kollmeyer, "Onboard unidirectional automotive G2V battery charger using sine charging and its effect on Li-ion batteries," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 6299–6305.

[106] H. Z. Beh, G. A. Covic, and J. T. Boys, "Effects of pulse and DC charging on lithium iron phosphate (LiFePO4) batteries," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 315–320.

[107] S. Bala, T. Tengner, P. Rosenfeld, and F. Delince, "The effect of low frequency current ripple on the performance of a Lithium Iron Phosphate (LFP) battery energy storage system," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 3485–3492.

[108] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.

[109] L. Chen, S. Wu, D. Shieh, and T. Chen, "Sinusoidal-ripple-current charging strategy and optimal charging frequency study for Li-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 88-97, Jan. 2013.

[110] S. Jeong, Y. Jeong, J. Kwon, and B. Kwon, "A soft-switching single-stage converter with high efficiency for a 3.3-kW on-board charger," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6959-6967, Sept. 2019.

[111] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962-981, Oct. 2003.

[112] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641-660, June 2004.

[113] A. Kamineni, M. J. Neath, G. A. Covic, and J. T. Boys, "A mistuning-tolerant and controllable power supply for roadway wireless power systems," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6689-6699, Sept. 2017.

[114] P. Si, A. P. Hu, S. Malpas, and D. Budgett, "A frequency control method for regulating wireless power to implantable devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 1, pp. 22-29, Mar. 2008.

[115] A. W. Green and J. T. Boys, "10 kHz inductively coupled power transfer-concept and control," in *Proc. IET 5th Int. Conf. Power Electron. Variable-Speed Drives*, London, 1994, pp. 694-699.

[116] J. Tian and A. P. Hu, "A DC-voltage-controlled variable capacitor for stabilizing the ZVS frequency of a resonant converter for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2312-2318, Mar. 2017.

[117] A. Kamineni, G. A. Covic, and J. T. Boys, "Self-tuning power supply for inductive charging," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3467-3479, May 2017.

[118] S. Samanta and A. K. Rathore, "Wireless power transfer technology using full-bridge current-fed topology for medium power applications," *IET Power Electron.*, vol. 9, no. 9, pp. 1903-1913, 2016.

[119] R. P. Twiname, D. J. Thrimawithana, U. K. Madawala, and C. A. Baguley, "A dual-active bridge topology with a tuned CLC network," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6543-6550, Dec. 2015.

[120] E. Asa, K. Colak, and D. Czarkowski, "Analysis of a CLL resonant converter with semi-bridgeless active rectifier and hybrid control," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6877-6886, Nov. 2015.

[121] K. Colak, E. Asa, M. Bojarski, D. Czarkowski, and O. C. Onar, "A novel phase-shift control of semibridgeless active rectifier for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6288-6297, Nov. 2015.

[122] I. I. Nam, R. A. Dougal, and E. Santi, "Novel unity-gain frequency tracking control of series–series resonant converter to improve efficiency and receiver positioning

flexibility in wireless charging of portable electronics," *IEEE Trans. Ind. Appl.,* vol. 51, no. 1, pp. 385-397, Jan.-Feb. 2015.

[123] G. Buja, M. Bertoluzzo, and K. N. Mude, "Design and experimentation of WPT charger for electric city car," *IEEE Trans. Ind. Electron.,* vol. 62, no. 12, pp. 7436-7447, Dec. 2015.

[124] D. Bavastro *et al.*, "Design of wireless power transmission for a charge while driving system," *IEEE Trans. Magn.,* vol. 50, no. 2, pp. 965-968, Feb. 2014.

[125] K. Aditya, S. S. Williamson, and V. K. Sood, "Impact of zero-voltage switching on efficiency and power transfer capability of a series-series compensated IPT system," in *Proc. IEEE Transport. Electrific. Conf. (ITEC-India),* Pune, 2017, pp. 1-7.

[126] K. Aditya and V. K. Sood, "Design of 3.3 kW wireless battery charger for electric vehicle application considering bifurcation," presented at the IEEE Elect. Power Energy Conf. (EPEC), Saskatoon, SK, 2017.

[127] Y. Jiang, L. Wang, Y. Wang, J. Liu, X. Li, and G. Ning, "Analysis, design, and implementation of accurate ZVS angle control for EV battery charging in wireless high-power transfer," *IEEE Trans. Ind. Electron.,* vol. 66, no. 5, pp. 4075-4085, May 2019.

[128] Y. Liu, U. K. Madawala, R. Mai, and Z. He, "Zero-phase-angle controlled bidirectional wireless EV charging systems for large coil misalignments," *IEEE Trans. Power Electron.,* vol. 35, no. 5, pp. 5343-5353, May 2020.

[129] H. Feng and S. M. Lukic, "Reduced-order modeling and design of single-stage LCL compensated IPT system for low voltage vehicle charging applications," *IEEE Trans. Veh. Technol.*, vol. 69, no. 4, pp. 3728-3739, Apr. 2020.

[130] K. Aditya and S. S. Williamson, "Design guidelines to avoid bifurcation in a series-series compensated inductive power transfer system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3973-3982, May 2019.

[131] Y. Yao, Y. Wang, X. Liu, F. Lin, and D. G. Xu, "A novel parameter tuning method for double-sided LCL compensated WPT system with better comprehensive performance," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8525-8536, 2018.

[132] G. R. Kalra, C. Y. Huang, D. J. Thirmawithana, U. K. Madawala, and M. Neuburger, "A comparative study on grid-integration techniques used in bi-directional IPT based V2G applications," in *IEEE 2nd Annu. Southern Power Electron. Conf. (SPEC)*, Auckland, 2016, pp. 1-6.

[133] J. T. Boys, C. Y. Huang, and G. A. Covic, "Single-phase unity power-factor inductive power transfer system," in *Proc. IEEE Power Electron. Specialists Conf.*, Rhodes, 2008, pp. 3701-3706.

[134] K. Colak, M. Bojarski, E. Asa, and D. Czarkowski, "A constant resistance analysis and control of cascaded buck and boost converter for wireless EV chargers," in *Proc. Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, Mar. 2015, pp. 3157-3161.

[135] K. Colak, E. Asa, M. Bojarski, and D. Czarkowski, "A novel common mode multi-phase half-wave semi-synchronous rectifier for inductive power transfer

applications," in *Proc. IEEE Transport. Electrific. Conf. Expo. (ITEC)*, Dearborn, MI, 2015, pp. 1-6.

[136] M. Fu, C. Ma, and X. Zhu, "A cascaded boost-buck converter for high-efficiency wireless power transfer systems," *IEEE Trans. Ind. Informat.,* vol. 10, no. 3, pp. 1972-1980, 2014.

[137] K. Aditya and S. S. Williamson, "Comparative study on primary side control strategies for series-series compensated inductive power transfer system," in *Proc. IEEE 25th Int. Symp. Ind. Electron. (ISIE)*, Santa Clara, CA, 2016, pp. 811-816.

[138] H. L. Li, "High frequency power converters based on energy injection control for IPT systems," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Auckland, Auckland, 2011.

[139] C. S. Wang, G. A. Covic, and O. H. Stielau, "Power transfer capability and bifurcation phenomena of loosely coupled inductive power transfer systems," *IEEE Trans. Ind. Electron.,* vol. 51, no. 1, pp. 148-157, Feb. 2004.

[140] S. Weearsinghe, D. J. Thrimawithana, and U. K. Madawala, "Modeling bidirectional contactless grid interfaces with a soft DC-link," *IEEE Trans. Power Electron.,* vol. 30, no. 7, pp. 3528-3541, July 2015.

[141] A. A. S. Mohamed, A. Berzoy, F. G. N. d. Almeida, and O. Mohammed, "Modeling and assessment analysis of various compensation topologies in bidirectional IWPT system for EV applications," *IEEE Trans. Ind. Appl.,* vol. 53, no. 5, pp. 4973-4984, Oct. 2017.

[142] Y. H. Sohn, B. H. Choi, E. S. Lee, G. C. Lim, G. H. Cho, and C. T. Rim, "General unified analyses of two-capacitor inductive power transfer systems: Equivalence of

current-source SS and SP compensations," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6030-6045, Nov. 2015.

[143] N. Liu and T. G. Habetler, "Design of a universal inductive charger for multiple electric vehicle models," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6378-6390, Nov. 2015.

[144] B. Esteban, M. Sid-Ahmed, and N. C. Kar, "A comparative study of power supply architectures in wireless EV charging systems," *IEEE Trans. Power Electron.*, vol. 11, no. 30, pp. 6408–6422, Nov. 2015.

[145] P. S. Huynh and S. S. Williamson, "Analysis and design of soft-switching active clamping half-bridge boost inverter for inductive wireless charging applications," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 1027-1039, Dec. 2019.

[146] Y. Zhang, T. Kan, Z. Yan, and C. C. Mi, "Frequency and voltage tuning of series–series compensated wireless power transfer system to sustain rated power under various conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1311-1317, June 2019.

[147] S. M. Cuk, "Modelling, analysis, and design of switching converters," Ph.D. dissertation, California Institute of Technology, Nov. 1976.

[148] E. X. Yang, F. C. Lee, and M. M. Jovanovic, "Small-signal modeling of power electronic circuits by extended describing function concept," in *Proc. Virginia Power Electron. Center Seminar*, 1991, pp. 167–178.

[149] Z. U. Z. e. al., "Modeling and control of series–series compensated inductive power transfer system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 11, pp. 111-123, March 2015.

[150] K. Aditya, V. K. Sood, and S. S. Williamson, "Magnetic characterization of unsymmetrical coil pairs using archimedean spirals for wider misalignment tolerance in IPT systems," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 2, pp. 454-463, June 2017.

[151] Y. Jiang, L. Wang, Y. Wang, J. Liu, M. Wu, and G. Ning, "Analysis, design, and implementation of WPT system for EV's battery charging based on optimal operation frequency range," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6890-6905, July 2019.

[152] A. Ramezani, S. Farhangi, H. Iman-Eini, B. Farhangi, R. Rahimi, and G. R. Moradi, "Optimized LCC-series compensated resonant network for stationary wireless EV chargers," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2756-2765, Apr. 2019.

[153] L. Patnaik, A. V. J. S. Praneeth, and S. S. Williamson, "A Closed-loop constant-temperature constant-voltage charging technique to reduce Charge time of Lithium-Ion batteries," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1059-1067, Feb. 2019.

[154] T. Ikeya, N. Sawada, S. Takagi, J. Murakami, and K. Kobayashi, "Multi-step constant-current charging method for electric vehicle, valve-regulated, lead/acid batteries during night time for load-leveling," *J. Power Sources*, vol. 75, no. 1, pp. 101–107, Sep. 1998.

[155] T. Ikeya, N. Sawada, J. Murakami, and K. Kobayashi, "Multi-step constant-current charging method for an electric vehicle nickel/metal hydride battery with high-energy efficiency and long cycle life," *J. Power Sources*, vol. 105, no. 1, pp. 6–12, Mar. 2002.

[156] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. Seattle, WA, USA: Morgan & Claypool, 2015.

[157] S. Samanta, A. K. Rathore, and D. J. Thrimawithana, "Analysis and design of current-fed half-bridge (C)(LC)–(LC) resonant topology for inductive wireless power transfer application," *IEEE Trans. Ind. Appl.,* vol. 53, no. 4, pp. 3917-3926, 2017.

[158] S. Samanta and A. K. Rathore, "Small signal modeling and closed-loop control of parallel-series/series resonant converter for wireless inductive power transfer," *IEEE Trans. Ind. Electron.*, pp. 1-1, 2018.

[159] T. Mishima and E. Morita, "High-frequency bridgeless rectifier based ZVS multiresonant converter for inductive power transfer featuring high-voltage GaN-HFET," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 9155-9164, Nov. 2017.

[160] F. Liu, K. Chen, Z. Zhao, K. Li, and L. Yuan, "Transmitter-side control of both the CC and CV modes for the wireless EV charging system with the weak communication," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 6, no. 2, pp. 955-965, June 2018.

[161] Y. Zhang, K. Chen, F. He, Z. Zhao, T. Lu, and L. Yuan, "Closed-form oriented modeling and analysis of wireless power transfer system with constant-voltage source and load,," *IEEE Trans. Power Electron.,* vol. 31, no. 5, pp. 3472-3481, May 2016.

[162] P. Mattavelli, G. Spiazzi, and P. Tenti, "Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers," *IEEE Trans. Power Electron.,* vol. 20, no. 1, pp. 140-147, Jan. 2005.

[163] W. Zhang, Y. Liu, and B. Wu, "A new duty cycle control strategy for power factor correction and FPGA implementation," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1745-1753, Nov. 2006.

[164] W. Zhang, G. Feng, Y. F. Liu, and B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1474-1485, Nov. 2004.

[165] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 411-419, Jan. 2003.

[166] (2018). Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤ 16 A per phase) [Online]. Available: https://webstore.ansi.org/Standards/IEC/IEC61000Ed2018-1673232

[167] F. Lacressonni, B. Cassoret, and J. F. Brudny, "Influence of a charging current with a sinusoidal perturbation on the performance of a lead–acid battery," in *Proc. Inst. Elect. Eng. Power Appl.*, Sep. 2005, vol. 152, pp. 1365–1370.

[168] K. Tae-Hoon *et al.*, "Analytical study on low-frequency ripple effect of battery charging," in *Proc. Veh. Power Propulsion Conf.*, Oct. 2012, pp. 809–811.

[169] S. Bala, T. Tengner, and P. Rosenfeld, "The effect of low frequency current ripple on the performance of a lithium iron phosphate (LFP) battery energy storage system," in *Proc. IEEE Energy Convers. Congr. Expo (ECCE)*, Sep. 2012, pp. 3485–3492.

[170] B. Koushki, P. Jain, and A. Bakhshai, "A single-stage bi-directional AC-DC converter with no electrolytic capacitor for EV," in *Proc. Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, 2018, pp. 1447-1454.

[171] W. L. Malan, D. M. Vilthgamuwa, G. R. Walker, M. A. H. Broadmeadow, D. Thrimawithana, and U. Madawala, "A single phase AC-DC bidirectional converter with integrated ripple steering," in *Proc. IEEE 8th Int. Power Electron. and Motion Control Conf. (IPEMC-ECCE Asia)*, Hefei, 2016, pp. 2270-2275.

[172] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 1, pp. 15-25, Mar. 2016.