Design and Development of a Traction Motor Emulator using a Three-Phase Bidirectional Buck-Boost AC-DC Converter

by

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

Abstract

An industrial drive testing, with a 'real-machine' can pave way, for some serious issues to test-bench, motor, and the operator. A slight disturbance in control logic amid testing, can damage the physical machine or drive. Such dangerous testing conditions can be avoided by supplanting real motor with a power electronic converter based 'Motor Emulator' (ME) test-bench system. The conventional ME comprises of two-stage three-phase AC-DC-AC conversion with first-stage AC-DC as emulator and second-stage DC-AC as regenerating unit. This two-stage power conversion, require independent control algorithm, burdening control complexity as well as the number of power electronic switches are quite significant.

Therefore, to economize and downsize conventional multistage ME system, this research work experimentally validates a common-DC-bus-configured ME system with only the AC-DC regenerative emulator stage. A bidirectional three-phase AC-DC converter is proposed as the regenerative emulator converter in a common-DC-Bus-configured ME system. The Proposed converter's operating principle along with mathematical design and control strategy are also presented. To validate the operation of the proposed converter as a common DC-bus-configured emulator, two permanent magnet synchronous motors (PMSM) of $7.5\ kW$ and $2.0\ kW$ are emulated and their simulation and experimental results are presented here.

The proposed bi-directional converter inspired from classical buck-boost operation, requires just ten unidirectional IGBT switches preventing any circulating current in the system. The proposed converter also eliminates the regenerative converter stage in classical ME system. Also, the proposed common-DC-bus-configured ME system requires a single stage control unlike independent control in existing ME system. The proposed converter provides four-quadrant operation and emulation of motor under study. The dynamic model of PMSM motor is simulated on the MATLAB simulation platform and the Simulation results are compared with experimental results. From the simulation and experimental results, it is concluded that, with the presented control scheme, the proposed ME converter can be made to draw the same current as a real machine would have drawn, had it been driven by the same DUT. Since, the output current of proposed converter is fed back to DC bus, the input power source requirement is reduced, making the overall ME system more energy efficient.

Keywords: AC-DC, bi-directional power converter, buck-boost, DC-AC, PMSM, synchronous power converter, traction motor emulator, virtual isolation

Author's Declaration

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Statement of Contributions

Part of the work described in Chapter – 2 has been published as:

[1] **A. H. Kadam**, R. Menon, and S. S. Williamson, "A four-quadrant three-phase AC-DC converter for virtual electric traction machine," *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, TN, India, 2018, pp. 1–6. **DOI: 10.1109/PEDES.2018.8707625**.

Part of the work described in Chapter – 3 has been published as:

[1] **A. H. Kadam**, and S. S. Williamson, "A common DC-bus-configured traction motor emulator using a virtually isolated three-phase AC-DC bidirectional converter," *in IEEE Access*, vol. 9, pp. 80621-80631, 2021. **DOI: 10.1109/ACCESS.2021.3085029**.

[2] **A. H. Kadam**, R. Menon, and S. S. Williamson, "A novel three-phase bi-directional buck-boost AC-DC converter for PMSM virtual machine system with common DC bus," *IEEE Applied Power Electronics Conference and Exposition-2018 (APEC–2018)*, San Antonio, TX, USA, 2018, pp. 1944–1951. **DOI: 10.1109/APEC.2018.8341284**.

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[2] **A. H. Kadam**, and S. S. Williamson, "A common DC-bus-configured traction motor emulator using a virtually isolated three-phase AC-DC bidirectional converter," *in IEEE Access*, vol. 9, pp. 80621-80631, 2021.

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[3] **A. H. Kadam**, and S. S. Williamson, "An electric traction system emulator using state feedback linearization single-loop control method," *in Journal of Emerging and Selected Topics in Industrial Electronics*. **(Under Review)**

[4] **A. H. Kadam**, R. Menon, and S. S. Williamson, "Traction inverter performance testing using mathematical and real-time controller-in-the-loop permanent magnet synchronous motor emulator," *IECON 2016 – 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, 2016, pp. 6651–6656.

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Dedicated to my ***Family...***

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APPENDIX – B

List of Abbreviations

AC	Alternating Current
C-BBC	Current DC-Link Back to Back Converter
CSI	Current Source Inverter
DC	Direct Current
DMC	Direct Matrix Converter
DSP	Digital Signal Processor
DTB	Dyno Test Bed
DUT	Device Under Test
EV	Electric Vehicle
HEV	Hardware-in-the-Loop
HTB	Hardware Test Bed
IEEE	Institute of Electrical and Electrical Engineers
IGBT	Insulated Gate Bipolar Transistor
IM	Induction Motor
IMC	Indirect Matrix Converter
MC	Matrix Converter
ME	Motor Emulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

PE	Power Electronics
PEC	Power Electronic Converter
PHIL	Power-Hardware-in-the-Loop
PLL	Phase Locked Loop
PM	Permanent Magnet
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
RMS	Root Mean Square
TME	Traction Motor Emulator
V-BBC	Voltage DC-link Back to Back Converter
VSI	Voltage Source Inverter

List of Symbols

i_{ds}^{s}	–	*d-axis Current in Stationary Reference Frame*
i_{qs}^{s}	–	*q-axis Current in Stationary Reference Frame*
i_{ds}^{r}	–	*d-axis Current in Synchronously Rotating Reference Frame*
i_{qs}^{r}	–	*q-axis Current in Synchronously Rotating Reference Frame*
λ_{ds}	–	*d-axis Winding Flux*
λ_{qs}	–	*Flux Linkages*
L_d	–	*d-axis Winding Inductance*
L_q	–	*q-axis Winding Inductance*
L_{dd}	–	*Self-Inductance of q-axis Winding*
L_{dq}	–	*Mutual Inductance Between d-axis and q-axis Winding*
L_{qd}	–	*Mutual Inductance Between q-axis and d-axis Winding*
ω_r	–	*Rotor Reference Speed*
ω_m	–	*Rotor Mechanical Speed*
p	–	*Differentiator Operator*
P	–	*Number of Poles*
P_i	–	*Instantaneous Power*
R_d	–	*d-axis Resistance*
R_q	–	*q-axis Resistance*

σ_d^{err}	–	*Integration of d-axis Current Error*
σ_q^{err}	–	*Integration of q-axis Current Error*
θ_r	–	*Instantaneous Rotor Position with respect to Stator d-axis*
θ	–	*Phase Angle*
T_e	–	*Electromagnetic Torque*
v_{ds}^s	–	*d-axis Voltage in Stationary Reference Frame*
v_{qs}^s	–	*q-axis Voltage in Stationary Reference Frame*
v_{ds}^r	–	*d-axis Voltage in Synchronously Rotating Reference Frame*
v_{qs}^r	–	*q-axis Voltage in Synchronously Rotating Reference Frame*

Chapter 1

Introduction

CONVENTIONALLY , in the development stage the drive is tested with a physical rotating electric machine. This traditional method has certain drawbacks like, large space requirement, large test time requirement, heavy and large equipment complexity, high operating cost, difficulty in testing for different load configuration as real motor need to be replaced for different configuration [1] etc. To overcome these issues “Motor Emulator” is the suitable option.

Motor emulator is a power electronic converter based controlled load, which resembles the characteristics of an electrical machine either PMSM or IM [2]. It matches the magnitude and wave-shape of the current which would be drawn from the source by a physical rotating electric machine, had the same source been applied to both. In a hardware test bed (HTB), it is possible to replace the real motor with a power electronic motor emulator which emulates the behavior of a PMSM. The machine parameter can easily be modified in the processor to make the emulator behave as a complete different motor[1]–[3].

According to [4], electric vehicle drives are tested with two standard test bench configurations –

- Dyno test bed (DTB) with physical rotating electric machine,
- Hardware-in-Loop (HIL) system with motor emulator.

The conventional method of EV drive testing is dyno test bed. The DTB comprises of real electric motor which is driven by the DUT. The DUT is tested by running the physical electric motor under desired torque and speed references. Since the real electric motor is used in DTB, in order to test the DUT, the motor needs to be replaced by another motor with desired rating. This is the major drawback of the DTB as this process increases the operating cost, test time and complexity.

HIL is a technique that is used in the development of complex real-time systems. In a control system, HIL simulation makes use of power electronic hardware instead of their simulation model and other part of the control loop are simulated in a high speed digital signal processor [5]. This provides the flexibility of interfacing of real quantities like voltages and current with the mathematical model of system through digital signal processor. The HIL reduces development time as well as allows comprehensive testing of control system to prevent expensive and hazardous failures [6]. HIL simulation is also used in Power propulsion systems for EV and HEV [7]–[11].

Bouscayrol, A. [6] has discussed in detail, the various concepts of HIL for electric drives viz. signal level, power level and mechanical level HIL simulation. According to [6], in signal level HIL simulation, the power electronics, machine and mechanical load are simulated in real-time. The DSPs and microcontrollers are widely used in real-time simulation of motor models [12], [13]. A real-time FPGA based HIL simulation have been reported in [2], [14]–[17]. But, as FPGAs not arithmetic processors, unlike DSPs, they require additional resources for complex mathematical tasks [18].

1.1 Dyno Test Bed v/s Motor Emulator

The comparison between traditional Dyno Test Bed and Motor Emulator is presented in TABLE – 1.1.

TABLE – 1.1
DYNO TEST BED V/S HARDWARE-IN-LOOP

Dyno Test Bed (DTB)	Hardware-in-Loop (HIL)
Extensive mechanical setup and handling with different electric motor types	Reduced handling effort with a virtual electric motor
Rotating parts (safety issue), hazardous environment	Low hazard potential, simplified automation/safety system
Operating, maintenance & lifetime costs	Lower operating costs
Electric motor availability limitation for different motor types	Switch between different model types by Software
Emission of acoustic noise	Placement in a development lab is possible
Inertia and dynamic of test rig drivetrain might be different from real vehicle drivetrain depending on dynamometer control dynamics and drivetrain simulation	All load conditions of the emulated electric motor can be simulated as they occur in the vehicle during real-life driving situation. No mechanical setup limiting the drivetrain dynamics

1.2 Motor Emulator

In the development of new motor drive application, modeling, simulation and control design are important steps and their interdependencies, together with implementation in hardware and tests on a test bench [3]. Software simulation platforms do not require power electronics or machines at all and are independent of physical world. Since many years, analog models and hardware-in-the-loop [19]–[21] have been employed to close the gap between simulation model and physical world. The next step on the way closer to reality

is to replace the machine itself by power electronics – the application to be tested (DUT) remains unchanged. The parameters of the motor to be emulated can such be selected by suitable models and their parameters. Motor emulator eliminates the need for restructuring HTB or replacing the physical rotating machine for testing a drive at different rating of the machine.

1.2.1 Concept of Motor Emulator

According to [2], the primary objective of motor emulation is to design the power electronic load interface for the actual motor load. Therefore, the behavior of the motor emulator must be close to the actual motor load when connected to a DUT. The motor emulator configuration is shown in Figure 1.1, where the power supply is from a three-phase DUT. Therefore, accurate information of the phase angle of the power supply voltages is essential. The phase angle of a three-phase voltage is obtained through the popular method called phase-locked loop (PLL). This takes as its input, the three-phase voltages of the DUT and produces a sinusoidal signal of the same frequency as the frequency of the three phase DUT voltages. The topic of PLL has been extensively reported in literature [22]–[24].

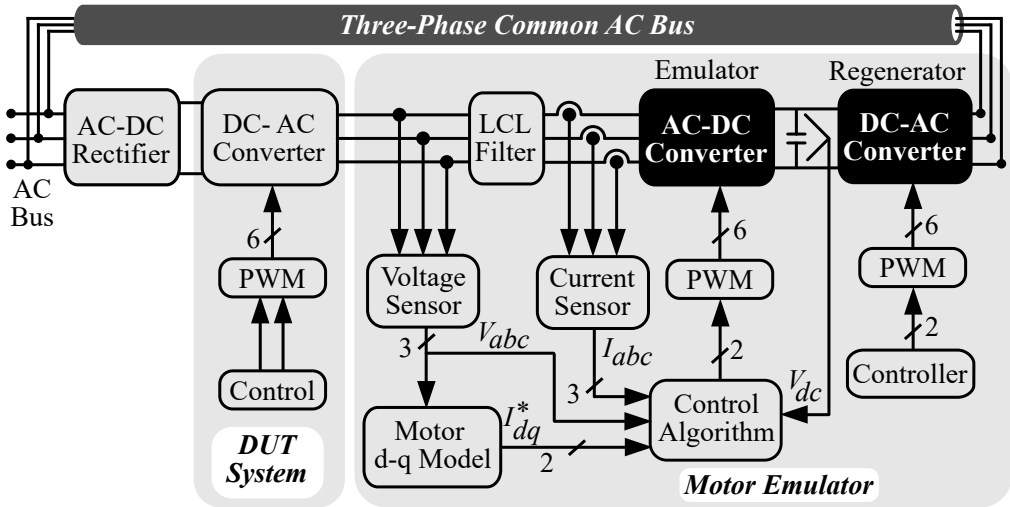

Figure 1.1: Block diagram of classical motor emulator.

The core element of motor emulation is the algorithm that produces the desired currents to be drawn so as to mimic the actual motor. Thereafter, the control system ensures that the ME draws or supplies currents that are as close as possible to the desired current references. The ME is connected to the DUT through an interface impedance known as the filter. Since the ME mimics the behavior of an electrical motor, it would have to draw or source power as per motor characteristics. In order to enable the ME to be a sink or source of active power, a back-to-back VSI forming a two level AC-AC cyclo-converter is used. The dc link of the ME VSI is common to another VSI known as the reverse power flow converter. This reverse power flow converter is a three-phase VSI whose AC output is interfaced to the three-phase AC grid. This converter draws or supplies active power from the three-phase AC grid to the emulator VSI.

1.2.2 Structure of Motor Emulator

A ME system comprises of two back-to-back AC-DC and DC-AC power converters as shown in Figure 1.1. Where former, operates as an *emulator* and latter as a *regenerating unit* [2], [3], [25]–[28]. The output of regeneration unit is interfaced with utility grid, to act as 'sink' or 'source' in case of motoring or regenerative braking operation respectively. This two-stage arrangement forming AC-AC PWM cyclo-converter with common DC link capacitor, requires independent control and increases controller complexity [2]. The dc-link element ensures the decoupling between two converter stages [29]. This entrench that, a constant source is available at the input of DC-AC inverter stage, which increases the converter's power capability. However, the dc-link element can have a relatively large size compared with the total converter size [29].

1.3 Issues with Existing Motor Emulator Systems

H. J. Slater [1], in 1996 proposed the concept of "virtual machine" or ME. Since then many researchers [2]–[4], [27], [30], [31] have worked in the field of ME. Although, ME are existing for almost two decades, there are few issues associated with the existing structure of ME as listed below –

- The existing ME system comprises of AC-DC and DC-AC converter with former operating as ME and later as regenerating unit. This increases the number of power electronic stages in the system as well as both these converters require independent control which increases the control complexity.

- The DUT has its own control algorithm independent from the ME control. If the DUT makes use of variable frequency drive (VFD), the ME converter and its control should adopt to the frequency change instantly and produce the variable frequency output.

1.4 Research Objectives

Considering the issues with existing ME system, the primary objectives of this research work are to –

- **Propose a simplified ME system architecture.**

- **Proposed an improved power converter topology for ME system.**

- **Propose a simplified control strategy for the proposed ME system**

The above objectives are further elaborated in Chapter – 2, section 2.4 with specific research contributions to this research work.

1.5 Thesis Outline

The organization of this thesis is as follows.

- **Chapter – 1:**

  The conceptual background introduction to existing ME system and a brief description of issues with existing ME system architecture along with the primary objectives are presented in Chapter – 1.

- **Chapter – 2:**

  Chapter – 2 provides a thorough background of the state-of-the-art of the motor emulator (ME) systems. The motivation, and problem definition along with the proposed research contributions to overcome and simplify the issues associated with ME system are presented in Chapter – 2.

- **Chapter – 3:**

  The proposed single-stage, bidirectional, buck-boost three-phase AC-DC power converter topology is presented in Chapter – 3. The operation of proposed bidirectional AC-DC converter along with voltage gain derivation in each quadrant is presented in Chapter – 3. Design of proposed converter and open loop simulation results of are also presented here.

- **Chapter – 4:**

  Chapter – 4 consists of design and development of the proposed common DC-bus-Configured ME system. A design methodology for each physical component of the proposed system is documented in Chapter – 4. Converter power loss and efficiency analysis is also presented.

- **Chapter – 5:**

  The control scheme for emulating a PMSM motor is discussed in Chapter – 5. Detailed experimental and simulation test results are presented for PMSM motors under study.

- **Chapter – 6:**

  Chapter – 6 summarizes the various findings of proposed research work. It also provides a brief overview of future scope of the work presented in this research work.

1.6 Summary

This chapter provides a brief overview of the existing ME systes, issues with existing ME systems as well as need of proposed common DC-bus-configured ME architecture. A brief description of the proposed research contributions of this research work has also been presented.

Chapter 2

Traction Motor Emulator – A Research Scope

MOTOR emulator are existing in literature for over two decades. The earliest available research article (*according to IEEE database*) related to electrical motor emulator is by Ben Saoud [32], from 1996. Although, this research work discuss emulation of DC machine, it laid the foundation and opened the doors for power electronics researchers to explore the possible research scope in this field. Since then, many researchers have worked on developing the AC as well as DC motor emulators. H. J. Slater [1], presented his PhD Dissertation in 1996 on the topic of "Virtual Machine" (VM). The research in the field of electrical motor emulation is also available in the literature by various names as "Electrical Load Emulator" [2], "Machine Emulator" [3], "e-Machine Emulator" [4], "Hardware-in-the-Loop" [6], [8]–[10], [25], [26], [33]–[35], "Virtual Electric Traction Machine" [36] etc.

This chapter presents a brief review of AC-AC converters used in ME applications, followed by the motivation and the problem definition to carry out this research work. The

specific research contributions to the field are listed in the following section which is then followed by the literature review of the state-of-the-art of the ME system.

2.1 AC-AC Converter - A Brief Review

AC-AC or AC-DC-AC converter is the essential part of the ME system. As discussed in the previous section, the existing ME systems consist of AC-DC-AC, two stage converters. This two stage conversion needs independent control as well as increases the controller complexity [2]. In addition, since the DUT has its own control drive which is independent of ME control, there is possibility of the DUT using variable frequency drive (VFD). Hence motor emulator AC-AC converter needs to provide variable voltage with variable frequency operation.

Three phase AC-AC converters with current or voltage dc-link are primarily used in PE applications. The advantage of the dc-link energy storage element is that, both the converter stages are to a large extent, decoupled regarding their control [29], [37]. Further, a constant source-independent quantity is available at the input of the second stage i.e. DC-AC inverter stage, which increases the converter's power capability. On the other hand, the dc-link energy storage element can have a relatively large physical volume compared with the total converter volume [29], [38].

There are three conventional AC-AC converter systems; direct AC-AC converters [39]–[41], indirect AC-DC-AC converters with dc-link [42]–[44], and matrix converters (MCs) [29], [45]–[50]. Although direct ac-ac converters provide single-stage conversion, has simple topology as well as simple control and smaller size [51]; can only provide voltage control operation. Indirect AC-DC-AC converters with dc-link element can provide both voltage control and frequency control. On the other hand, they need a huge dc-link capacitor and a bulky source filter inductor resulting in high cost, large size, high losses and

low reliability [29].

The MCs can also provide voltage and frequency control with directly connected input supply to load without dc-link element. Therefore, they are best substitute to conventional indirect AC-DC-AC converters with dc-link [49]. Due to huge demand in industrial applications, the MCs have successfully attracted PE researchers to carry out research on their topological development [52], [53], modeling and control [54]–[56], and applications [46], [57].

A brief comparison of the basic bidirectional AC-AC converter topologies, i.e., the V-BBC, C-BBC (indirect AC-AC converter), IMC, and DMC, is presented in [29] by Kolar et. al. as part of AC-AC converter review. The key properties of these topologies, such as the number of transistors and diodes, the number of isolated gate driver supplies, or the required PWM signals, etc., are listed in TABLE – 2.1.

TABLE – 2.1
KEY PROPERTIES OF THE BASIC AC-AC CONVERTER TOPOLOGIES [29]

Parameters	V-BBC	C-BBC	IMC	DMC
Number of Transistor	12	12	18	18
Number of Diode	12	12	18	18
Number of Isolated Gate Driver Supplies	8	8	9	9
Number of PWM Signals	12	12	12	18
Number of Devices in Current Path	4	8	6	4
Intermediate Storage Element	C	L	No	No
Maximum Output Voltage	$> V_{in}$	$> V_{in}$	$0.86V_{in}$	$0.86V_{in}$
Additional Protection	No	Yes	Yes	Yes

From the data tabulated in TABLE – 2.1, it is evident that, though MC needs more

number of switches and PWM signals compared to AC-AC converters with DC link element, they don't require additional protection circuitry. The MC has a limited output voltage range compared to V-BBC and C-BBC, which allows boost operation of the input stage [29].

2.2 Motivation

The issues discussed in above, motivated to carry out the further research in the field of ME. According to the literature review presented in previous section, there is scope for the improvement in the overall architecture of the ME system and the AC-AC converter topology with less no. of switches, diodes, isolated gate drivers as well as boost operation of input stage. In other words, there is need for the novel power converter topology with all the features of different types of AC-AC converters. The issues discussed before demands the –

- Development of a single-stage, bi-directional, buck-boost converter topology.

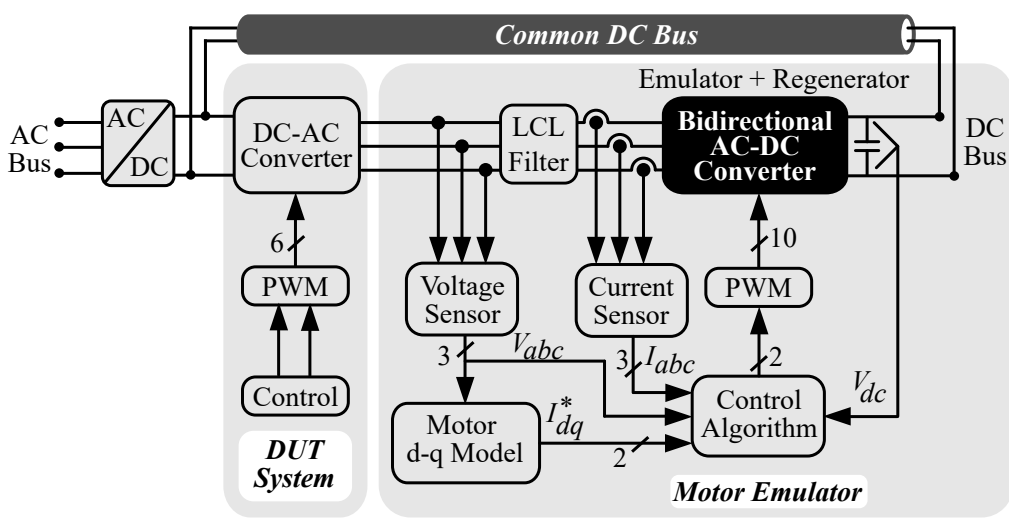

Figure 2.1: Block diagram of common DC-bus-configured motor emulator.

To simplify the control algorithm and to reduce the number of converter stages, a common DC-bus-configured ME system architecture is proposed in this research work and was presented in [58], [59], where output of the AC-DC converter stage is fed back to DC source of the DUT. The structure of ME with common DC bus is shown in Figure 2.1, where DUT input as well as DC side of the proposed converter are supplied with a common DC source. Unlike the system shown in Figure 1.1, where three-phase AC output of the regenerator converter is fed back to the utility, the output power of proposed converter is fed back to the common DC source.

2.3 Problem Definition

The first and foremost choice of AC-DC converter for ME system with the common DC bus architecture shown in Figure 2.1 is, conventional two-level, six-switch, three-phase, three-leg full bridge converter. This most popular and simplest topology however, pose some difficulties particularly in common DC bus ME architecture due to applied voltage potential on either side of converter. To briefly discuss issue associated with conventional three-phase AC-DC topology, an equivalent but reduced structure with only three-phase AC input from DUT and DC bus at the output representing *'Bidirectional AC-DC Converter'* block in **??**, is presented in Figure 2.2. Rest of the ME system shown in **??** is assumed to be as it is.

A standard two-level three-phase AC-DC converter with MOSFET switches as shown in Figure 2.2, is considered for the brief discussion of issues associated with its utilization in common DC bus ME architecture. It is assumed that –

- ME is operating in forward motoring mode with positive $phase - a$ and $-c$, and negative $phase - b$.

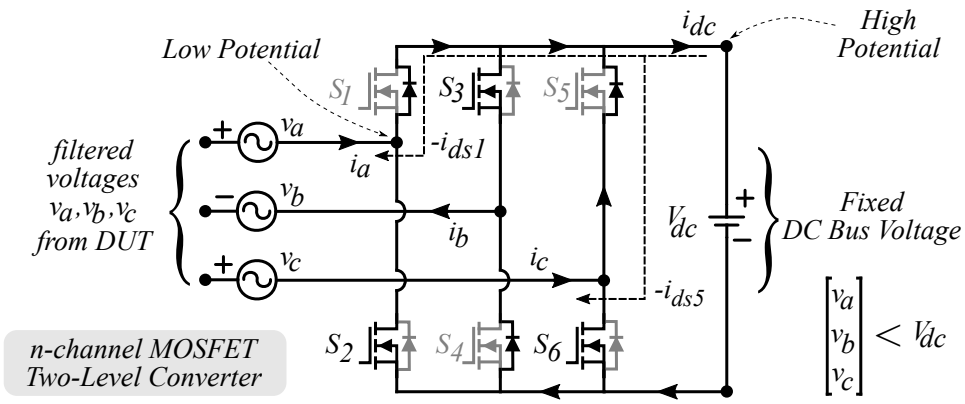

Figure 2.2: Forward current blocking with conventional AC-DC full-bridge converter.

- Currents i_a and i_c are expected to be flowing from DUT to DC bus.
- Current i_{dc} is returning through S_4 in the form of i_b.
- Switch S_2, S_3 and S_6 are ON while switch S_1, S_4 and S_5 are OFF.
- The filtered voltages v_a and v_c are time varying AC voltage with peak magnitude less than stiff DC bus voltage (V_{dc}), due to the filter attenuation as well as the emulated speed of the motor.

In $n - channel$ MOSFET, forward current flows through switch from, $drain$ terminal to $source$ terminal [60]. With the arrangement shown in Figure 2.2, following are the issues with conventional two-level converter with $n - channel$ MOSFET while used in common DC-Bus-configured ME.

- With the arrangement shown in Figure 2.2, desired current flow from $source$ to $drain$ terminal is not possible through body diode of MOSFET switches during forward motoring operation.

- The body diodes are always reversed biased due to high potential on $drain$ terminal of upper switches and low potential on $source$ terminal of lower switches.

- A 'high' switching pulse on any of the upper switch (*which is always a case*), will cause current to flow from 'high potential' $DC+$ terminal to 'low potential' $source$ terminal of switch, resulting in forward current blocking. The forward blocking current path are shown in Figure 2.2, as i_{ds1} and i_{ds5}.

- Reversing the direction of the MOSFET switches would reverse the direction of the anti-parallel diodes. This will result in short-circuit in each limb of the two-level converter, since diodes will be forward biased due to applied DC bus voltage.

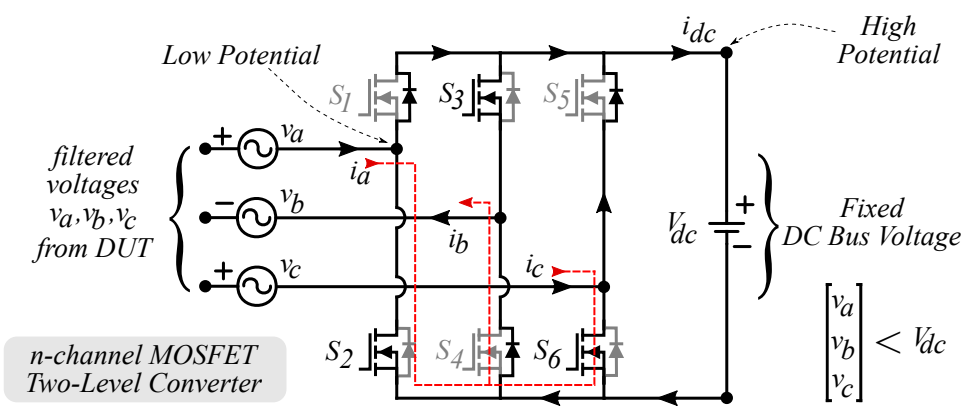

Figure 2.3: Circulating current in conventional AC-DC full-bridge converter.

An another issue associated with using conventional full-bridge AC-DC converter is, the circulating current.

- For the given assumption conditions, the *anode* terminal of S_4 body diode is at '*zero*' potential and *cathode* terminal is at *negative* potential, resulting the body diode to forward bias.

- This opens a shortest circulating current path for the forward current which could adversely affect the control algorithm and needs to be suppressed.

Although, MOSFET switches are shown in Figure 2.2 and 2.3 for discussion of issue, same issues are applicable for two-level IGBT converter with anti-parallel diode. Overall, given the situation, conventional three-phase AC-DC topology is not suitable for ME application especially with common DC bus architecture shown in Figure 2.1. However, in braking mode this arrangement would not cause any issue, as current is desired to flow from DC bus to DUT.

From Figure 2.2 and 2.3, it is inferred that, during forward motoring operation, a voltage higher than DC bus voltage is required to be maintained at the AC side of emulator converter for current flow from DUT to DC bus through ME converter. **For this purpose, a boost operation is desired.** Whereas, during forward braking operation, voltage lower than DC bus voltage is required to be maintained at the AC side of ME converter, **which can be achieved by buck operation.** Therefore, conventional AC-DC converter cannot be used in common DC bus ME system and needs to be replaced by a **bidirectional buck-boost AC-DC converter.**

Similarly, to eliminate the circulating current path, **unidirectional power semiconductor switches such as RB-IGBTs** can be used in the proposed converter. Also, to avoid forward current blocking, a **short-duration virtual isolation of DC bus** is desired.

2.4 Research Contribution

Although, motor emulator are existing for over two decades, there has been little to no research focus on simplifying the whole system by optimizing power converter topology used as an emulator. Therefore, as an attempt to simplify the whole ME architecture

including converter topology, this research proposes a virtually isolated bidirectional three-phase AC-DC converter based on synchronous buck-boost operation. The objectives and contributions of this research work are –

1. **Design and development of a virtually isolated, bi-directional buck-boost AC-DC power converter topology.**

   A virtually isolated bi-directional AC-DC power converter topology inspired from conventional buck-boost DC-DC converter and AC-DC converter is proposed here. A 10-kW prototype of the proposed bidirectional buck-boost AC-DC converter is designed for the experimental verification of the topology. and its application as a ME system. However, for experimental verification, an $7.5\ kW$ PMSM motor has been considered to compare the results with physical motor. The topology presented here makes use of ten reverse blocking power semiconductor switches. The reverse blocking IGBTs used in the proposed topology prevents any shoot-through effect in as well as avoids any circulating current from AC side to DC side and vice-versa.

2. **Development of a common DC-bus-configured ME system prototype.**

   A common DC-bus-configured ME system has been developed for experimental verification of the proposed system. The proposed system comprises of an off-the-shelf Semikron converter as DUT controlled with DTC. The control algorithm for DUT has been implemented on a digital signal processor (DSP) LaunchXL F28379D from Texas Instruments Inc. The prototype of proposed bi-directional converter, is interfaced with the DUT to develop a common DC-Bus-configured ME system. For experimental verification of the proposed system and converter topology, a PMSM motor of $7.\ 5kW$ is emulated. The experimental results obtained for $7.5\ kW$ PMSM motors are validated with a physical PMSM motor test results as well as simulation results.

3. **Implementation of a single loop control strategy for proposed ME System.**

   Normally, with LCL filter, the control system follows double closed loop with outer loop controlling DC voltage and inner loop controlling AC current. However, for some special applications like common DC-bus-configured motor emulator (ME) system, the DC bus voltage is not required to be controlled. In addition, the presence of LCL filter introduces cross coupling of flux and torque component in case of AC motor emulation. The double closed loop control is generally adopted to decouple torque and flux components, however the controller design is more complex process. Therefore, this research presents a single loop control of a common DC-bus-configured ME system with LCL filter based on state feedback linearization method. The decoupling equations in direct and quadrature axis are derived here.

2.5 Literature Review

Since beginning, there has been little to no change in the architecture of ME system. The generalized ME architecture comprises of an AC-DC-AC power electronic converter as emulator, and controller for implementing mathematical model of motor under study as well as for implementing close loop control of the system.

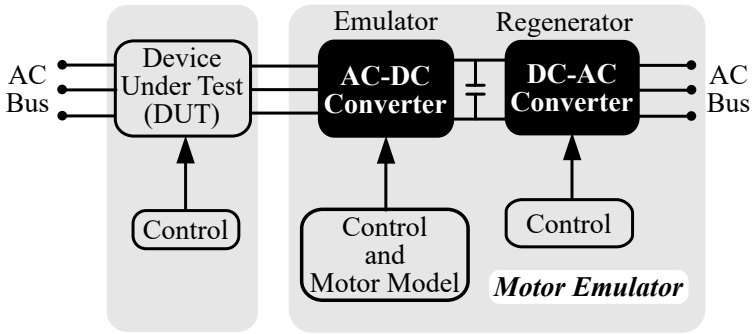

Figure 2.4: Generalized ME system architecture.

Rao [2] *et.al.* were among the early researchers in the field of ME system. The ME system presented in [2] is based on generalized ME system architecture shown in Figure 2.4 and operates on feedback control technique. The capacity of the emulator is limited by the power rating and bandwidth of the system designed.

Amitkumar [26], has presented a versatile Power-Hardware-in-the-Loop (PHIL) motor emulator based on the generalized system architecture. The machine emulator system presented in [26] uses flux and torque lookup tables obtained from an FEA tool allowing the machine emulator to emulate a variety of transient conditions and mimic the machine magnetic (e.g., saturation) and geometric (e.g., torque ripple) behavior. The proposed machine emulator system in [26] uses a simple current control for the emulator system along with an inductive filter to connect the machine emulator with the driving inverter.

An FPGA based ME system for Interior PMSM motor is presented in [61]. The ME system presented here by Luo [61], consists of a SiC-based power converter with an inductive coupling, an RRTM for an IPM machine implemented in FPGA iterating at 1 MHz, and a hybrid CCS-MPC current controller which can accurately track the emulated motor current, including its ripple contents. The developed gate stitching modulation scheme for the ME power converter synchronizes the switching states of ME and IUT to avoid current spikes in the system. The gate stitching strategy, when combined with the MPC, enables high control bandwidth without the need for excessively high switching frequency or complex topology. The high-bandwidth of the current controller enables a high dc bus voltage to line inductance ratio that allows the use of a small line inductor.

Various ME system configuration with common AC bus are presented in [62] by Lee. The ME system architecture presented by Lee makes use of dual active bridge (DAB) power converter. Here a power circu- lation method is proposed, which utilizes high frequency three phase AC. Thus, the transformer size is reduced greatly when it is compared

with 60 Hz. Since the proposed method relies on the three phase, it is more cost effective than a system using DAB. Due to the sinusoidal nature, currents have less harmonics, thereby a normal silicon steel transformer can be used.

An another ME system based on generalized common AC bus architecture is evaluated by Masadeh [63]. The proposed ME emulates an induction motor (IM) with main and leakage flux saturation. Experimental procedures to obtain the magnetic saturation characteristics in the main and leakage flux paths for the 5-hp IM are discussed in this paper. The dq-model of the IM was modified by including the main and leakage saturation effects.

An signal transmission delay compensation control strategy is presented by Xie in [64]. This paper has proposed a compensation scheme for the signal transmission delay to improve the accuracy of a motor emulator in a boosted wide speed range of the emulated motor. The signal transmission delay comes from the PWM voltage sampling and the discrete position signal updating of the ME, which are inevitable in realistic emulator system which is with separated controllers for motor emulator and inverter under test. Such a transmission delay will cause cross coupling between dq axis and brings inaccuracy to the system. This influence is proportional to the emulated motor speed so that it will be much more severe for higher speed of emulated motor. Sampling period averaging method along with synchronization are implemented to ensure a constant delay during voltage sampling. A virtual encoder is proposed to continue the discrete updated rotor position signal and ensure a constant time delay during position signal transmission.

Numerous researchers have proposed 3-ϕ AC-DC converter topologies with buck, boost, buck-boost mode of operation [65]–[74]. A detailed review of three-phase AC-DC converter is presented in [75].

A 3-ϕ step-down bi-directional AC-DC converter topology was proposed in [66]. A similar approach can be considered for 3-ϕ bi-directional AC-DC buck-boost converter.

However, this would require twelve power semiconductor switches. A single-switch three-phase AC-DC converter topology was proposed in [67] and an upgraded topology was proposed in [68].

Another single switch buck-boost three-phase AC-DC converter topology was proposed in [69]. The thee-phase diode bridge-rectifier, used in these topologies would block reverse power flow in braking mode.

Thus, AC-DC converter with diode bridge rectifier, makes them unsuitable for ME system. A three-phase single-stage AC-DC PWM full bridge converter was proposed in [70]. Although single-stage AC-DC conversion is possible, only buck operation provided by this topology is not desired for ME application.

Another interesting converter topology providing low current THD was proposed in [71] consisting of buck-boost inductor in each leg of converter bridge. An isolated bi-directional AC-DC converter topology comprising of eighteen power semiconductor switches was proposed in [72], [73]. However, isolated converter topology is unsuitable for ME, as for low speed emulation, the isolation transformer's coil magnetization is insufficient to generate secondary voltage, resulting in poor emulation performance.

These factors associated with aforementioned converter topologies, highly demand a reduced switch, bi-directional, non-isolated AC-DC converter topology. In addition, single-stage reverse power control is also desired. Hence, for common DC bus ME application, with little modification in the 3-ϕ AC-DC converter topology presented in [74], a virtually isolated bi-directional buck-boost AC-DC converter topology is presented here.

2.6 Summary

In this chapter, state-of-the-art of motor emulator systems based on converter topologies, architecture, and control schemes are presented. As mentioned in the research objectives, the primary focus of this research work is to improve the motor emulator architecture, and propose a suitable converter topology for ME system. Therefore, this chapter explores all the possible AC-AC and AC-DC converter topologies suitable for ME application.

Chapter 3

Design of Proposed Bidirectional Three-Phase AC-DC Converter

THE 3-ϕ AC-DC converter are popular in electrical and power electronics field for quite a long time. However, as discussed in previous chapter, the conventional three-phase AC-DC topology is not suitable especially in case of common DC bus ME application. In case of ME, the converter is desired to operate in bi-directional buck-boost mode. This is because the ME, emulating the behavior of a machine should be able to allow bi-directional power flow to replicate its four quadrant operation as represented in Figure 3.1.

In any rotating machine, the four quadrant operation is primarily based on direction of speed and torque, as shown in Figure 3.1 graphically. However, physical rotating machine is absent in ME. Therefore, for understanding the principle of operation, direction of electrical equivalent quantities of speed and torque i.e. voltage and current respectively are used. Figure 3.1, graphically represents the direction of mechanical quantities and their equivalent electrical quantities in case of ME system. Referring to Figure 3.1, a ME is

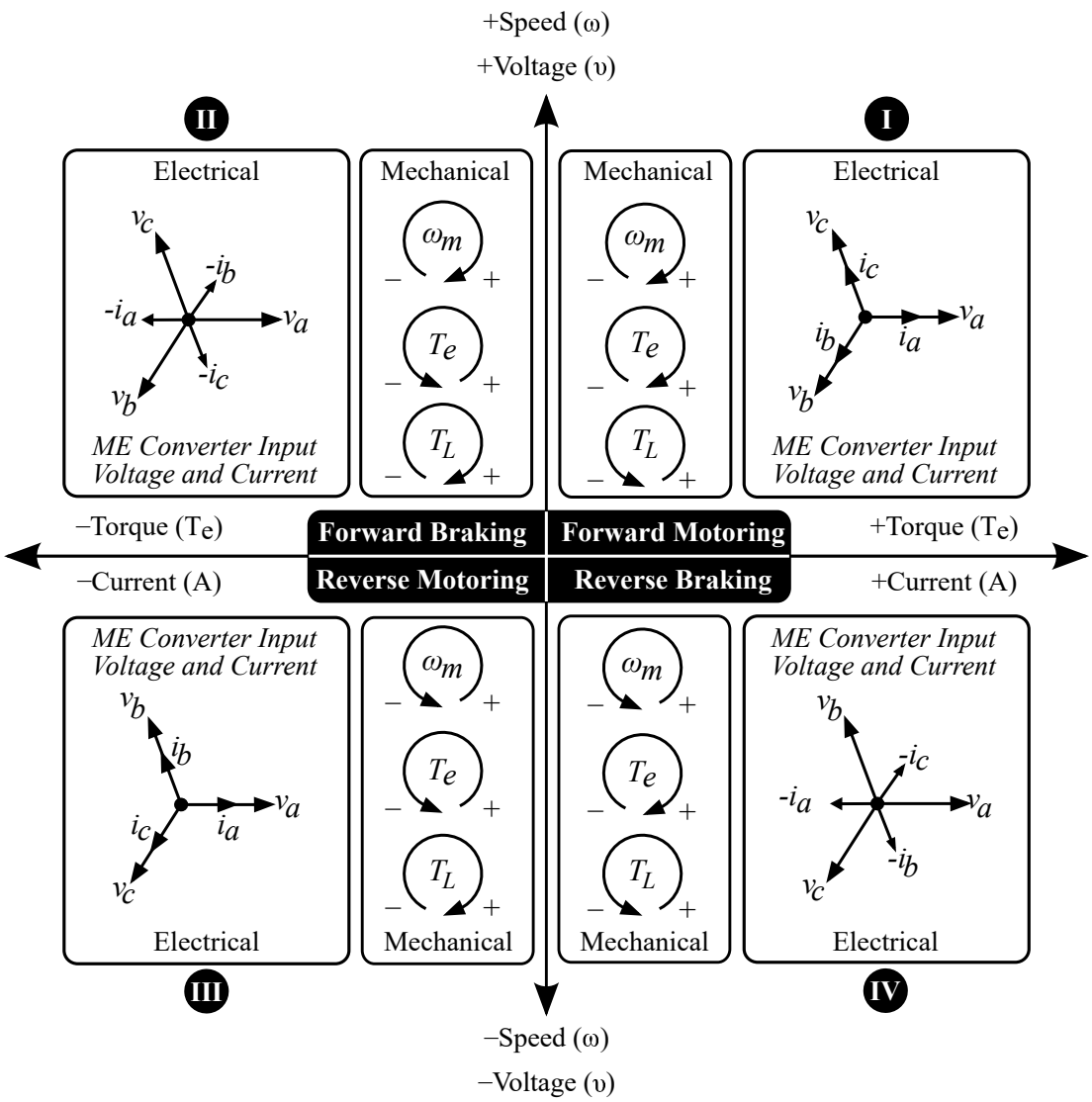

Figure 3.1: Four quadrant graphical representation of electrical and mechanical quantities of AC machine [36].
(ω_m : mechanical speed; T_e : electromechanical torque; T_L : load torque)

operating in quadrant - I, i.e forward motoring, when DUT output voltage and current are in-phase. In other word, when the direction of current is from DUT to ME. Whereas, it is operating in forward braking mode, i.e. quadrant - II, when the direction of current flow is from ME to DUT. During Forward braking, regenerative power is being fed back to drive.

3.1 Proposed Converter Topology

Numerous researchers have proposed 3-ϕ AC-DC converter topologies with buck, boost, buck-boost mode of operation [65]–[74]. A detailed review of three-phase AC-DC converter is presented by in [75]. A 3-ϕ step-down bi-directional AC-DC converter topology was proposed in [66]. A similar approach can be considered for 3-ϕ bi-directional AC-DC buck-boost converter. However, this would require twelve power semiconductor switches. A single-switch three-phase AC-DC converter topology was proposed in [67] and an upgraded topology was proposed in [68]. Another single switch buck-boost three-phase AC-DC converter topology was proposed in [69]. The thee-phase diode bridge-rectifier, used in these topologies would block reverse power flow in braking mode. Thus, AC-DC converter with diode bridge rectifier, makes them unsuitable for ME system. A three-phase single-stage AC-DC PWM full bridge converter was proposed in [70]. Although single-stage AC-DC conversion is possible, only buck operation provided by this topology is not desired for ME application. Another interesting converter topology providing low current THD was proposed in [71] consisting of buck-boost inductor in each leg of converter bridge. An isolated bi-directional AC-DC converter topology comprising of eighteen power semiconductor switches was proposed in [72], [73]. However, isolated converter topology is unsuitable for ME, as for low speed emulation, the isolation transformer's coil magnetization is insufficient to generate secondary voltage, resulting in poor emulation performance.

These factors associated with aforementioned converter topologies, highly demand a reduced switch, bi-directional, non-isolated AC-DC converter topology. In addition, single-stage reverse power control is also desired. Hence, for common DC bus ME application, with little modification in the 3-ϕ AC-DC converter topology presented in [74], a virtually isolated bi-directional buck-boost AC-DC converter topology is presented here.

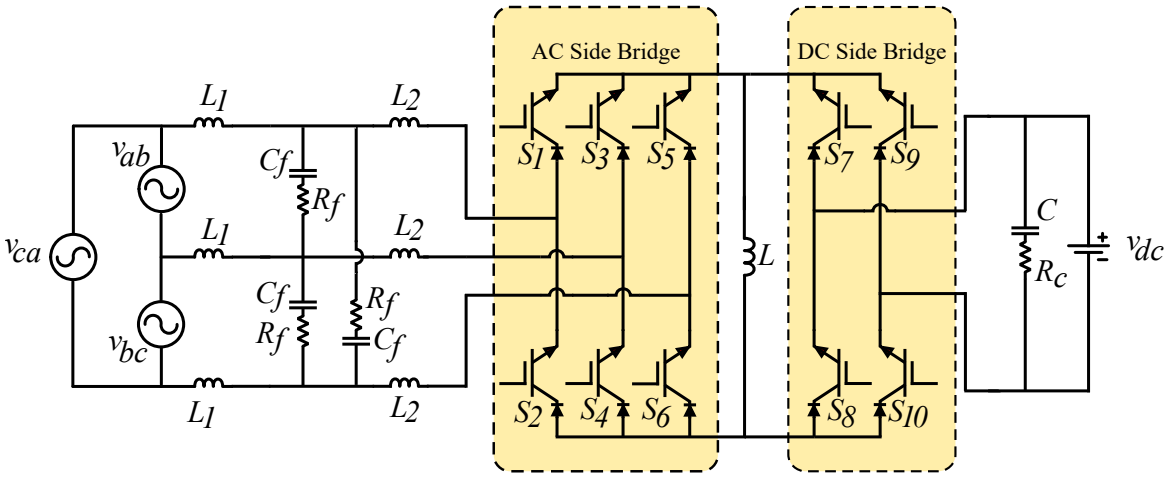

Figure 3.2: Proposed bi-directional buck-boost 3-ϕ AC-DC converter.

The proposed converter topology is presented in Figure 3.2. For simple understanding of proposed converter operation, detailed schematic of common DC bus ME system along with proposed converter, control strategy and PMSM model are not shown here. The detailed ME structure along with the proposed converter topology will be discussed in Chapter – 5. Referring to Figure 3.2, three-phase unfiltered voltages, v_{ab}, v_{bc} and v_{ca} from DUT are applied as input to the proposed converter. On the output side, there is common DC bus, v_{dc}, which connects both ME output and DUT input. It is to be noted that, throughout this thesis, v_{dc} represents common DC bus voltage. Inductor L is buck-boost inductor, capacitor C is DC link capacitor.

3.1.1 Virtual Isolation

The operation of proposed converter is discussed based on SVPWM (space vector pulse width modulation) technique. It is a well known phenomenon that, a SVPWM cycle comprises of two active vectors and one zero (null) vector. This phenomenon is used to achieve virtual isolation between the three-phase AC and DC sides of the proposed converter. During the active states as shown in Figure 3.3, DC side full bridge of the proposed converter is virtually isolated as it is kept OFF for the entire active state duration.

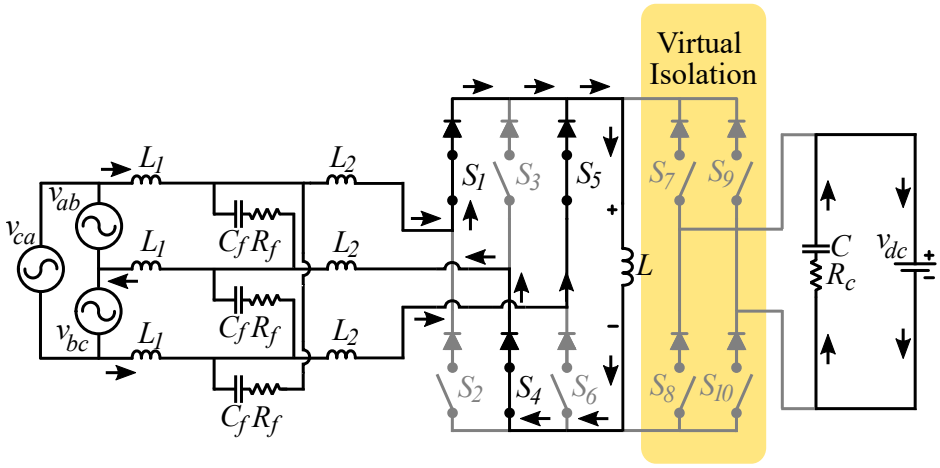

Figure 3.3: Virtual isolation during active switching state.

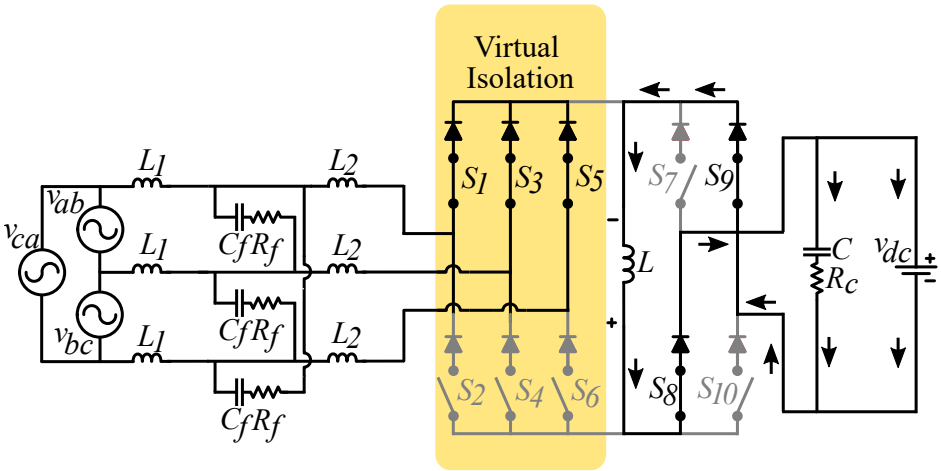

Figure 3.4: Virtual isolation during zero switching state.

Whereas, during zero state, the energy stored in buck-boost inductor is dissipated into common DC bus through DC side full bridge as shown in Figure 3.4. While in zero state, either all upper or lower switches from AC side three-phase bridge are ON, resulting in virtual isolation from DC side full bridge. The AC side converter switches S_1 to S_6 forms a two-level PWM converter converting 3-ϕ input AC voltage from DUT to DC which appears across the buck-boost inductor L. At any instant the voltage appearing across inductor L is –

$$v_l = \sqrt{3} \cdot v_i$$

where, $v_i = v_a = v_b = v_c$ input phase voltage.

3.1.2 Quadrant – I : Forward Motoring

In *forward motoring* operation, switch S_7 and S_{10} are kept *OFF* for the entire duration of *forward motoring* mode. In this mode of operation, energy is stored in buck-boost inductor L during active state. The current flow path for active state 101 is shown in Figure 3.5.

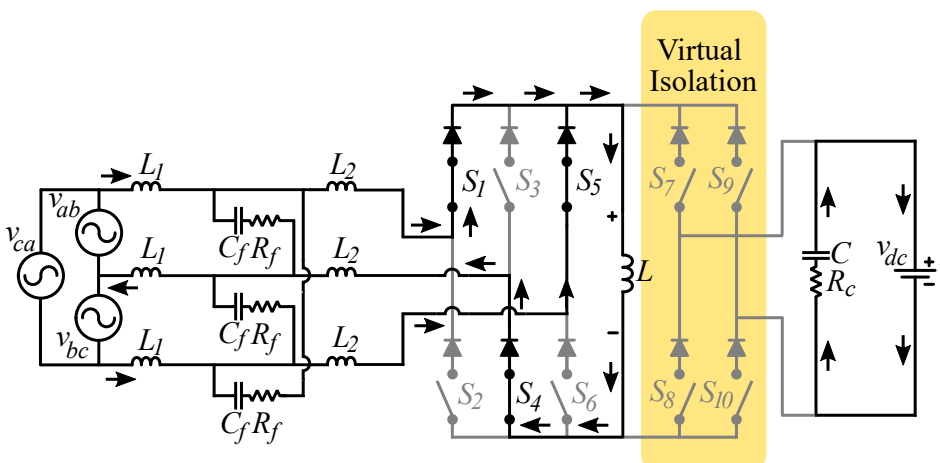

Figure 3.5: Forward motoring operation during active switching state - 101.

During active state as shown in Figure 3.5, based on the SVPWM control algorithm, the switches on AC side bridge turn *ON* and *OFF*, storing energy of the magnitude of v_l in inductor L.

$$v_l = L \times \frac{\delta i_l}{\delta t} \tag{3.1}$$

where, i_l is current through inductor L.

The rise in inductor current I_l during both the active states is given by –

$$\Delta i_l(+) = \frac{(\sqrt{3} \cdot v_i - i_l \cdot R_l)}{L} \times T_{ON} \tag{3.2}$$

where, T_{ON} = $T_1 + T_2$, sum of two active vectors duration as shown in Figure 3.6.

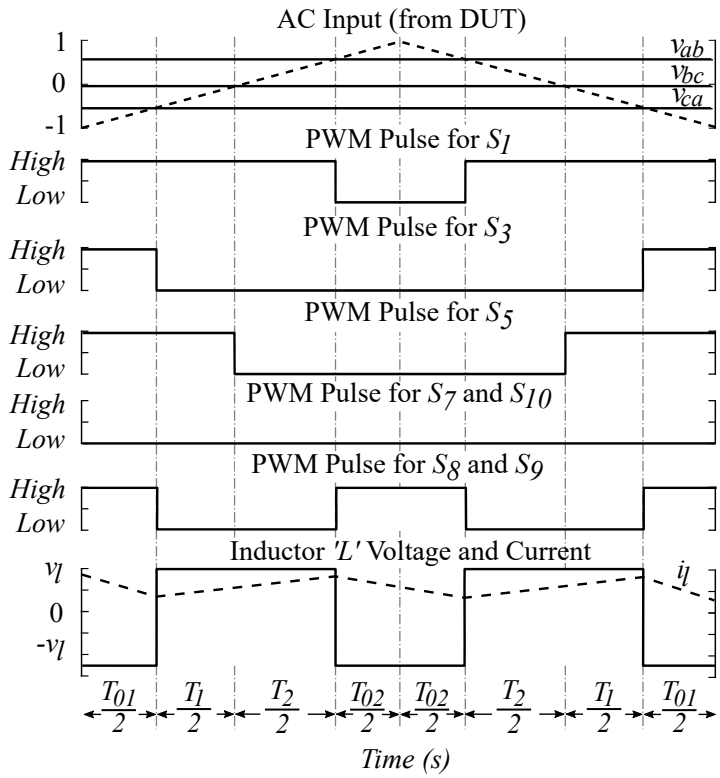

Figure 3.6: SVPWM switching pattern for forward motoring.

For simplicity, the negligible voltage drop across switches is not considered here. The highlighted box in Figure 3.5 shows the virtual isolation in proposed topology during active SVPWM (Space Vector PWM) states which isolates the DC link capacitor from buck-boost inductor. The SVPWM switching pattern for forward motoring operation is shown in Figure 3.6.

During zero-state, as shown in Figure 3.7, the polarity of inductor L reverses and the stored energy in L, dissipates through $L(+) \rightarrow S_8 \rightarrow v_{dc} \rightarrow S_9 \rightarrow L(-)$, performing forward motoring operation. During forward motoring, DC bus act as '*sink*', as the forward current flows into the DC bus v_{dc}.

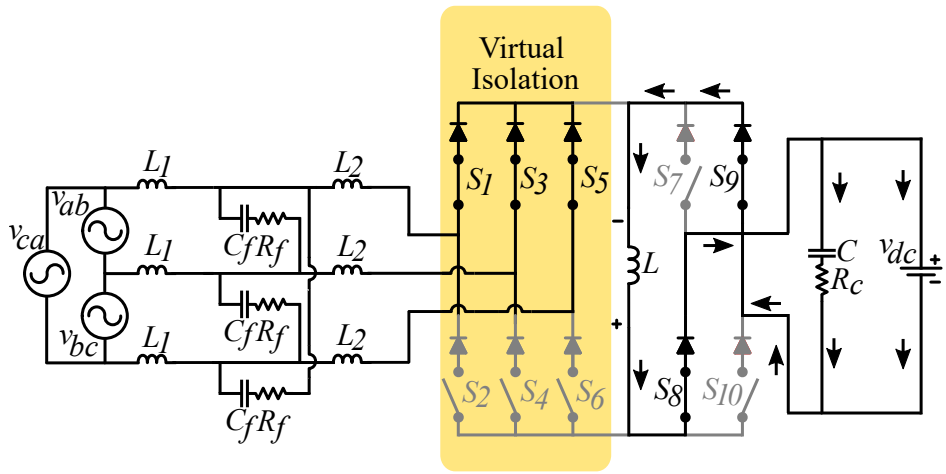

Figure 3.7: Forward motoring operation during zero switching state - 111.

The fall in inductor current i_l during zero switching state is given by –

$$\Delta i_l(-) = \frac{(v_C - i_l \cdot R_l)}{L} \times T_{OFF} \tag{3.3}$$

where, T_{OFF} = T_0 = $T_{01} + T_{02}$, zero switching state duration.

For steady-state operation, the rise in inductor current $\Delta i_l(+)$ and fall in inductor current $\Delta i_l(-)$ should be equal. Otherwise the cumulative increase or decrease in inductor current over a number of switching cycles would result in unstable condition. Therefore, by equating (3.2) and (3.3), output voltage for forward motoring operation i.e. capacitor voltage v_C can be estimated as –

$$v_C = \sqrt{3} \cdot v_i \times \frac{T_{ON}}{T_{OFF}} \tag{3.4}$$

where, $v_i = v_{ab} = v_{bc} = v_{ca}$ phase voltage.

Here, the impedance R_l of inductor L is small enough to be neglected. Therefore, second term $I_l \cdot R_l$ in (3.2) and (3.3) are neglected in (3.4). The steady-state output voltage

equation (3.4) can therefore be rewritten as –

$$v_C = \sqrt{3}\frac{D}{(1-D)}v_i \tag{3.5}$$

where,

$$D = \frac{T_{ON}}{T_s}, \quad (1-D) = \frac{T_{OFF}}{T_s}\text{, and} \quad T_s = T_{ON} + T_{OFF}$$

3.1.3 Quadrant – II : Forward Braking

In *forward braking* operation, the torque direction reverses while speed direction remains same as that of *forward motoring*. However, during this mode of operation the DUT output voltage and current are $180°$ out of phase. This results in reverse current flow from DC side of the converter to AC side. During this mode of operation, switches S_8 and S_9 are kept continuously *OFF* while switches S_7 and S_{10}, are switched *ON* and *OFF* simultaneously during zero switching state. This causes the current to flow from DC side source $v_c(+) \rightarrow S_7 \rightarrow L \rightarrow S_{10} \rightarrow V_c(-)$, completing the closed path as shown in Figure 3.8. As the current flows through inductor L, an energy of the magnitude of v_l is stored in it.

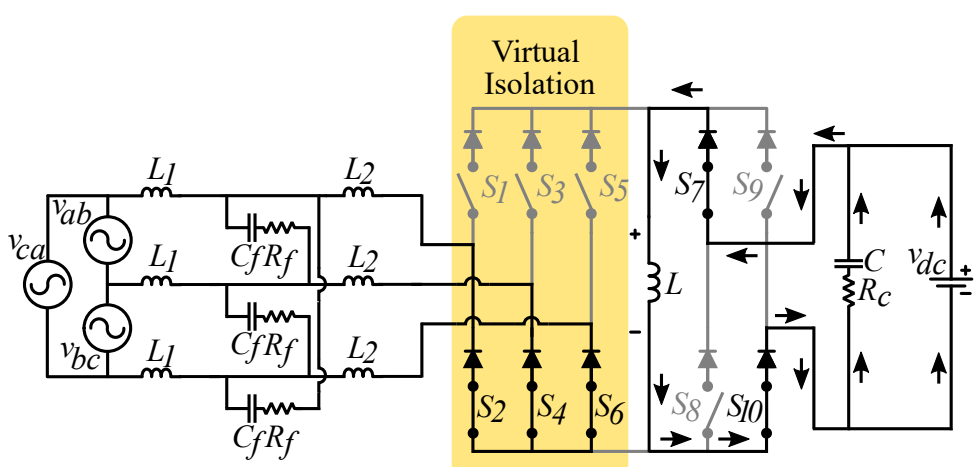

Figure 3.8: Forward braking operation during zero switching state - 000.

The rise in current $i_l(+)$ during this period is given by–

$$\Delta i_l(+) = \frac{(v_C - i_l \cdot R_l)}{L} \times T_{OFF} \tag{3.6}$$

This stored energy in inductor *L*, then dissipates stored energy through AC side converter switches. For the duration of forward breaking, according to control strategy implemented, the AC sided bridge switching allows reverse flow of current back to DUT as shown in Figure 3.9. At the same time, according to the control algorithm for DUT, ME terminal voltage is maintained positive with respect to the reference voltage. The fall in inductor current i_l during both the active states is given by –

$$\Delta i_l(-) = \frac{(\sqrt{3} \cdot v_i - i_l \cdot R_l)}{L} \times T_{ON} \tag{3.7}$$

Solving (3.6) and (3.7) for output voltage in forward braking operation, i.e. v_{phase} in this case, gives –

$$v_i = \frac{1 - D}{\sqrt{3} \cdot D} v_C \tag{3.8}$$

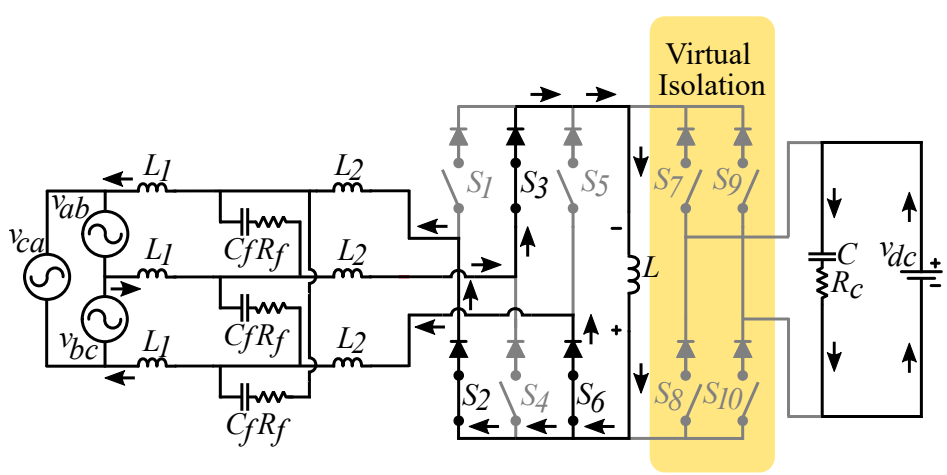

Figure 3.9: Forward braking operation during active switching state - 010.

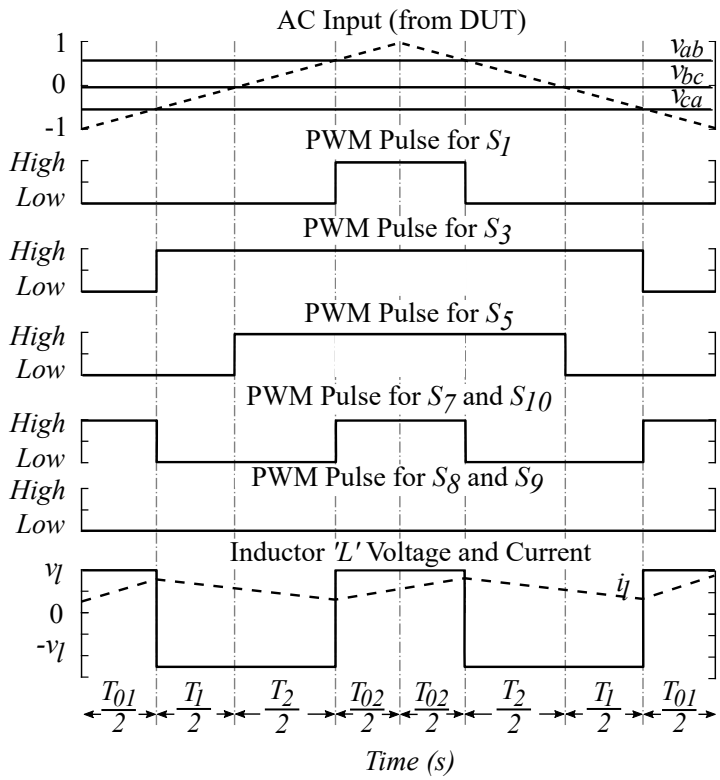

Figure 3.10: SVPWM switching pattern for forward braking.

The switching patterns during forward breaking operation is shown in Figure 3.10. As opposed to forward-motoring, in forward-braking mode, the energy is stored in inductor L during zero switching state. Whereas, it is dissipated during active switching state.

3.1.4 Quadrant – III : Reverse Motoring

In *reverse motoring* operation, switch S_7 and S_{10} are kept *OFF* for the entire duration of *reverse motoring* mode. In this mode of operation, energy is stored in buck-boost inductor L during active state. The current flow path for active state 101 is shown in Figure 3.11.

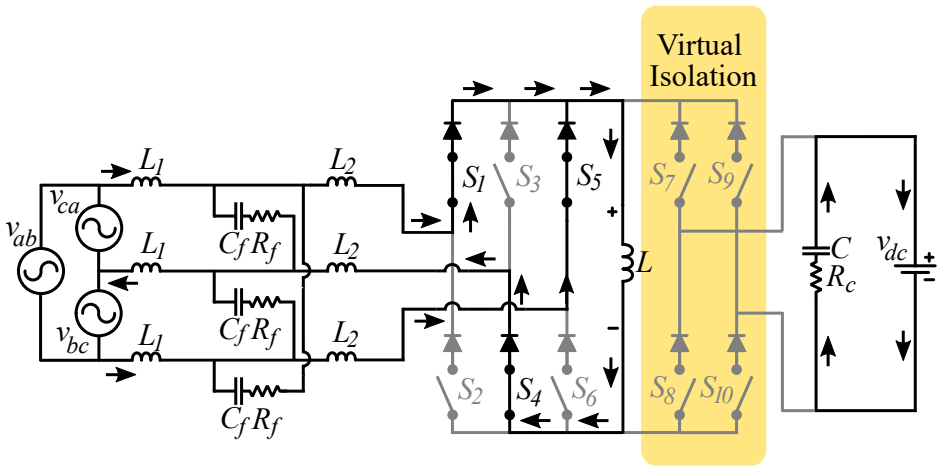

Figure 3.11: Reverse motoring operation during active switching state - 101.

During active state as shown in Figure 3.11, based on the SVPWM control algorithm, the switches on AC side bridge turn *ON* and *OFF*, storing energy of the magnitude of v_l in inductor L.

$$v_l = L \times \frac{\delta i_l}{\delta t} \tag{3.9}$$

where, i_l is current through inductor L.

The rise in inductor current I_l during both the active states is given by –

$$\Delta i_l(+) = \frac{(\sqrt{3} \cdot v_i - i_l \cdot R_l)}{L} \times T_{ON} \tag{3.10}$$

where, T_{ON} = $T_1 + T_2$, sum of two active vectors durations. For simplicity, the negligible voltage drop across switches is not considered here.

During zero-state, as shown in Figure 3.12, the polarity of inductor L reverses and the stored energy in L, dissipates through $L(+) \rightarrow S_8 \rightarrow v_{dc} \rightarrow S_9 \rightarrow L(-)$, performing forward motoring operation. During reverse motoring, DC bus act as '*sink*', as the forward current flows into the DC bus v_{dc}.

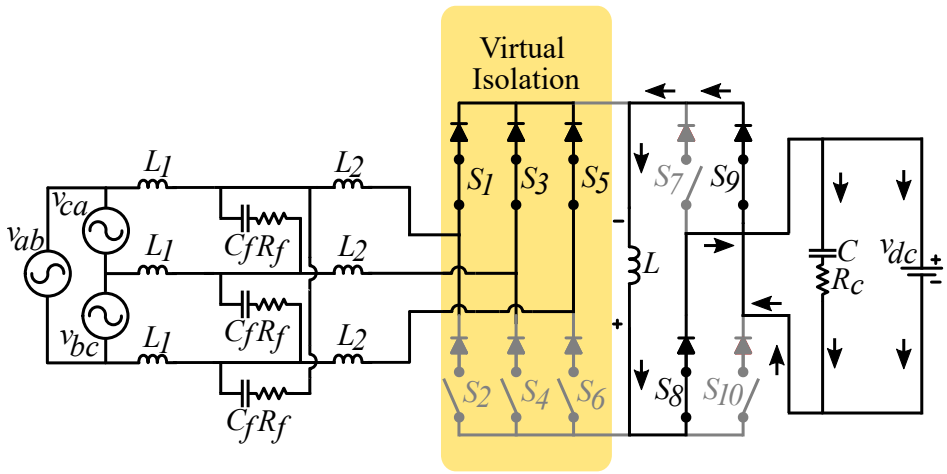

Figure 3.12: Reverse motoring operation during zero switching state - 111.

The fall in inductor current i_l during zero switching state is given by –

$$\Delta i_l(-) = \frac{(v_C - i_l \cdot R_l)}{L} \times T_{OFF} \tag{3.11}$$

where, T_{OFF} = T_0 = $T_{01} + T_{02}$, zero switching state duration.

For steady-state operation, the rise in inductor current $\Delta i_l(+)$ and fall in inductor current $\Delta i_l(-)$ should be equal. Otherwise the cumulative increase or decrease in inductor current over a number of switching cycles would result in unstable condition. Therefore, by equating (3.2) and (3.3), output voltage for forward motoring operation i.e. capacitor voltage v_C can be estimated as –

$$v_C = \sqrt{3} \cdot v_i \times \frac{T_{ON}}{T_{OFF}} \tag{3.12}$$

where, $v_i = v_{ab} = v_{bc} = v_{ca}$ phase voltage.

Here, the impedance R_l of inductor L is small enough to be neglected. Therefore, second term $I_l \cdot R_l$ in (3.10) and (3.11) are neglected in (3.12). The steady-state output voltage equation (3.12) can therefore be rewritten as –

$$v_C = \sqrt{3}\frac{D}{(1-D)}v_i \tag{3.13}$$

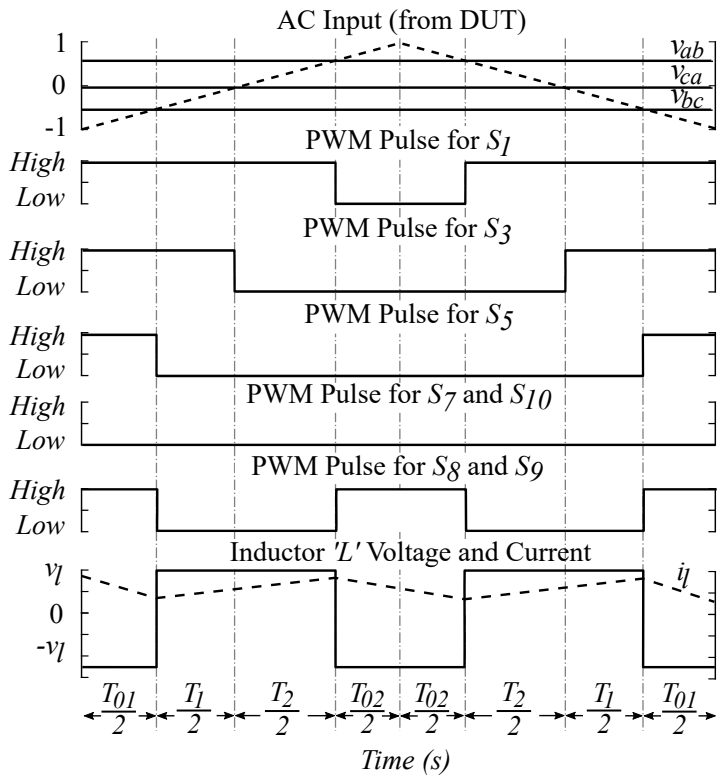

Figure 3.13: SVPWM switching pattern for reverse motoring.

The SVPWM switching pattern for reverse motoring operation is as shown in Figure 3.11.

3.1.5 Quadrant – IV : Reverse Braking

In *reverse braking* operation, the torque direction reverses while speed direction remains same as that of *reverse motoring*. However, during this mode of operation the DUT output voltage and current are $180°$ out of phase. This results in reverse current flow from DC side of the converter to AC side. During this mode of operation, switches S_8 and S_9 are kept continuously *OFF* while switches S_7 and S_{10}, are switched *ON* and *OFF*

simultaneously during zero switching state. This causes the current to flow from DC side source $v_c(+) \rightarrow S_7 \rightarrow L \rightarrow S_{10} \rightarrow V_c(-)$, completing the closed path as shown in Figure 3.14. As the current flows through inductor L, an energy of the magnitude of v_l is stored in it. The rise in current $i_l(+)$ during this period is given by–

$$\Delta i_l(+) = \frac{(v_C - i_l \cdot R_l)}{L} \times T_{OFF} \tag{3.14}$$

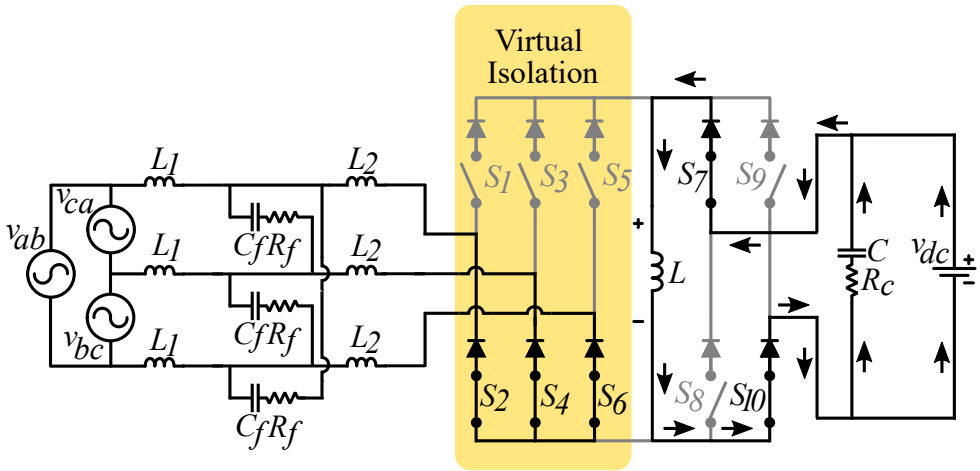

Figure 3.14: Reverse braking operation during zero switching state - 000.

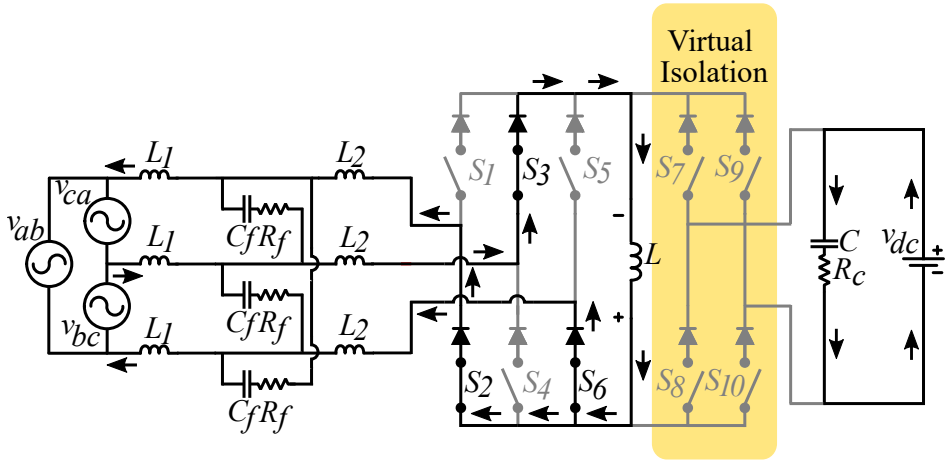

Figure 3.15: Reverse braking operation during active switching state - 010.

This stored energy in inductor L, then dissipates stored energy through AC side converter switches. For the duration of reverse breaking, according to control strategy implemented, the AC sided bridge switching allows reverse flow of current back to DUT as shown in Figure 3.15. At the same time, according to the control algorithm for DUT, ME terminal voltage is maintained positive with respect to the reference voltage. The fall in inductor current i_l during both the active states is given by –

$$\Delta i_l(-) = \frac{(\sqrt{3} \cdot v_i - i_l \cdot R_l)}{L} \times T_{ON} \tag{3.15}$$

Solving (3.14) and (3.15) for output voltage in forward braking operation, i.e. v_{phase} in this case, gives –

$$v_i = \frac{1 - D}{\sqrt{3} \cdot D} v_C \tag{3.16}$$

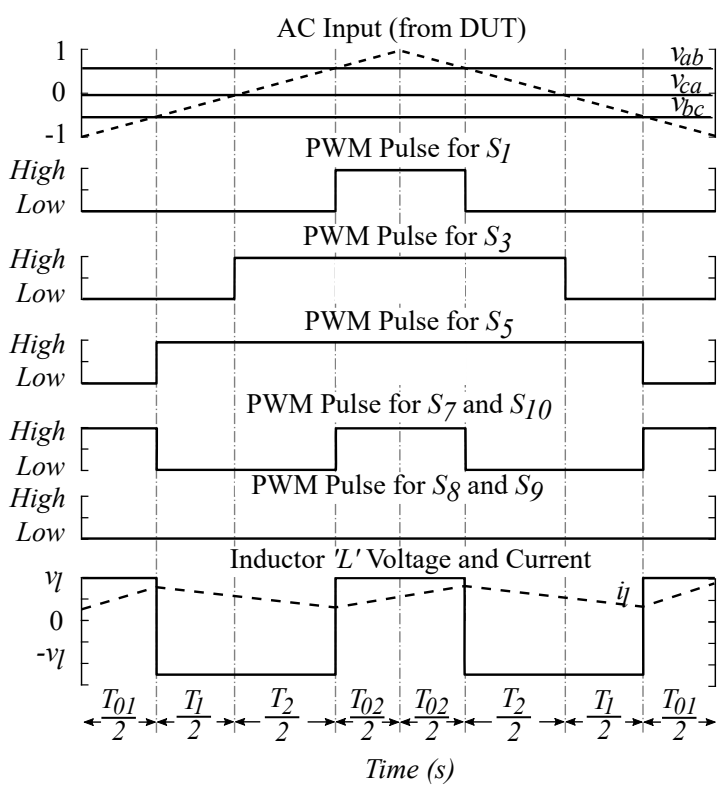

Figure 3.16: SVPWM switching pattern for reverse braking.

The switching patterns during reverse breaking operation is shown in Figure 3.16. As opposed to reverse-motoring, in reverse-braking mode, the energy is stored in inductor L during zero switching state. Whereas, it is dissipated during active switching state.

3.1.6 Voltage Gain

The voltage gain expression for motoring operation can be derived from (3.5) and (3.13) as–

$$\therefore A_{v,m} = \frac{v_c}{v_i} = \sqrt{3}\frac{D}{(1-D)} \tag{3.17}$$

The gain expression derived in (3.17) is valid for motoring operation during first and third quadrant. Similarly, voltage gain ($A_{v,b}$) for braking operation can be derived from (3.8) and (3.16) as –

$$A_{v,b} = \frac{v_i}{v_c} = \frac{1}{\sqrt{3}}\frac{(1-D)}{D} \tag{3.18}$$

The voltage gain curves, for expressions derived in (3.17) and (3.18), for motoring as well as braking modes of operation respectively, are shown in Figure 3.17. The gain curves are plotted for duty cycle D ranging from 0.1 to 0.8. This is because of the theoretically infinite

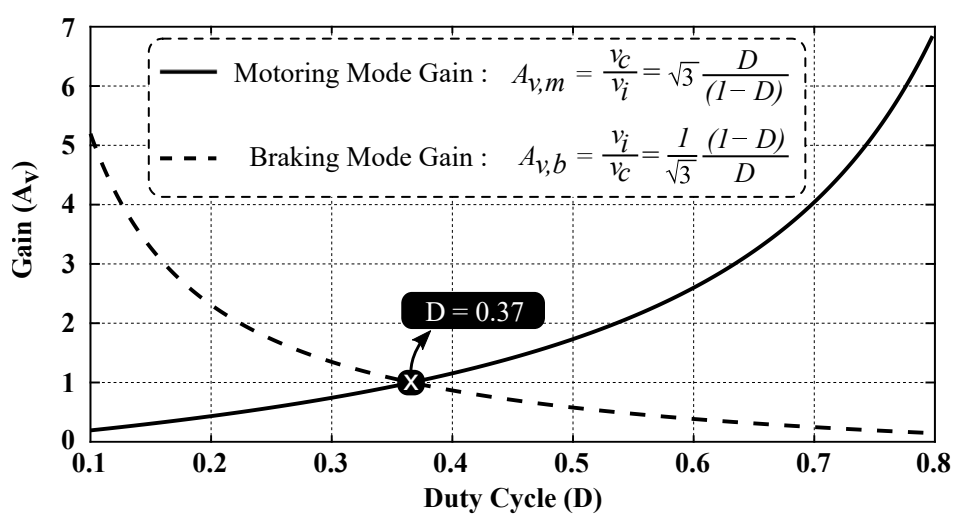

Figure 3.17: Theoretical voltage gain curve for motoring and braking mode of operation.

gain possible above $D = 0.8$, using (3.17) and below $D = 0.1$, using (3.18). As shown in Figure 3.17, the buck to boost and vice-versa crossover occurs at $D = 0.37$ duty cycle.

3.2 Converter Design

Design is the very important aspect for achieving desired output, for any power converter. The proposed bidirectional converter consist of an energy storage element between AC and DC sides switching bridge serving as buck-boost inductor and a LCL filter between DUT and AC side input terminals of converter. In addition to these components, a capacitor on DC side serve as DC link element.

3.2.1 LCL Filter Design

The LCL filter is designed following the procedure provided in [76] and [77] and therefore the design formulas are not repeated here. The initial assumptions made for the design of LCL filter are as listed in TABLE – 3.1.

TABLE – 3.1
INITIAL CONVERTER DESIGN ASSUMPTIONS

Parameter	Symbol	Value
DC Bus Voltage	v_{dc}	500.00 V
Line to Line RMS Voltage	V_{ll}	208.00 V
Nominal Frequency	f_n	60.00 Hz
DUT Switching Frequency	$f_{sw,DUT}$	10.00 kHz
ME Switching Frequency	$f_{sw,ME}$	25.00 kHz
Output Power	P_o	10.00 kW

The base impedance is defined by (3.19). Thus, the filter values will be referred to in a percentage of the base values:

$$Z_b = \frac{V_{ll}^2}{P_o} \tag{3.19}$$

$$Z_b = \frac{(208\ \ V)^2}{10\ \ kW} \tag{3.20}$$

$\therefore$ the base impedance is –

$$Z_b = 4.33\ \ \Omega \tag{3.21}$$

Similarly, The base capacitance is defined by (3.22).

$$C_b = \frac{1}{\omega_b \times Z_b} \tag{3.22}$$

where, $\omega_b = 2 \times \pi \times f_n$

$$C_b = \frac{1}{2 \times \pi \times 60\ \ Hz \times 4.33\ \ \Omega} \tag{3.23}$$

$\therefore$ the base capacitance is –

$$C_b = 613.12\ \ \mu F \tag{3.24}$$

For the design of the filter capacitance, it is considered that the maximum power factor variation on output voltage is 5%. Therefore the Filter Capacitance is designed as –

$$C_f = 0.05 \times C_b \tag{3.25}$$

$\therefore$ the filter capacitance is –

$$C_f = 30.66\ \ \mu F \tag{3.26}$$

The maximum current ripple at the AC side of the proposed converter is given by –

$$\Delta I_{Lmax} = \frac{2 \times V_{DC}}{3 \times L_1} \times (1 - m) \cdot m \cdot T_{sw,dut} \tag{3.27}$$

where m is the modulation factor.

The maximum peak to peak current ripple is estimated by –

$$\Delta I_{Lmax} = \frac{V_{DC}}{6 \times f_{sw,dut} \times L_1} \tag{3.28}$$

where L_1 is the DUT side inductor.

For 10% current ripple with respect to rated current for the design parameters is given by –

$$\Delta I_{Lmax} = 0.1 \times I_{max} \tag{3.29}$$

where

$$I_{max} = \frac{\sqrt{2} P_o}{3 \times V_{ph}} \tag{3.30}$$

Substituting (3.29) in (3.28) and rearranging to dervie L_1 –

$$L_1 = \frac{V_{DC}}{6 \times f_{sw,dut} \times 0.1 \times I_{max}} \tag{3.31}$$

Therefore,

$$L_1 = \frac{500 \ \ V}{6 \times 5 \ \ kHz \times 0.1 \times 39.25 \ A} \tag{3.32}$$

$$L_1 \approx 2.1 \ \ mH \tag{3.33}$$

The ME side filter inductor, L_2 is estimated by

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2} + 1}}{C_f \omega_{sw}^2} \tag{3.34}$$

where, k_a^2 is the desired attenuation. Considering 20% attenuation, the inductor L_2 is estimated as –

$$L_2 = \frac{\sqrt{\frac{1}{(0.2)^2} + 1}}{(30.66\ \mu F) \times (2\pi \times 10\ kHz)^2} \tag{3.35}$$

$$L_2 \approx 49.58\ \ \mu H \tag{3.36}$$

A resistor in series R_f with the filter capacitor C_f attenuates part of the ripple on the switching frequency in order to avoid the resonance. The value of this resistor should be one third of the impedance of the filter capacitor at the resonant frequency [78].

The resistor in series with the filter capacitance is given by –

$$R_f = \frac{1}{3\omega_{res} C_f} \tag{3.37}$$

where,

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{3.38}$$

Substituting (3.26), (3.33), and (3.36) in (3.38), the ω_{res} is calculated as –

$$\omega_{res} = \sqrt{\frac{2.1\ \ mH + 49.58\ \ \mu H}{2.1\ \ mH \times 49.58\ \ \mu H \times 30.66\ \ \mu F}} \tag{3.39}$$

Therefore,

$$\omega_{res} = 25949 \ \ rad/s \tag{3.40}$$

and,

$$f_{res} = \frac{\omega_{res}}{2\pi} = 4.13 \ \ kHz \tag{3.41}$$

The resonant frequency range must also satisfy the (3.42)

$$10 f_n < f_{res} < 0.5 f_{sw,dut} \tag{3.42}$$

It is evident that, the resonant frequency obtained from (3.40), satisfy the (3.42).

Substituting, (3.26) and (3.40) in (3.37), the series resistance with the filter capacitor can be estimated as –

$$R_f = \frac{1}{3 \times 25949 \ \ rad/s \times 30.66 \ \ \mu F} \tag{3.43}$$

$$R_f = 0.42 \ \ \Omega \tag{3.44}$$

3.2.2 Energy Storage Inductor (L)

For Buck mode, neglecting ESR and assuming $10 \ \%$ allowable current ripple, the energy storage inductor L can be estimated as –

$$L > \frac{V_{dc}}{\Delta I_{Lmax} \times f_{sw,ME}} \tag{3.45}$$

Here, ΔI_{Lmax} includes $10\ \%$ current ripple. From (3.45), the buck mode energy storage inductance is estimated as –

$$L > \frac{500}{3.925\ A \times 25\ kHz} = 5.1\ \ mH \tag{3.46}$$

Similarly, for boost mode –

$$L > \frac{\sqrt{3} \cdot v_i}{\Delta I_{Lmax} \times f_{sw,ME}} \tag{3.47}$$

Therefore,

$$L > \frac{\sqrt{3} \cdot 120}{3.928\ \ A \times 25\ kHz} = 2.12\ \ mH \tag{3.48}$$

where, v_i is input phase voltage from DUT.

For the design of converter, the inductor with higher inductance among (3.46) and (3.48) i.e. $5.1\ \ mH$ is selected.

3.2.3 DC Link Capacitor (C)

The size of DC link capacitor can be estimated using the expression for energy stored in the capacitor. The energy stored in capacitor is given by the relation $0.5Cv^2$. Using this relation the DC capacitor value can be estimated by –

$$C = \frac{2 \times P}{(v_{c,max} - v_{c,min})^2 \times f_{sw,ME}} \tag{3.49}$$

where, P is power capacity of the converter.

Considering $\pm 2\%$ voltage ripple and substituting other quantities in (3.49), the DC link capacitance can be estimated as –

$$C = \frac{2 \times 10000\ W}{(510\ V - 490\ V)^2 \times 25000\ Hz} \tag{3.50}$$

Therefore,

$$C = 2000\ \mu F \tag{3.51}$$

The design values derived in this section for proposed converter are as listed in TABLE – 3.2

TABLE – 3.2
CONVERTER PARAMETER DESIGN VALUES

Parameter	Symbol	Value
DC Bus Voltage	v_{dc}	500.00 V
Line to Line RMS Voltage	V_{ll}	208.00 V
Nominal Frequency	f_n	60.00 Hz
DUT Switching Frequency	$f_{sw,DUT}$	10.00 kHz
ME Switching Frequency	$f_{sw,ME}$	25.00 kHz
Output Power	P_o	10.00 kW
DUT Side Filter Inductor	L_1	2.10 mH
Filter Capacitor	C_f	30.66 μF
Filter Capacitor ESR	R_f	0.42 Ω
Emulator Side Filter Inductor	L_2	49.58 μH
Energy Storage Inductor	L	2.12 mH
DC Link Capacitor	C	2000.00 μF

The detailed mathematical analysis and transient responses for the proposed converter are presented in Chapter – 5.

3.3 Summary

In this chapter detailed operating principle of proposed bidirectional converter topology for common DC-bus-configured ME system is presented. The proposed converter operation during various quadrants is summarized in TABLE – 3.3. The design equations for LCL filter along with energy storage inductor and DC link capacitor are presented in previous section and the design values are tabulated in TABLE – 3.2.

TABLE – 3.3
SUMMARY OF PROPOSED CONVERTER SWITCHING

Parameter		Quadrant			
		I	II	III	IV
Torque Reference		Positive	Negative	Negative	Positive
Speed Reference		Positive	Positive	Negative	Negative
Operating Mode		Forward Motoring	Forward Braking	Reverse Motoring	Reverse Braking
Comparator Operator		$v_{tri} \leq v_i$	$v_{tri} \geq v_i$	$v_{tri} \leq v_i$	$v_{tri} \geq v_i$
Input Phase Difference	v_{ab}	$0°$	$0°$	$0°$	$0°$
	v_{bc}	$-120°$	$-120°$	$-240°$	$-240°$
	v_{ca}	$-240°$	$-240°$	$-120°$	$-120°$
Energy Storage in 'L'	*During*	Active Vector	Zero Vector	Active Vector	Zero Vector
	Through	S_1 to S_6	S_7 and S_{10}	S_1 to S_6	S_7 and S_{10}
Energy Dissipation from 'L'	*During*	Zero Vector	Active Vector	Zero Vector	Active Vector
	Through	S_8 and S_9	S_1 to S_6	S_8 and S_9	S_1 to S_6
DC Bus	*act as*	'Sink'	'Source'	'Sink'	'Source'

v_{tri}: triangular carrier signal; v_i: modulating input signal (where, *i = phase – a, b or c*)

Chapter 4

Development of Common DC-Bus-Configured ME System

THE proposed ME converter for design parameters listed in TABLE – 3.2, has been developed for experimental testing. The developed setup is as shown in Figure 4.1. As, drive under test (DUT), an off-the-shelf Semikron inverter module (SEMITEACH B6U) is used, which is controlled by Texas Instruments DSP TMS320F28379. High precision LEM voltage and current sensors are used for voltage and current sensing. The voltage sensor LV-20P has the capability of sensing $0 - 500\ V$ AC or DC voltage with sensed output up to $\pm 15\ V$. Similarly, current sensor LTS-25 from LEM used in developed setup can sense up to $25\ A$ AC or DC current with proportional output voltage varying from $0\ V$ to $5\ V$ DC. The proposed converter is developed using $600\ V/85\ A$ Reverse-Blocking IGBT (RB-IGBT) FGW85N60RB from Fuji Electric. Two RB-IGBT's are used in series at each switch place (S_1 to S_{10}) in proposed converter to make up for the desired voltage rating of $1200\ V$ of each switch. The controller used for proposed converter is TMS320F28335 from Texas Instruments Inc. Two DC power supplies of $500\ V,\ 5\ kW$ capacity are used in parallel to supply $10\ kW$ power to common DC bus. The experimental setup details are

listed in Table - 4.1.

TABLE – 4.1
LIST OF COMPONENTS AND LABORATORY EQUIPMENT USED FOR EXPERIMENTAL SETUP

	Part # (Manufacturer)	Ratings
Device Under Test (DUT)	SEMITEACH (Semikron)	750 V DC In 400 V AC Out
DUT Microcontroller	F28379 (Texas Instru.)	100 MHz
Voltage Sensor	LV–20P (LEM)	0-500 V AC/DC In ± 15 V AC Out
Current Sensor	LTS–25 (LEM)	25 A AC/DC In 0–5 V DC Out
Emulator Converter Power Switch	FGW85N60RB (Fuji Electric)	600 V / 85 A
Emulator Microcontroller	TMS320F28335 (Texas Instru.)	150 MHz
DC Power Supply	RP7951 (KEYSIGHT)	0-500 V DC 10 A 5 kW

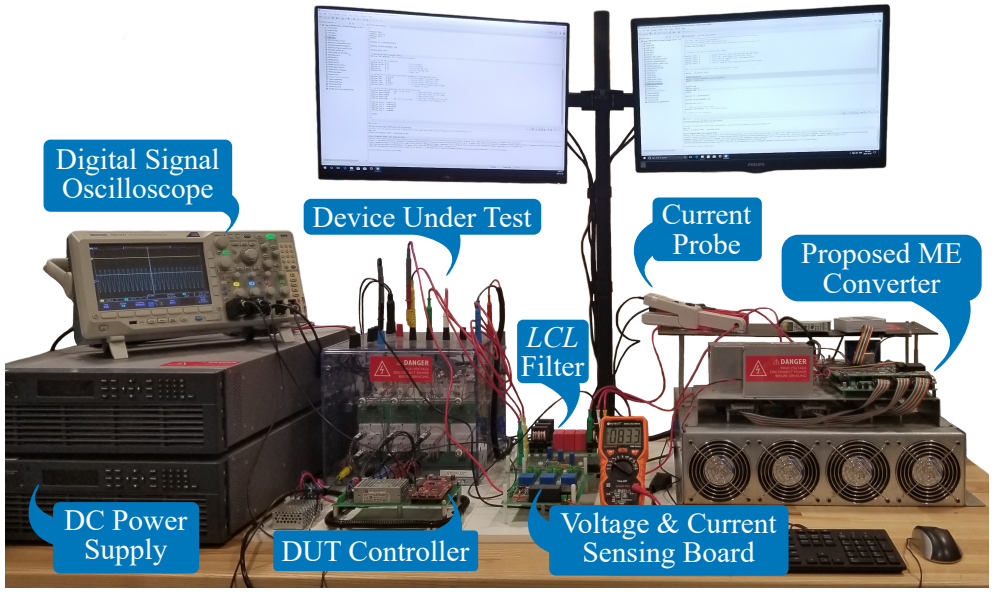

Figure 4.1: Hardware setup of proposed ME system.

4.1 Analog Front End

An analog front-end (AFE or analog front-end controller AFEC) is a set of analog signal conditioning circuitry that uses operational amplifiers, filters, and sometimes application-specific integrated circuits for sensors and other circuits to provide a configurable and flexible electronics functional block, needed to interface a variety of sensors to an analog to digital converter or in some cases to a micro-controller. AFE hardware modules are used as interface sensors of many kinds to digital systems, providing hardware modularity.

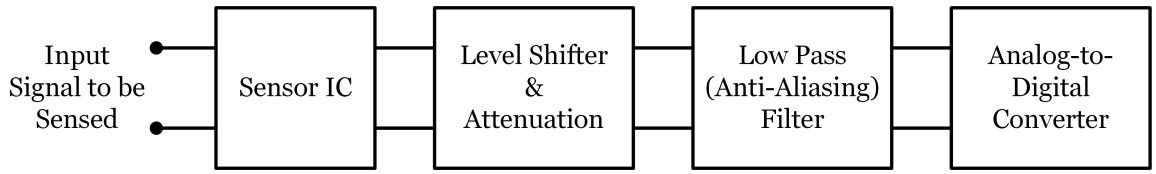

Figure 4.2: Basic block diagram of a Analog Front End (AFE)

Figure 4.2 shows the basic block diagram of the Analog Front End (AFE). A high magnitude analog signal to be converted into digital is first sensed using a sensor which gives the equivalent voltage with certain gain ratio at the output. This signal, if it is out side the voltage level of the ADC circuit (*3.3 V in case of LAUNCHPAD F28379*), has to be attenuated or amplified as required. This signal is then level shifted to fit into the envelop of accepted voltage level of ADC. A low pass filter (LPF) follows the level shifting stage to remove any unwanted noise from the signal. This LPF upon selecting a cut-off frequency such that, the sampling frequency is greater than or equal to the double of cut-off frequency, acts as a anti-aliasing filter (AAF). The filtered signal then goes into the ADC for the conversion.

The various stages in the AFE are briefly explained below -

- **Voltage/Current Sensor :** A current sensor is a device that detects electric voltage/current (AC or DC) in a wire, and generates a signal proportional to it. The generated signal could be analog voltage or current or even digital output. It can be then utilized to display the measured current in an ammeter or can be stored for further analysis in a data acquisition system or can be utilized for control purpose.

- **Attenuation :** Attenuation is a general term that refers to any reduction in the strength of a signal. Attenuation occurs with any type of signal, whether digital or analog. Sometimes called loss, attenuation is a natural consequence of signal transmission over long distances.

- **Level Shifter :** A level shifter is usually a circuit that shifts analog signals from one voltage level to another.

- **Low Pass Filter :** A low-pass filter is a circuit that passes signals with a frequency lower than a certain cut-off frequency and attenuates signals with frequencies higher than the cut-off frequency. The amount of attenuation for each frequency depends on the filter design.

- **Anti-aliasing Filter :** An anti-aliasing filter (AAF) is a filter used before a signal sampler to restrict the bandwidth of a signal to approximately or completely satisfy the sampling theorem over the band of interest. Since the theorem states that unambiguous reconstruction of the signal from its samples is possible when the power of frequencies above the Nyquist frequency is zero, a real anti-aliasing filter trades off between bandwidth and aliasing. A realizable anti-aliasing filter will typically either permit some aliasing to occur or else attenuate some in-band frequencies close to the Nyquist limit. For this reason, many practical systems sample higher than required to ensure that all frequencies of interest can be reconstructed, a practice called oversampling.

- **Analog -to-Digital Converter (ADC) :** An analog-to-digital converter (ADC, A/D, or A to D) is a device that converts a continuous physical quantity (usually voltage or current) to a digital number that represents the quantity's amplitude.

  The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Furthermore, instead of continuously performing the conversion, an ADC does the conversion periodically, sampling the input. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

4.1.1 Current Sensor (LTS25-NP)

The LTS25-NP is a $\pm 25\ A$ current sensor. The LEM^{TM} provides economical and precise solutions for AC or DC current sensing. The device package (shown in Figure 4.3) allows for easy implementation by the customer. Typical applications include AC variable speed drives and servo motor drives, static converters for DC motor drives, battery supplied applications, uninterruptible power supplies (UPS), switched mode power supplies (SMPS), power supplies for welding applications etc.

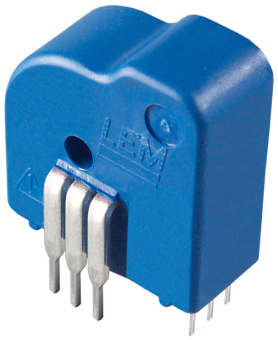

Figure 4.3: LTS25-NP current sensor.

The device consists of a precise, low-offset, linear Hall effect current transducer. Applied current flowing through this copper conduction path generates a magnetic field which the Hall transducer converts into a proportional voltage. The output of the device

has a positive slope when an increasing current flows through the primary copper conduction path. The internal resistance of this conductive path is $50\ \Omega$ typical, providing low power loss. The current corresponding voltage output of the ACS714ELCTR-20A-T varies between 0.5 V to 4.5 V as shown in Figure 4.4.

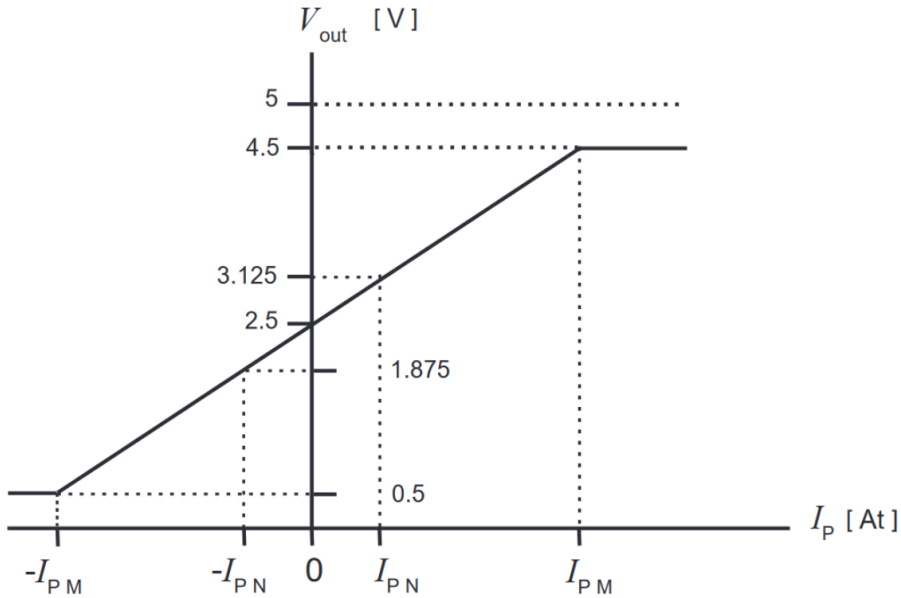

Figure 4.4: Output voltage versus primary sensed current plot

4.1.2 Attenuation and Level Shifter

As evident from Figure 4.4, the output voltage of the sensor varies from $4.5\ V$ to $0.5\ V$. Whereas, the LAUNCHPAD F28379 can sense voltage from $0\ V$ to $+3.3\ V$. Hence, the output of the LTS25-NP has to be attenuated to $0\ V$ to $3.3\ V$ range. This can be done with a simple voltage divider circuit.

The LTS25-NP requires minimum $2\ k\Omega$ resistance between V_{IOUT} and GND terminals. Hence, considering the lower resistor in the divider network as $4.7\ k\Omega$ as shown in Figure 4.5, the other resistance value can be estimated.

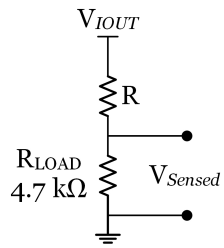

Figure 4.5: Voltage divider network for attenuating LTS25-NP output

$$R = \frac{V_{IOUT} \times R_{LOAD}}{V_{Sensed}} - R_{LOAD} \tag{4.1}$$

where,

V_{Sensed} = 3.3 V as the ADC can take up to 3.3 V as input.

V_{IOUT} = 4.0 V as the difference between the max and min of actual output voltage *i.e.*(= 4.5 - 0.5).

$R_{LOAD} = 4.7\ k\Omega$.

Substituting above values in equation Equation 4.1, we get -

$$R = \frac{4V \times 4.7k\Omega}{3.3V} - 4.7k\Omega \tag{4.2}$$

$$R = 996.96\Omega \approx 1.0k\Omega \tag{4.3}$$

With R = 1kΩ, the sensed output attenuates and varies between 0.4 V to 3.7 V as shown in Figure 4.6

The output of the voltage divider network, V_{Sensed} is more than the input voltage limitation of the ADC i.e. 3.3 V. Hence it is required to be shifted downward by 0.4 V. This will adjust the sensed voltage between 0V to 3.3 V. But this requires an additional unity gain voltage differential amplifier using OPAMP which subtracts the 0.4 V DC from the sensed signal and shifts it downward to fit into 0 V to 3.3 V band. Figure 4.7 shows the

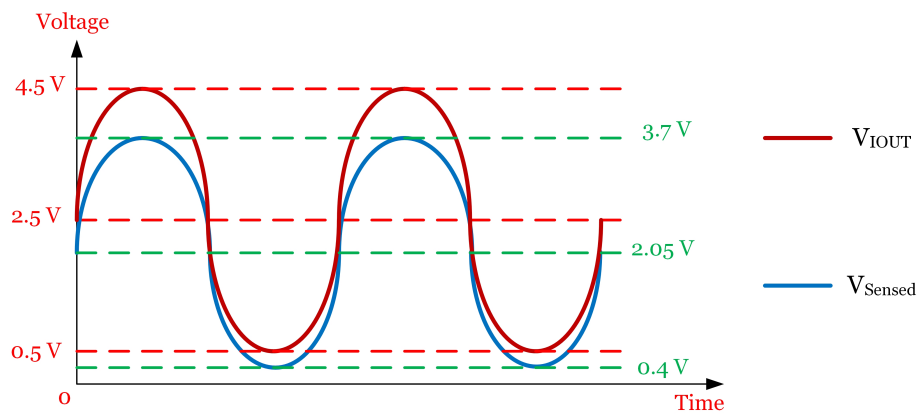

Figure 4.6: Voltage divider network for attenuating LTS25-NP output.

circuit diagram of a unity gain voltage differential amplifier suing OPAMP.

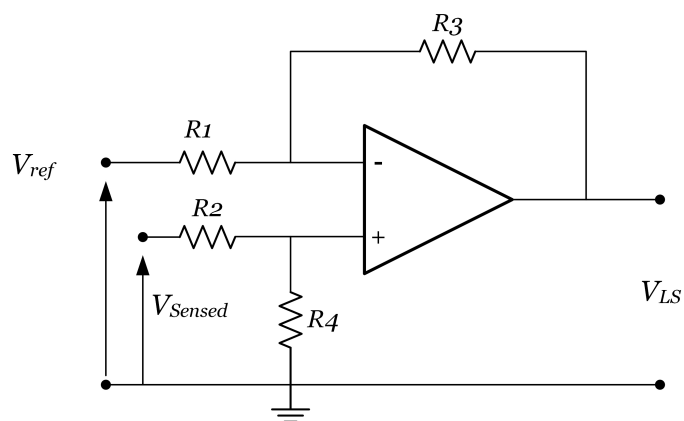

Figure 4.7: Active Voltage Level Shifter circuit

The output voltage expression of the above circuit is given as -

$$V_{LS} = V_{Sensed} \times \frac{R_4}{R_2 + R_4} \times \frac{R_1 + R_3}{R_1} - V_{ref} \times \frac{R_3}{R_1} \tag{4.4}$$

When resistors, $R_1 = R_2 and R_3 = R_4$ the above transfer function for the differential amplifier can be simplified to the following expression:

$$V_{LS} = \frac{R_3}{R_1}(V_{Sensed} - V_{ref}) \tag{4.5}$$

Where, V_{ref} = 0.4 V.Assuming the $R_1 = R_2 = R_3 = R_4 = 10\ k\Omega$, the circuit acts as a unity gain differential amplifier as shown in Figure

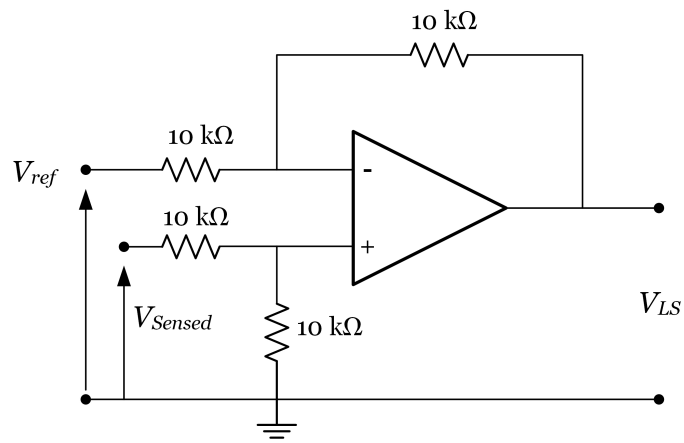

Figure 4.8: Active voltage level shifting circuit.

ALTERNET APPROACH :

With the sight adjustment in the resistance value of the voltage divider network, the "Voltage Level Shifting" stage can be completely eliminated but at the cost of resolution of the ADC which is comparatively negligible.

In the equation Equation 4.1 if the V_{IOT} is assumed to be 4.5 V, and substituted into equation Equation 4.2 we get -

$$R = \frac{4.5V \times 4.7k\Omega}{3.3V} - 4.7k\Omega \tag{4.6}$$

$$R = 2.35k\Omega \approx 2.4k\Omega \tag{4.7}$$

With R = 2.4 kΩ, the sensed output attenuates and varies between 0.33 V to 2.97 V as shown in Figure 4.9

The output of the voltage divider network is well within the input voltage levels of the ADC pin of the LAUNCHPAD. This also provides a $0.33\ V$ window on both positive

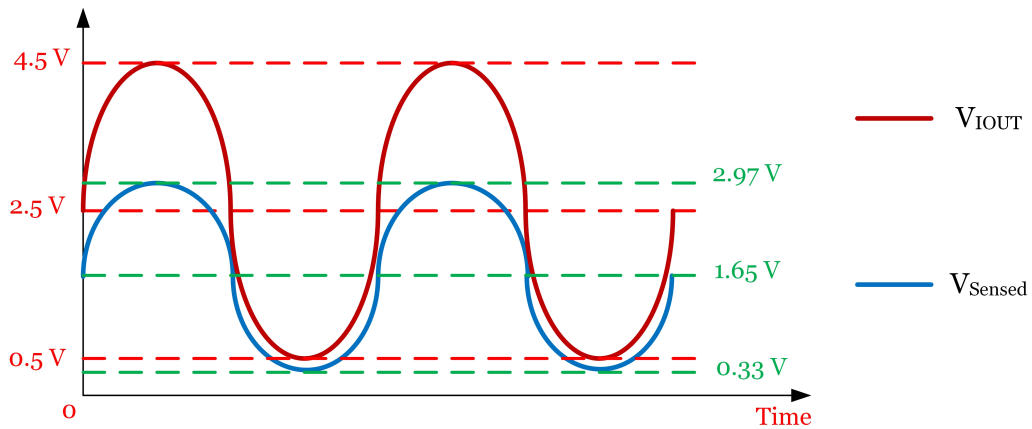

Figure 4.9: Voltage divider network for attenuating LTS25-NP output (For R = 2.4 kΩ).

and negative cycle to protect ADC pin of DSP from any unwanted current spike beyond ±25 A.

With such arrangement of voltage divider network, the active voltage level shifting stage can be eliminated which requires additional OPAMP, 0.4 V DC source and other components of the circuit shown in Figure 4.8.

4.1.3 Second Order Sallen-Key Butterworth Filter

Most designs of second order filters are generally named after their inventor with the most common filter types being: Butterworth, Chebyshev, Bessel and Sallen-Key. All these types of filter designs are available as either: low pass filter, high pass filter, band pass filter and band stop (notch) filter configurations, and being second order filters, all have a 40-dB-per-decade roll-off.

The Sallen-Key filter design is one of the most widely known and popular 2nd order filter designs, requiring only a single operational amplifier for the gain control and four passive RC components to accomplish the tuning.

Most active filters consist of only op-amps, resistors, and capacitors with the cut-off

point being achieved by the use of feedback eliminating the need for inductors as used in passive 1st-order filter circuits.

Second order (two-pole) active filters whether low pass or high pass, are important in Electronics because we can use them to design much higher order filters with very steep roll-off's and by cascading together first and second order filters, analogue filters with an nth order value, either odd or even can be constructed up to any value, within reason. Second order low pass filters are easy to design and are used extensively in many applications. The basic configuration for a Sallen-Key second order (two-pole) low pass filter is given as:

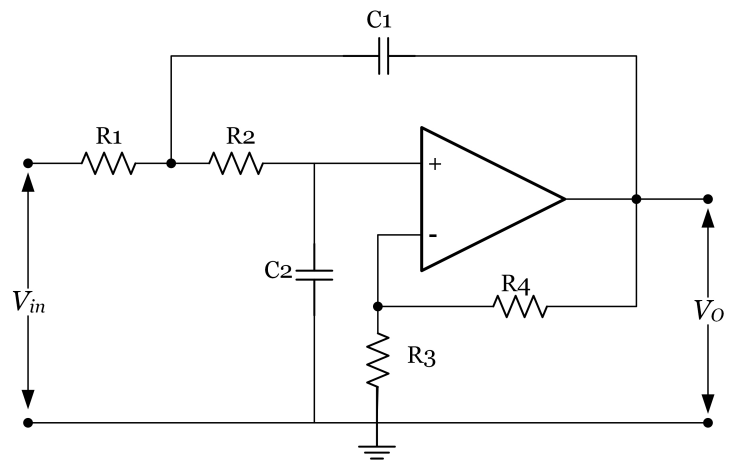

Figure 4.10: Low Pass Sallen-Key Architecture

This second order low pass filter circuit has two RC networks, R1 - C1 and R2 - C2 which give the filter its frequency response properties. The filter design is based around a non-inverting op-amp configuration so the filters gain,A will always be greater than 1. Also the op-amp has a high input impedance which means that it can be easily cascaded with other active filter circuits to give more complex filter designs.

The transfer function of the second order Sallen-Key Butterworth filter is -

$$H(f) = \frac{\dfrac{R_3 + R_4}{R_3}}{(j2\pi f)^2(R_1R_2C_1C_2) + (j2\pi f)\left[R_1C_1 + R_2C_1 + R_1C_2\left(-\dfrac{R_4}{R_3}\right)\right] + 1} \tag{4.8}$$

Also, the standard second order low pass filter transfer function is -

$$H_{LP}(f) = -\frac{K}{\left(\dfrac{f}{f_c}\right)^2 + \dfrac{1}{Q}\dfrac{jf}{f_c} + 1} \tag{4.9}$$

Comparing 4.8 with 4.9, we get -

$$K = \frac{R_3 + R_4}{R_3} \tag{4.10}$$

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \tag{4.11}$$

and

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + R_1C_2(1-K)} \tag{4.12}$$

Letting $R_1 = mR$, $R_2 = R$, $C_1 = C$, $C_2 = nC$ and $K = 1$, results in :

$$fc = \frac{1}{2\pi RC\sqrt{mn}} \tag{4.13}$$

and

$$Q = \frac{\sqrt{mn}}{m+1} \tag{4.14}$$

This sets the gain = 0dB in the pass band. Design should start by determining the ratios "m" and "n" for the required "Q" of the filter and then selecting "C" and calculating "R" to set "f_c".

For the Butterwoth filter the quality factor "Q" is 0.707. Hence by substituting Q = 0.707 and m = 1 in equation 4.14, we get n = 2.

Assuming capacitor "C" as 220 nF and substituting it in to equation 4.13 for the cut-off frequency of 4 kHz, the "R" can be estimated.

$$\therefore R = \frac{1}{2\pi C fc\sqrt{mn}} \tag{4.15}$$

$$\therefore R = \frac{1}{2\pi \times 220nF \times 4kHz \times \sqrt{1 \times 2}} \tag{4.16}$$

$$\therefore R = 127.88\Omega \approx 130\Omega \tag{4.17}$$

Therefore, $R1 = R2 = 130\Omega$, $C1 = 220nF$, $C2 = 440nF \approx 470nF$.

The second order Sallen-Key Butterworth filter with the estimated design values is shown in Figure 4.11

4.1.4 ADC Protection

For protecting ADC pin of micro-controller or DSP, two back-to-back connected zener diodes are placed across the output voltage terminal of the Analog Front End (AFE) as shown in the following Figure 4.12. The two zener diodes of 3.3 V rating, if connected back to back will short any signal above 3.3 volts and protect the DSP pin from any unwanted transient.

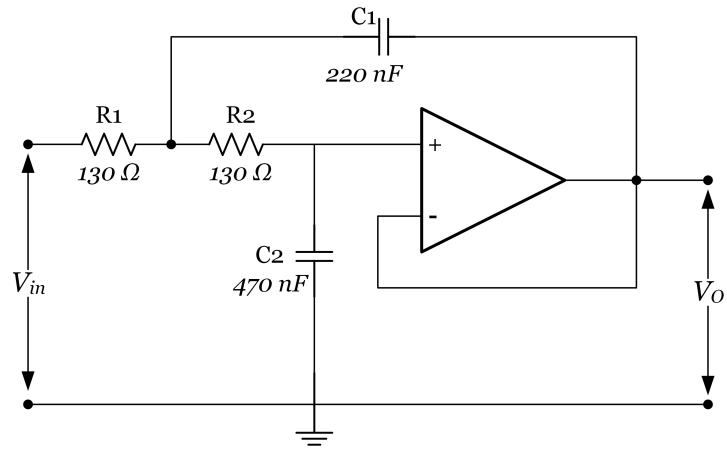

Figure 4.11: Low Pass Sallen-Key Design

4.1.5 ADC Resolution

The ±25 A input current to the sensor be converted by the 12-bit ADC at the resolution of -

$$\text{Resolution} = \frac{+25 - (-25)}{2^{12}} = \frac{50}{2^{12}} \tag{4.18}$$

$$\therefore \text{Resolution} = 0.01220 = 12.2mA \tag{4.19}$$

4.1.6 Current Sensor AFE

The Figure 4.12 shows the complete circuit diagram of the designed Analog Front End (AFE) without level shifter circuit for LV25-P current sensor.

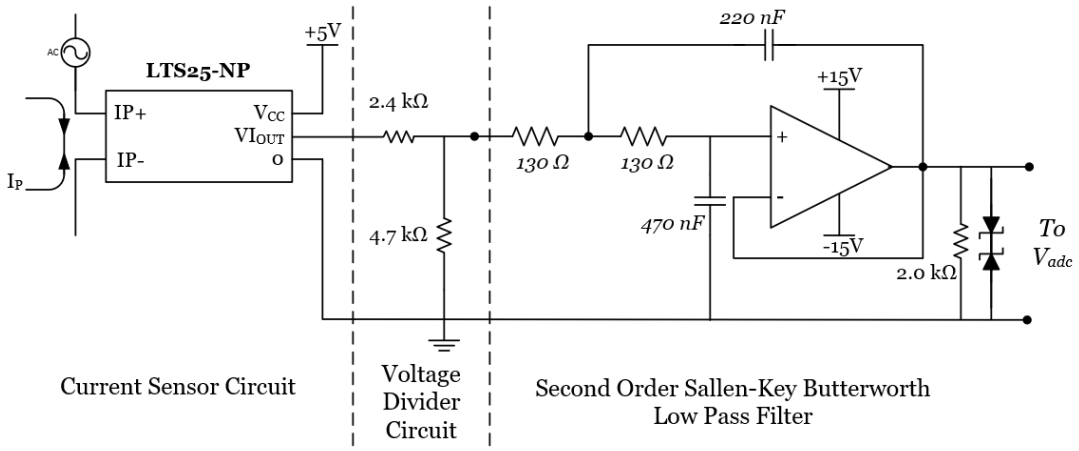

Figure 4.12: Analog Front End for LTS25-NP without voltage level shifting circuit.

4.1.7 Voltage Sensor AFE

Similarly the voltage sensor AFE circuit is designed and is as shown in the following Figure 4.13.

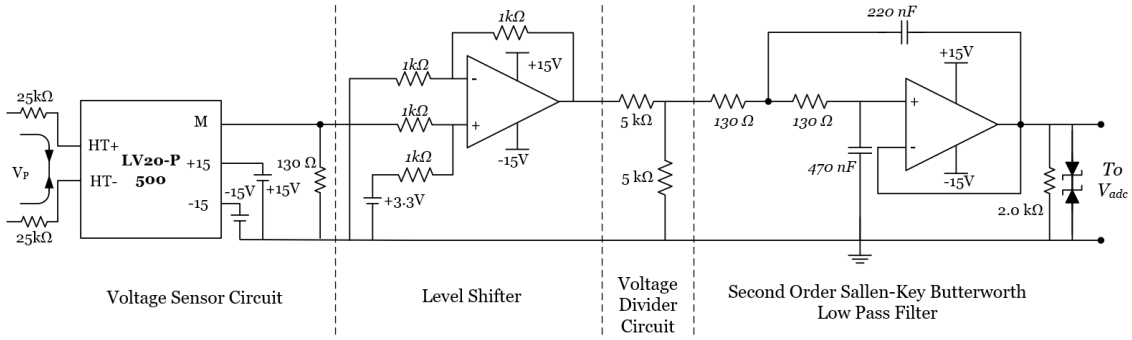

Figure 4.13: Analog Front End for LTS25-NP without voltage level shifting circuit.

4.2 Converter Power Loss and Efficiency Analysis

The switching loss analysis of the proposed converter topology is presented in this section. For the analysis, following operating conditions as listed in Table - 4.2 are considered.

TABLE – 4.2
PROPOSED CONVERTER OPERATING CONDITIONS

Parameter	Operating Condition
DC Bus Voltage	500 V
Line-to-line RMS Output Current ($I_{rms,ll}$)	14 A
Power Factor ($cos\ \beta$)	0.8
Modulation Index (m)	0.9
Switching Frequency (f_{sw})	25 kHz

Based on these operating conditions, the conduction loss and switching loss are calculated for the reverse blocking IGBT (FGW85N60RB). The power loss is calculated under only the assumed condition as an example.

4.2.1 Conduction Power Loss

The equivalent RMS current and average current through one IGBT with reverse blocking diode are calculated by (4.20) and (4.21) respectively,

$$I_{rms,igbt} = \frac{I_{rms,ll}}{2} \cdot \sqrt{1 + \frac{8 \cdot m \cdot cos\ \beta}{3 \cdot \pi}} \tag{4.20}$$

$$I_{avg,igbt} = \frac{I_{rms,ll}}{\sqrt{2 \cdot \pi}} \cdot \left(1 + \frac{\pi \cdot m \cdot cos\ \beta}{4}\right) \tag{4.21}$$

From the above two equations, the RMS and average IGBT current are calculated as, $I_{rms,igbt} = 8.89\ A$ and, $I_{avg,igbt} = 4.93\ A$. Also, from IGBT datasheet, it is found that, on-state resistance $(R_{on,igbt})$ is $0.0017\ \Omega$ and IGBT zero current voltage $(V_{0,igbt})$ is 0.7 V.

The conduction power loss of IGBT can be calculated by eq. (4.22)

$$P_{c,igbt} = I^2_{rms,igbt} \cdot R_{on,igbt} \ + \ V_{0,igbt} \cdot I_{avg,igbt} \tag{4.22}$$

Thus, the from calculated RMS as well as average current and eq. (4.22), the conduction power loss is estimated as,

$$P_{c,igbt} = 3.59\ W \tag{4.23}$$

4.2.2 Switching Power Loss

The graph of collector current (I_c) vs switching energy loss is refereed from IGBT datasheet, for estimating switching loss. The switching energy losses are proportional to the RMS current and DC-link voltage. Therefor, a coefficient should be multiplied to the values obtained in the figures if the RMS current or DC-link voltage is different from the one shown in the datasheet testing condition. The plot given in IGBT datasheet is for 400 V DC link. Thus, under 500V DC-link voltage and 150 degree junction temperature, the values of E_{on} and E_{off} are estimated by multiplying by 1.2 coefficient factor. The approximate values of E_{on} and E_{off} are $0.6\ mJ$ and $0.7\ mJ$ respectively.

For the switching frequency of $25\ kHz$, the IGBT switching power loss is calculated by,

$$P_{sw,igbt} = (E_{on} + E_{off}) \cdot f_{sw} \tag{4.24}$$

from, eq. (4.24), the switching loss in individual IGBT is calculated as, $P_{sw,igbt} = 26\,W$.

4.2.3 Total Power Loss

The total power loss in an IGBT is the sum of conduction power loss and switching power loss. From the previous subsections, the total power loss in an IGBT is estimated as,

$$P_{loss,igbt} = P_{c,igbt} + P_{sw,igbt} = 29.59\,W \tag{4.25}$$

Also, the total loss in proposed converter is the product of number of IGBT switches and total power loss in an IGBT for the given operating conditions. As described in Section - IV, two RB-IGBT's are used in series at each switch place in the proposed converter to make up for the desired collector-emitter voltage rating of $1200\ V$. Therefore the total number of IGBT's used in proposed system are twenty.

Hence, the total power loss in all the IGBT's used in proposed converter is, $591.8\,W$.

4.2.4 Converter Efficiency

The efficiency of any power converter is the ratio of output power to input power. The proposed system is designed for $10\ kW$. However, the motor parameters considered for emulation are for a $7.5\ kW$ PMSM motor. Therefore the input power to the converter is $7.5\ kW$.

The output power of power proposed converter is,

$$P_{out} = P_{in} - P_{loss,igbt} = 6908.4\,W \tag{4.26}$$

Here, the power loss across LCL filter and othet passive elements is not considered for efficiency calculation.

Therefore, the efficiency of the proposed converter is,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{6708.4}{7500} = 0.9211 = 92.11\% \tag{4.27}$$

4.3 Summary

In this chapter detailed hardware development stages involved in the process of development of the proposed bidirectional converter topology for common DC-bus-configured ME system are described. The conduction and switching power loss analysis along with converter efficiency is evaluated in the previous section. From the analysis it is evident that the proposed converter topology is 92.11% efficient.

Chapter 5

Common DC-Bus-Configured AC Traction Motor Emulator

INTEGRATION of power electronics together with software simulation is being used for developing a hardware-in-loop (HIL) system for emulating an electric motor [25]. In traditional ME system, real rotating machine is replaced with AC-DC-AC multistage power electronic converter [3], [26], [79]. Whereas, in the proposed Common DC-Bus-Configured ME system, the AC-DC-AC conevrter is replaced with a single-stage AC-DC buck-boost converter fed by a common DC source. The mathematical motor model estimates the phase, frequency and magnitude of current for a specific motor for the applied voltage input at motor terminals by drive [2]. Further, based on control strategy implemented, the emulating converter is controlled in such a way that, current drawn from 'Device Under Test' *or* 'Drive Under Test' (DUT) mimics the estimated reference current by motor model. The advantage of such ME system is, flexible load configuration. By changing parameters in motor model and control loop, ME starts emulating an all new motor [3], [26], [33]–[35], eliminating need for replacing real physical motor as well as restructuring of the test-bench setup.

As described earlier, the LCL filters are most commonly used in back-to-back converter systems.However, due to relatively low damping the output side inductor current possess high resonance which impacts the stability of the system with LCL filter and needs to be taken into account while designing the controller. To overcome this issue an active damping control approach is widely used in the control system as presented by [80]. In addition, there are several different approach are proposed and presented in various literature. State feedback linearization method is one of those which has proved effective in non-linear power electronics systems [81]–[83].

This chapter presents a single loop control scheme for the proposed common DC-bus-configured ME system emulating PMSM motor. The proposed control method is simulated on MATLAB/Simulink simulation platform as well as experimentally validated to verify the system stability, and the results are presented here. The mathematical state space model of emulator bidirectional AC-DC power converter and the proposed control strategy for the ME test rig setup are briefly explained. The detailed structure of common-DC-bus motor emulator system is followed by the simulation and experimental results.

The DUT used for simulation is a standard two-level AC-DC converter, controlled using vector control method with switching frequency of $10\ kHz$. A detailed review of PMSM motor drive systems is presented in [84]. A ME system is expected to be independent of DUT converter topology and its control algorithm has to exclusively emulate electric motor characteristics. In addition, the DUT drive topology and its control can vary from customer-to-customer as per system requirements. Therefore, detailed explanation of DUT control drive is out of the scope of this research. The detailed mathematical model of PMSM motor is documented in [85], and used here for simulation verification. The control strategy implemented for the proposed ME system is a single-loop current control based on state feedback linearization. To understand the different stages of control strategy, this chapter is divided into following sections.

5.1 PMSM Motor Mathematical Model

A twin-axis PMSM stator with winding and rotor with PMs is shown in Figure 5.1. The stator winding are spatially displaced by 90^0. The d and q-axes stator voltages are derived as the sum of the resistive voltage drops and the derivative of the flux linkages in the respective winding as [86] -

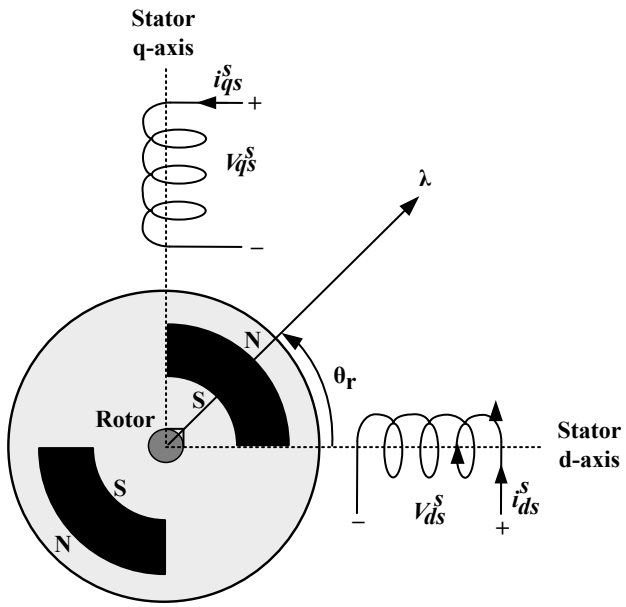

Figure 5.1: Twin-axis *dq* representation of PMSM.

$$\begin{bmatrix} v_{ds}^s \\ v_{qs}^s \end{bmatrix} = \begin{bmatrix} R_d & 0 \\ 0 & R_q \end{bmatrix} \cdot \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} + \rho \begin{bmatrix} \lambda_{ds} \\ \lambda_{qs} \end{bmatrix} \tag{5.1}$$

where, ρ represents differentiation operator, $\frac{\delta}{\delta t}$; v_{ds}^s and v_{qs}^s are the voltages in the d-axis and q-axis windings respectively; i_{ds}^s and i_{qs}^s are the currents through the d-axis and q-axis windings; R_d and R_q are the resistances of the d-axis and q-axis windings and λ_{ds} and λ_{qs} are the flux linkages in the d-axis and q-axis windings. The flux linkage can further be expanded as -

$$\begin{bmatrix} \lambda_{ds} \\ \lambda_{qs} \end{bmatrix} = \begin{bmatrix} L_{dd} & L_{qd} \\ L_{dq} & L_{qq} \end{bmatrix} \cdot \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} + \lambda_m \begin{bmatrix} \cos\theta_r \\ \sin\theta_r \end{bmatrix} \tag{5.2}$$

The, L_{dd} and L_{qq} are the self-inductances of the d-axis and q-axis respectively. L_{qd}, L_{dq} are the mutual inductances between d-axis and q-axis and are equal. Instantaneous rotor position with respect to stator d-axis is denoted by, θ_r. The resistances R_d and R_q can be replaced with R_s, as the PMSM windings are balanced and therefore the resistances are equal. Further, by substituting (5.2) into (5.1), the stator d-axis and q-axis voltage can be written in matrix form as -

$$\begin{bmatrix} v_{ds}^s \\ v_{qs}^s \end{bmatrix} = \begin{bmatrix} R_s + \rho L_{dd} & \rho L_{dq} \\ \rho L_{qd} & R_s + \rho L_{qq} \end{bmatrix} \times \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} \begin{bmatrix} + & \lambda_m \rho \end{bmatrix} \begin{bmatrix} \cos\theta_r \\ \sin\theta_r \end{bmatrix} \tag{5.3}$$

where,

$$L_{dd} = \frac{1}{2}[(L_q + L_d) - (L_q - L_d)\cos\theta_r]$$

$$L_{qq} = \frac{1}{2}[(L_q + L_d) + (L_q - L_d)\cos\theta_r]$$

$$L_{qd} = \frac{1}{2}[(L_d - L_q)\sin\theta_r]$$

The above analysis is done in the stationary reference frame for the stator windings. The stationary reference frame analysis is further transformed into synchronously rotating reference frame analysis using (5.4).

$$f_{dq}^r = K \cdot f_{dq}^s \tag{5.4}$$

where, 'f' can be voltage, current or flux and superscript 'r' denotes rotating reference frame. K is the transformation matrix and is as follows -

$$K = \begin{bmatrix} \cos\theta_r & -\sin\theta_r \\ \sin\theta_r & \cos\theta_r \end{bmatrix}$$

Equation (5.4) can further be rearranged as (5.5) to replace the stationary reference frame voltage and current variables.

$$f^s_{dqs} = \begin{bmatrix} \cos\theta_r & \sin\theta_r \\ -\sin\theta_r & \cos\theta_r \end{bmatrix} \cdot f^r_{dqs} \tag{5.5}$$

Transforming voltage and current from stationary reference frame variables to synchronously rotating reference frame using (5.5) and substituting it in (5.3), we obtain (5.6) as the PMSM model after simplification.

$$\begin{bmatrix} v^r_{ds} \\ v^r_{qs} \end{bmatrix} = \begin{bmatrix} R_s + L_d\rho & -\omega_r L_q \\ \omega_r L_d & R_s + L_q\rho \end{bmatrix} \times \begin{bmatrix} i^r_{ds} \\ i^r_{qs} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_r \lambda_m \end{bmatrix} \tag{5.6}$$

where, $\omega_r = \dfrac{\delta\theta_r}{\delta t} = \rho\theta_r$, rotor reference speed in rad/s.

Another important quantity which determines the dynamics of the machine is electromagnetic torque. This torque is derived from the input power. The instantaneous power can be written in the form of two phase quantities as,

$$P_i = \left(\frac{3}{2}\right)\left(v^r_{qs} i^r_{qs} + v^r_{ds} i^r_{ds}\right) \tag{5.7}$$

Neglecting the zero sequence terms and replacing voltages with associated speed voltages in (5.7), the instantaneous power can be rewritten as,

$$P_i = \left(\frac{3}{2}\right)(\omega_r \lambda_{ds} i_{qs}^r - \omega_r \lambda_{qs} i_{ds}^r) \tag{5.8}$$

The electromagnetic torque is proportional to the ratio of instantaneous power to rotor speed, i.e.

$$T_e = \frac{P_i}{\omega_m} \tag{5.9}$$

Substituting (5.8) in (5.9) and replacing, $\omega_r = \frac{P}{2}\omega_m$ the electromagnetic torque is determined as,

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\{\lambda_m i_{qs}^r + (L_d - L_q) i_{qs}^r i_{ds}^r\} \tag{5.10}$$

where, P is the number of poles and λ_{qs} as well as λ_{ds} are replaced by, $\lambda_{qs} = L_q i_{qs}^r$ and $\lambda_{ds} = \lambda_m + L_d i_{ds}^r$.

To implement the PMSM mathematical model in MATLAB/Simulink, (5.6) is rearranged as follows,

$$\frac{\delta}{\delta t} i_{ds}^r = \frac{1}{L_d} v_{ds}^r - \frac{R_s}{L_d} i_{ds}^r + \frac{L_q}{L_d} \omega_r i_{qs}^r \tag{5.11}$$

$$\frac{\delta}{\delta t} i_{qs}^r = \frac{1}{L_q} v_{qs}^r - \frac{\lambda_m}{L_q} \omega_r - \frac{R_s}{L_q} i_{qs}^r - \frac{L_d}{L_q} \omega_r i_{ds}^r \tag{5.12}$$

5.2 Proposed Single Loop Control

The control stratagy implemented for the proposed ME system is a single-loop current control based on state feedback linearization. The block diagram of proposed converter's mathematical model in dq coordinate system is shown in Figure 5.2 and 5.3. The

corresponding voltage and current quantities in dq coordinates at each of the node of proposed topology are represented by their respective suffix letter d or q.

As stated before, the proposed topology is of a bidirectional converter. Therefore, The current through energy storage inductor L, is represented by i_l. To efficiently and accurately emulate the behaviour of AC machine, the phase, frequency and magnitude of the AC current must be taken into account. The inductor current i_l, being DC quantity, does not account for phase, frequency and magnitude. Whereas, the detailed information about the phase, frequency and magnitude of the AC current is carried by i_q and i_d currents. Therefore, for implementing control strategy, DC bus voltage v_{dc} is considered as input and i_q and i_d currents are considered as outputs.

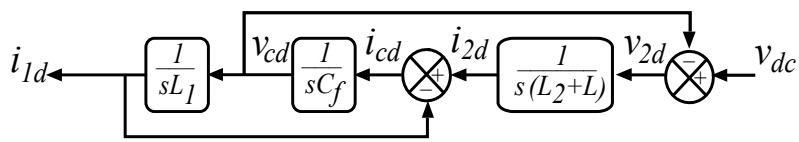

Figure 5.2: Mathematical model of emulator power converter in *d -axis* coordinate system.

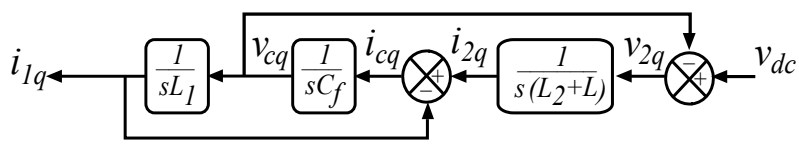

Figure 5.3: Mathematical model of emulator power converter in *q-axis* coordinate system.

In a converter topology with LCL filter, inductor current and capacitor voltage are coupled in the synchronous reference coordinate system. Conventionally, the three-phase converter system with LCL filter is controlled in a double control loop strategy. However, the LCL filter increases the order of the system. Therefore, it is necessary to damp the LC resonance by decoupling dq current components. The single loop decoupling of LCL filter system in dq coordinates is presented in [87].

$$\begin{bmatrix} \hat{i}_{1d} \\ \hat{i}_{1q} \\ \hat{v}_{cd} \\ \hat{v}_{cq} \\ \hat{i}_{2d} \\ \hat{i}_{2q} \\ \hat{v}_{dc} \end{bmatrix} = \begin{bmatrix} 0 & \omega & \frac{-1}{L_1} & 0 & 0 & 0 & \frac{m_d}{L_1} \\ -\omega & 0 & 0 & \frac{-1}{L_1} & 0 & 0 & \frac{m_q}{L_1} \\ \frac{1}{C_f} & 0 & 0 & \omega & \frac{-1}{C_f} & 0 & 0 \\ 0 & \frac{1}{C_f} & -\omega & 0 & 0 & \frac{-1}{C_f} & 0 \\ 0 & 0 & \frac{1}{L_2+L} & 0 & 0 & \omega & 0 \\ 0 & 0 & 0 & \frac{1}{L_2+L} & -\omega & 0 & 0 \\ -\frac{m_d}{C_{dc}} & -\frac{m_q}{C_{dc}} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{1d} \\ i_{1q} \\ v_{cd} \\ v_{cq} \\ i_{2d} \\ i_{2q} \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_1} & 0 \\ 0 & \frac{-1}{L_1} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} e_d \\ q_q \end{bmatrix} \tag{5.13}$$

The state space model of the ME converter presented in [59] and as shown in Fig. Figure 5.5 is as follows -

where the state variables $X = [i_{1d}\ i_{1q}\ v_{cd}\ v_{cq}\ i_{2d}\ i_{2q}\ v_{dc}]^T$ represents the DUT side inductance current, the filter capacitor voltage , the emulator side inductance and the DC link capacitor . The DUT voltage in $d-q$ reference frame are represented as e_d and e_q. The modulation vector input variable are defined as,

$$U = \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} m_d \\ m_q \end{bmatrix}$$

The DUT side inductance current is taken as the output variable $Y = R(X) = [r_1(X)\ r_2(X)]^T = \left[(i_{1d}^* - i_{1d})\ (i_{1q}^* - i_{1q})\right]^T$, where i_{1d}^* and i_{1q}^* are the reference currents.

The (5.13) can therefore be written as a nonlinear differential equation comprising of state variables and input variables –

$$\begin{aligned} \hat{X} &= f[X(t)] + G[X(t)]U \\ Y &= R(X) \end{aligned} \tag{5.14}$$

where,

$$f(X) = \begin{bmatrix} \omega i_{1q} - v_{cd}/(L_1) \\ -\omega i_{1d} - v_{cq}/(L_1) \\ i_{1d}/C_f + \omega v_{cq} - i_{2d}/C_f \\ i_{1q}/C_f - \omega v_{cd} - i_{2q}/C_f \\ v_{cd}/(L_2 + L) + \omega i_{2q} - e_d/(L_2 + L) \\ v_{cq}/(L_2 + L) - \omega i_{2d} - e_q/(L_2 + L) \end{bmatrix} \tag{5.15}$$

and

$$G(X) = \begin{bmatrix} g_1(X) \\ g_2(X) \end{bmatrix} = \begin{bmatrix} 0 & \frac{v_{dc}}{(L_1)} \\ \frac{v_{dc}}{(L_1)} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{5.16}$$

It is evident from (5.15), that state variables are symmetric vector field pairs ($l = 3$) in dq coordinates. Therefore the $l - 1$ order Lie derivative for (5.15) and (5.16) is as follows –

$$
\begin{aligned}
L\delta g_1(X) &= L_f g_1 - L_{g1} f \\
L\delta^2 g_1(X) &= L_f[L\delta g_1(X)] - L\delta g_1(X) f \\
L\delta g_2(X) &= L_f g_2 - L_{g2} f \\
L\delta^2 g_2(X) &= L_f[L\delta g_2(X)] - L\delta g_2(X) f
\end{aligned}
\tag{5.17}
$$

Solving (5.17) for Lie bracket operation results in six-dimensional vector matrix as follows–

$$
M_6 = \left[g_1 \; g_2 \; L\delta g_1 \; L\delta g_2 \; L\delta^2 g_1 \; L\delta^2 g_2\right] \tag{5.18}
$$

It is to be noted here that, the elements in (5.18) does not contain any state variables i.e. it is a constant vector field.

The output state variable of the ME converter is current error $r_1(X) = i_{1d}^* - i_{1d}$. Therefore to analyze the output, its Lie derivative need to be obtained -

$$
\begin{aligned}
L_{g1} r_1(X) &= 0 \\
L_{g2} r_1(X) &= 0 \\
L_f r_1(X) &= \frac{-v_{cd}}{L_1} - \omega i_{2q} + \frac{e_d}{L_1} \\
L_{g1} L_f r_1(X) &= 0 \\
L_{g2} L_f r_1(X) &= 0 \\
L_f^2 r_1(X) &= \frac{i_{2d} - i_{1d}}{L_1 C_f} - \frac{2\omega v_{cq}}{L_1} + \omega^2 i_{2d} + \frac{\omega e_d}{L_1} \\
L_{g1} L_f^2 r_1(X) &= \frac{-v_{dc}}{L_1(L_2 + L)C_f} \neq 0 \\
L_{g2} L_f^2 r_1(X) &= 0
\end{aligned}
\tag{5.19}
$$

Similarly for $r_2(X) = i_{1q}^* - i_{1q}$ -

$$
\begin{aligned}
L_{g1} r_2(X) &= 0 \\
L_{g2} r_2(X) &= 0 \\
L_f r_2(X) &= \frac{-v_{cq}}{L_1} - \omega i_{2d} + \frac{e_q}{L_1} \\
L_{g1} L_f r_2(X) &= 0 \\
L_{g2} L_f r_2(X) &= 0 \\
L_f^2 r_2(X) &= \frac{i_{2q} - i_{1q}}{L_1 C_f} + \frac{2\omega v_{cd}}{L_1} + \omega^2 i_{2q} - \frac{\omega e_q}{L_1} \\
L_{g1} L_f^2 r_2(X) &= 0 \\
L_{g2} L_f^2 r_2(X) &= \frac{-v_{dc}}{(L_2 + L) L_1 C_f} \neq 0
\end{aligned}
\tag{5.20}
$$

From (5.19) and (5.20), the decoupling matrix can be derived as -

$$
\begin{aligned}
D(X) &= \begin{bmatrix} L_{g1} L_f^2 r_1(X) & L_{g2} L_f^2 r_1(X) \\ L_{g1} L_f^2 r_2(X) & L_{g2} L_f^2 r_2(X) \end{bmatrix} \\
&= \begin{bmatrix} \dfrac{-v_{dc}}{L_1 (L_2 + L) C_f} & 0 \\ 0 & \dfrac{-v_{dc}}{L_1 (L_2 + L) C_f} \end{bmatrix}
\end{aligned}
\tag{5.21}
$$

It is evident that the matrix is a non-singular matrix. The total relation degree of the system output variables is $d = d_1 + d_2 = 6 = n$. Therefore, the original system can be directly transformed into a controllable linear system.

Let's define the state variable for the system with feedback linearization Z as – $Z = [z_1\ z_2\ z_3\ z_4\ z_5\ z_6]^T$.

The relationship between the new and original state variables can be derived as

$$
\begin{aligned}
z_1 &= r_1(X) = i_{1d}^* - i_{1d} \\
z_2 &= L_f r_1(X) = \frac{-v_{cd}}{L_1} - \omega i_{2q} + \frac{e_d}{L_1} \\
z_3 &= L_f^2 r_1(X) = \frac{i_{2d} - i_{1d}}{L_1 C_f} - \frac{2\omega v_{cq}}{L_1} + \omega^2 i_{2d} + \frac{\omega e_q}{L_1} \\
z_4 &= r_2(X) = i_{2q}^* - i_{2q} \\
z_5 &= L_f r_2(X) = \frac{-v_{cq}}{L_1} - \omega i_{2d} + \frac{e_q}{L_1} \\
z_6 &= L_f^2 r_2(X) = \frac{i_{2q} - i_{1q}}{L_1 C_f} - \frac{2\omega v_{cd}}{L_1} + \omega^2 i_{2q} + \frac{\omega e_d}{L_1}
\end{aligned}
\tag{5.22}
$$

The original output state variable X is now mapped in to new state variable Z with Lie derivative transformation. The Lie derivative of new state variable Z is as follows –

$$
\begin{aligned}
\hat{z_1} &= \frac{-v_{cd}}{L_1} - \omega i_{2q} + \frac{e_d}{L_1} = z_2 \\
\hat{z_2} &= \frac{i_{2d} - i_{1d}}{L_1 C_f} - \frac{2\omega v_{cq}}{L_1} + \omega^2 i_{2d} + \frac{\omega e_q}{L_1} = z_3 \\
\hat{z_3} &= \frac{-3\omega i_{1q}}{L_1 C_f} + \left(\frac{L_1 + L_2 + L}{(L_1 + L) L_1^2 C_f} + \frac{3\omega^2}{L_1} \right) v_{cd} \\
&\quad + \left(\frac{3\omega}{L_1 C_f} + \omega^3 \right) i_{2q} - \left(\frac{1}{L_1^2 C_f} + \frac{\omega^2}{L_1} \right) e_d - \frac{v_{dc}}{(L_2 + L) L_1 C_f} u_1 \\
\hat{z_4} &= \frac{-v_{cq}}{L_1} - \omega i_{2d} + \frac{e_q}{L_1} = z_5 \\
\hat{z_5} &= \frac{i_{2q} - i_{1q}}{L_1 C_f} - \frac{2\omega v_{cd}}{L_1} + \omega^2 i_{2q} + \frac{\omega e_d}{L_1} = z_6 \\
\hat{z_6} &= \frac{-3\omega i_{1d}}{L_1 C_f} + \left(\frac{L_1 + L_2 + L}{(L_2 + L) L_1^2 C_f} + \frac{3\omega^2}{L_1} \right) v_{cq} \\
&\quad + \left(\frac{3\omega}{L_1 C_f} + \omega^3 \right) i_{2d} - \left(\frac{1}{L_1^2 C_f} + \frac{\omega^2}{L_1} \right) e_q - \frac{v_{dc}}{(L_2 + L) L_1 C_f} u_2
\end{aligned}
\tag{5.23}
$$

From (5.23), it is evident that z_3 and z_6 does not contain direct information of z_1 and z_4. Defining the new control variable for coordinate transformation as $V = [v_1 \;\; v_2]^T$, the

relationship between the system control variable U and V of can be derived as -

$$U = D^{-1}(X)\left[V - R(X)\right] \tag{5.24}$$

where,

$$R(X) = \begin{bmatrix} \hat{L}_f^2 r_1(X) \\ \hat{L}_f^2 r_2(X) \end{bmatrix} \tag{5.25}$$

Substituting, (5.24) in (5.14), the decoupled controller equations can be derived as –

$$\begin{aligned} u_1 &= \frac{1}{v_{dc}}\left[-3(L_1)\omega i_{1q}\right] \\ &+ \frac{1}{v_{dc}}\left[\left(3L_1C_f\omega^2 + \frac{L_1+L_2+L}{L1}\right)v_{cd}\right] \\ &+ \frac{1}{v_{dc}}\left[\left(3L_1\omega + (L_2+L)L_1C_f\omega^3\right)i_{2q}\right] \\ &- \frac{1}{v_{dc}}\left[\left(L_1C_f\omega^2 + \frac{L_1}{L_2+L}\right)e_d\right] \\ &- \frac{1}{v_{dc}}\left[(L_2+L)L_1C_fv_1\right] \end{aligned} \tag{5.26}$$

$$\begin{aligned} u_2 &= \frac{1}{v_{dc}}\left[-3L_1\omega i_{1d}\right] \\ &+ \frac{1}{v_{dc}}\left[\left(3L_1C_f\omega^2 + \frac{L_1+L_2+L}{L1}\right)v_{cq}\right] \\ &- \frac{1}{v_{dc}}\left[\left(3L_1\omega + (L_2+L)L_1C_f\omega^3\right)i_{2d}\right] \\ &- \frac{1}{v_{dc}}\left[\left(L_1f\omega^2 + \frac{L_1}{L_2+L}\right)e_q\right] \\ &- \frac{1}{v_{dc}}\left[(L_2+L)L_1C_fv_2\right] \end{aligned} \tag{5.27}$$

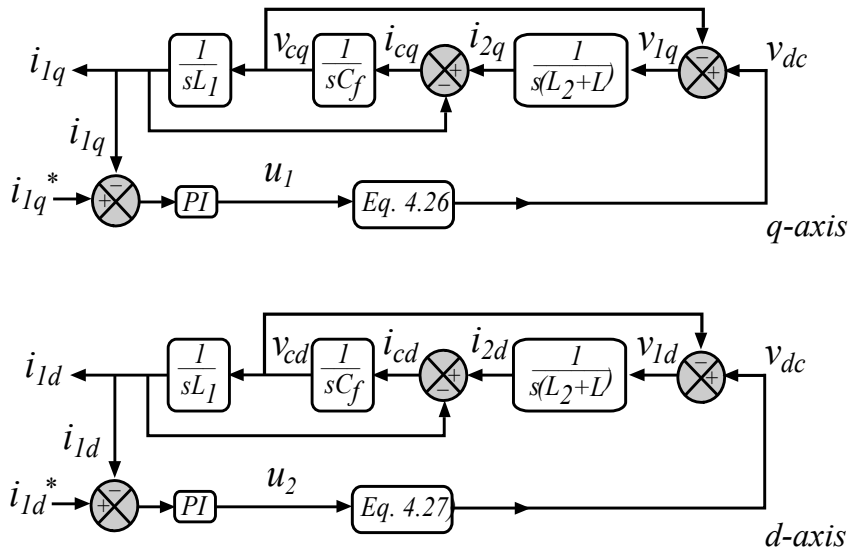

Figure 5.4: Single-loop decoupled current control strategy in dq coordinates.

The single loop, decoupled current control strategy for the proposed converter is shown in Figure 5.4. As shown in Fig. Figure 5.5 and 5.4, the measured i_{1d} and i_{1q} currents are compared with their corresponding reference values i.e. i_{1d}^* and i_{1q}^*. The errors of two are then controlled using individual PI controllers which produces v_1 and v_2 as output signals respectively. The two-phase direct and quadrature axis voltage quantities, v_1 and v_2, are then transformed to *abc* quantities to generate sinusoidal template, v_{abc} for carrier based SVPWM generation. The voltage template v_{abc}, is proportional to the amount of voltage required to be applied across inductor L, to allow the matching current to be drawn from DUT with that of reference current. The PI controller design and tuning is performed in MATLAB to estimate the k_p and k_i gain vlaues.

5.3 Detailed Hardware and Control Structure

A detailed structure of proposed ME system with common DC bus is presented in Fig. 5.5. The detailed structure of proposed ME system consist of a DC bus, a device under

test (DUT) along with its control, three-phase voltage and current sensors, proposed ME converter and controller board along with gate driver circuits.

The DUT used for experimentation is a standard two-level AC-DC converter, controlled using vector control method with switching frequency of $20\ kHz$. However, ME system is expected to be independent of DUT converter topology and its control algorithm has to exclusively emulate electric motor characteristics. In addition, the DUT drive topology and its control can vary from customer-to-customer as per system requirements. Therefore, detailed explanation of DUT control drive is out of the scope of this research.

As shown in Figure 5.4 and 5.5, the measured i_d and i_q currents are compared with their corresponding reference values i.e. i_d^* and i_q^*. The errors of two are then controlled using individual PI controllers which produces v_{qs}^* and v_{ds}^* as output signals respectively.

$$v_{qs}^* = \left(K_p + \frac{K_i}{s}\right) \cdot (i_{qs}^* - i_{qs}) \tag{5.28}$$

and,

$$v_{ds}^* = \left(K_p + \frac{K_i}{s}\right) \cdot (i_{ds}^* - i_{ds}) \tag{5.29}$$

The two-phase direct and quadrature axis voltage quantities, v_{qs}^* and v_{ds}^*, are then transformed to *a-b-c* quantities to generate sinusoidal template, v_{abc} for carrier based SVPWM generation. The voltage template v_{abc}, is proportional to the amount of voltage required to be applied across inductor L, to allow the matching current to be drawn from DUT with that of reference current.

The operation of the proposed ME system is divided into four quadrants. The reference torque and speed signals are used to decide the quadrant of operation according to Table - 3.3. As per quadrant of operation, comparator operator is selected to compare v_{abc} with v_{tri} for SVPWM generation. The generated PWM pulses are further used, to drive

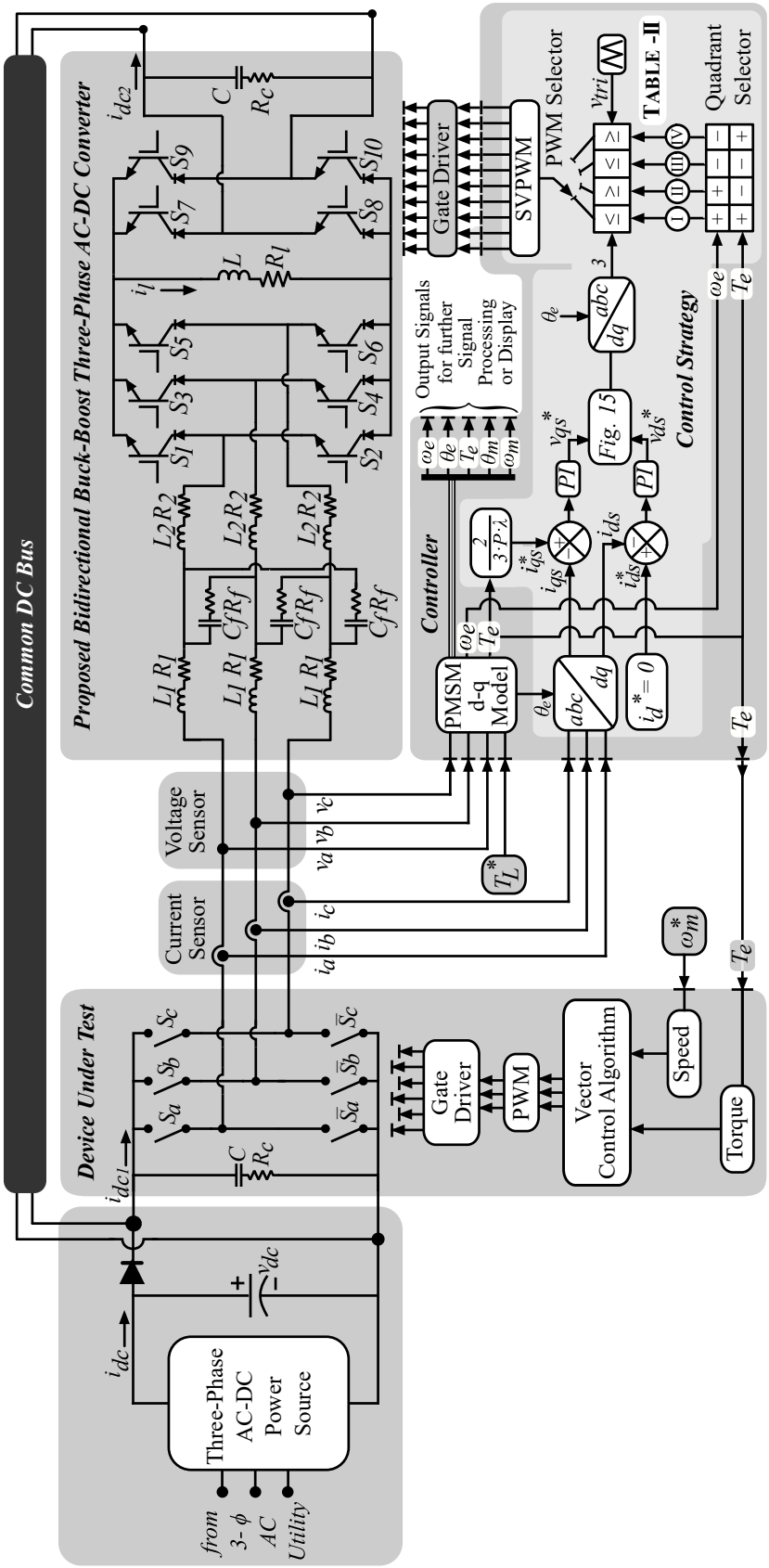

Figure 5.5: Detailed structure of proposed ME system.
($\omega_m{}^*$: mechanical speed reference; ω_e: electric speed; T_e: electromagnetic torque; T_L^*: load torque reference; θ_e: electric angle; P: number of pole pairs; λ: flux linkage; v_{tri}: triangular-wave carrier signal; v_{abc}: three-phase modulating signal.)

proposed ME converter.

It is to be noted that, carrier based SVPWM technique calculates switching (ON and OFF) time duration for AC side converter switches. However, DC side converter switches are activated during zero switching state and according to quadrant of operation as summarized in Table - 3.3.

5.4 PMSM Motor – 1 Results Analysis

The ME system presented in Figure 5.5 is simulated on MATLAB for the validation of proposed virtually isolated converter topology, for the PMSM motor parameters listed in TABLE – 5.1. The state-space model of PMSM motor presented in [85] is used for simulation of proposed system to verify the control scheme as well as the converter topology. The hardware for proposed converter topology is developed and tested for the motor parameters listed in TABLE – 3.2 and TABLE – 5.1 and test conditions listed in TABLE – 5.2 respectively.

TABLE – 5.1
PMSM MOTOR – 1 PARAMETERS

Motor Parameter	Nomenclature	Value
Rated Power	P_m	7.5 kW
Rated Speed	ω_r	1800 rpm
Rated Torque	T_r	14 $N \cdot m$
Rated Current	I_r	14 A
Number of Poles	P	6
Stator Resistance	R_s	0.348 Ω
Stator d-axis Inductance	L_d	3 mH
Stator q-axis Inductance	L_q	14.9 mH
Magnetic Flux	λ	0.22 Vs/rad
Inertia	J	0.01 kgm^2

TABLE – 5.2
TORQUE AND SPEED INPUT REFERENCE COMMANDS FOR PMSM MOTOR – 1

Operating Mode	Quadrant	Load Torque (T_L^*)	Load Torque Step-Time	Rotor Speed (ω_m^*)	Rotor Speed Step-Time
Forward Motoring	I	10 Nm	0.0 s	500 RPM	0.0 s
Forward Braking	II	-10 Nm	3.0 s	900 RPM	4.0 s
Reverse Motoring	III	-10 Nm	7.0 s	-500 RPM	8.0 s
Reverse Braking	IV	10 Nm	18.0 s	-900 RPM	15.0 s

The proposed common DC-bus-configured ME system is simulated on MATLAB for the mathematical model of PMSM motor listed in TABLE – 5.1 along with proposed converter topology. The simulation results are presented in Figure 5.6. The simulation model is executed for 20 s for the torque and speed test commands listed in TABLE – 5.2 to estimate dynamic current, speed and torque signals for the PMSM motor under test. The test commands are selected such a way that, proposed system can be tested for all four quadrants of operation. The various modes of operation are triggered in simulation as well as experimental setup as per the 'Step-Time' listed in TABLE – 5.2 for torque as well as speed. The simulation results obtained (shown in Figure 5.6) are compared with experimental test results to verify the proposed converter topology.

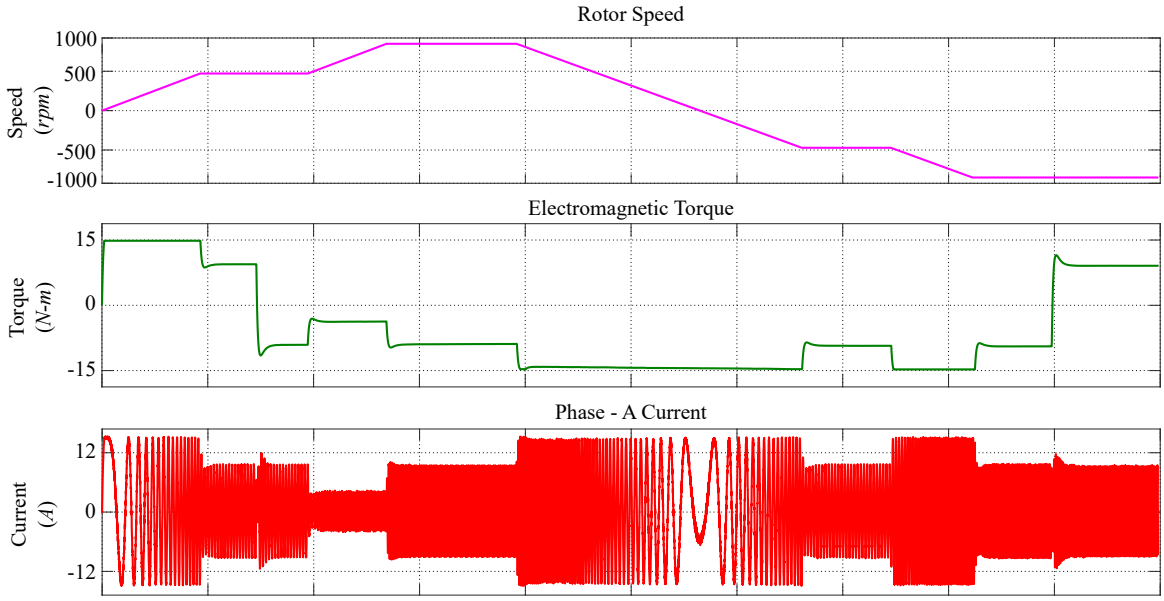

Figure 5.6: PMSM Motor - 1 estimated speed, torque and current reference signals.

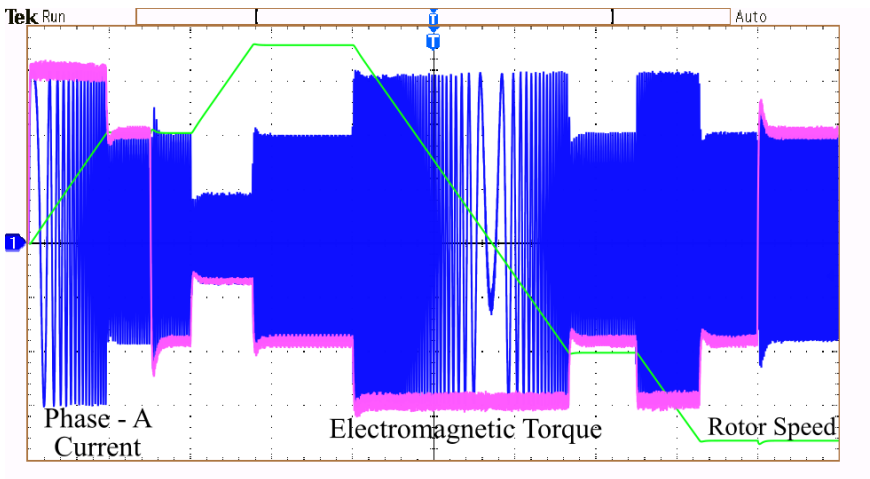

Figure 5.7: Experimental results for PMSM motor – 1.

(CH1:5A/div [Blue]; CH3:5V/div(1V/50 RPM)[Green]; CH4:5V/div(1V/Nm)[Pink]; X-axis:2.0 s/div)

Figure 5.7 to 5.11 shows experimental results for all test commands listed in TABLE – 5.2. The phase-A current waveform for current drawn from DUT is displayed on channel CH1. The signals on channel CH-3 and CH-4 on Fig. 5.7 to 5.11 are rotor speed

and electromagnetic torque estimated by motor model respectively. These speed and torque signals are displayed on oscilloscope through DAC pin of DSP controller.

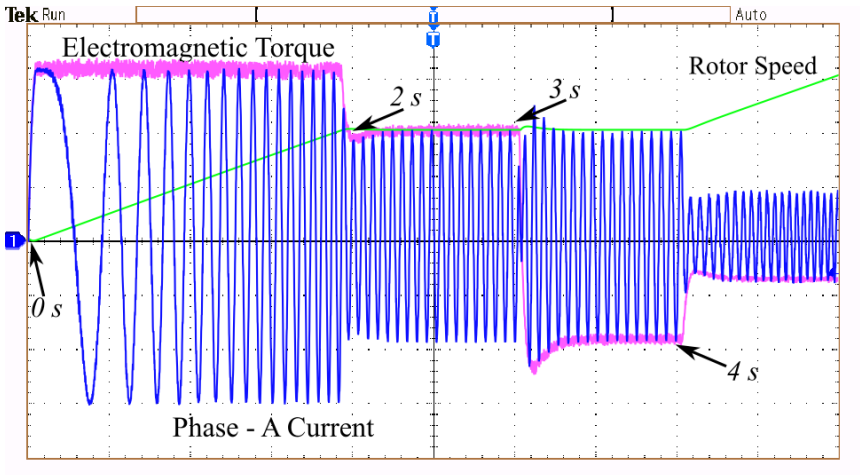

Figure 5.8: Experimental results (Zoomed view of Fig. 5.7 from 0s to 5s).

(CH1:5A/div [Blue]; CH3:5V/div(1V/50 RPM)[Green]; CH4:5V/div(1V/Nm)[Pink]; X-axis:0.5 s/div)

The results for all four quadrants are shown in Figure 5.7 for various torque and speed test commands. As shown in Figure 5.8, at time $t = 0\ s$, both speed and torque commands are set to $500\ RPM$ and $10\ Nm$ respectively. With these test commands, the emulator is expected to emulate first quadrant (forward motoring) of operation of PMSM motor under study. Until $2\ s$, when motor attains desired $500\ RPM$ speed, the emulator draws high current to emulate high starting torque as can be seen in Figure 5.8. As soon as the emulated speed reaches to desired speed reference, emulator starts drawing nominal current and electromagnetic torque drops down to its reference value i.e. $10\ Nm$. The torque remains constant to $10\ Nm$ until the next test command, which appears at $3\ s$. For initial three seconds, the ME system emulates forward motoring operation.

At $3\ s$, the torque command changes to $-10\ Nm$ to force emulation of forward braking operation. It is visible in Figure 5.8 that, as soon as the torque command changes

the, the emulated torque drops to $-10\ Nm$ and phase-A current reverses. A minor spike in current as well as speed waveform can be noticed in Figure 5.8. However, emulator still draws, the $10\ A$ peak current from DUT. At $4\ s$, the speed reference is changed to $900\ RPM$ and to operate in constant torque region, the electromagnetic torque increases from $-10\ Nm$ to $-4\ Nm$.

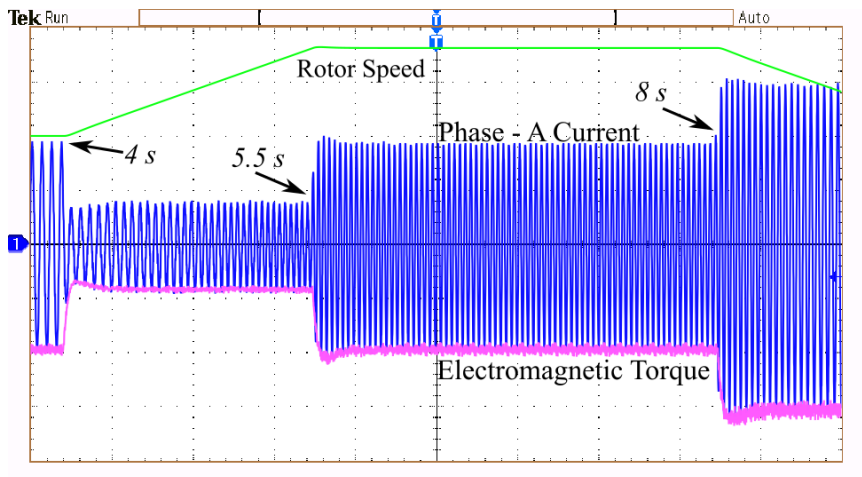

Figure 5.9: Experimental results (Zoomed view of Fig. 5.7 from 4s to 8s).

(CH1:5A/div [Blue]; CH3:5V/div(1V/50 RPM)[Green]; CH4:5V/div(1V/Nm)[Pink]; X-axis:0.5 s/div)

At $5.5\ s$, the emulator speed attains the desired reference of $900\ RPM$ as shown in Figure 5.9. The electromagnetic torque returns to the $-10\ Nm$ reference mark and remains steady until next test command appears at $8\ s$. As the speed reference is dropped to $-500\ RPM$ at $8\ s$, the braking current increases to approximately $15\ A$ peak. The emulator, draws high braking current until rotor speed is dropped to zero at approx. $11.5\ s$. At this instance, the forward braking operation ends.

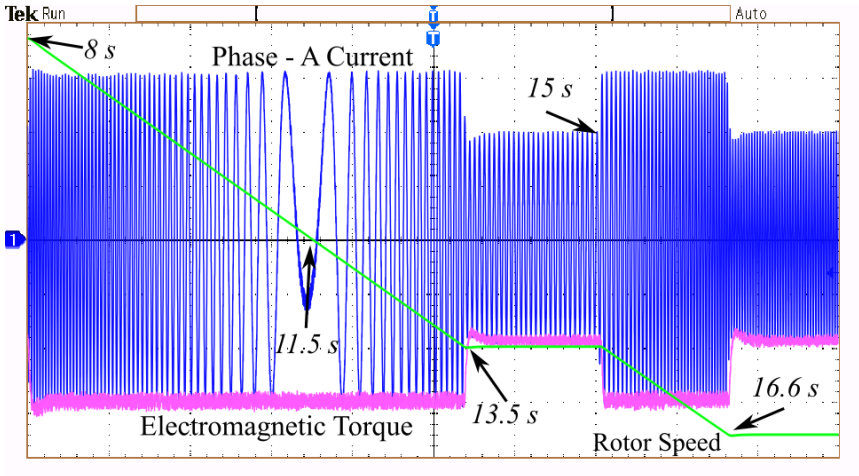

Figure 5.10: Experimental results (Zoomed view of Fig. 5.7 from 8s to 18s).

(CH1:5A/div [Blue]; CH3:5V/div(1V/50 RPM)[Green]; CH4:5V/div(1V/Nm)[Pink]; X-axis:1.0 s/div)

At $11.5\ s$, speed as well as phase reversal occurs as shown in Figure 5.10. The emulated rotor speed further drops linearly in negative direction (reverse motoring) until desired speed is attained at $13.5\ s$. The electromagnetic torque returns to its reference value of $-10\ Nm$ and remains constant until next test command appears at $15\ s$. At $15\ S$, the reference speed is further increased in reverse direction to $-900\ RPM$, as shown in Figure 5.10. The DUT supplies, the high current demand during speed increment until speed is reached to $-900\ RPM$ at $16.6\ s$. The reverse motoring operation continues till $18.0\ s$ when next test command appears.

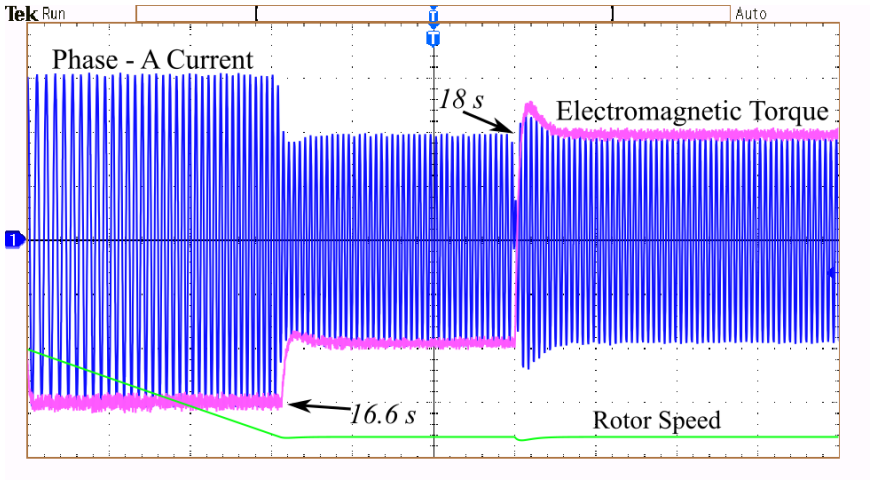

Figure 5.11: Experimental results (Zoomed view of Fig. 5.7 from 15s to 20s).

(CH1:5A/div [Blue]; CH3:5V/div(1V/50 RPM)[Green]; CH4:5V/div(1V/Nm)[Pink]; X-axis:0.5 s/div)

As shown in Figure 5.11, at $18.0\ s$, the torque reference is changed from $-10\ Nm$ to $10\ Nm$, to force reverse braking operation. This sudden braking causes minor spike in current signal, as can be noticed in Figure 5.11.

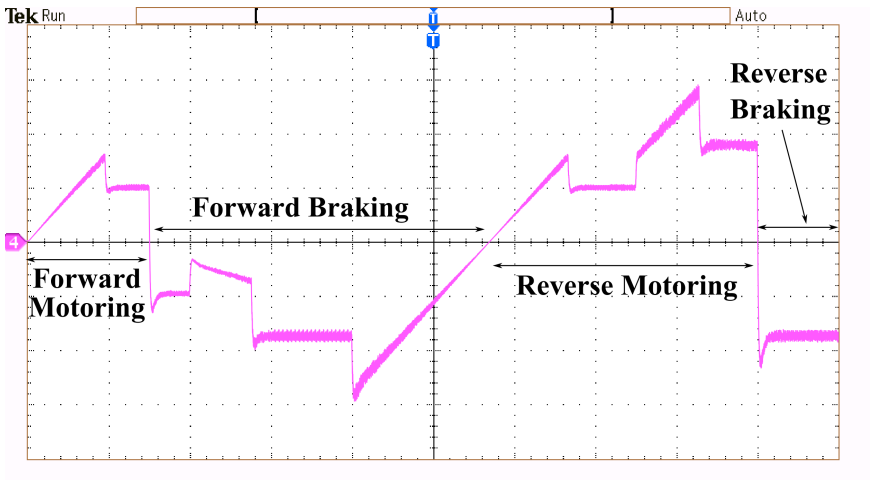

Figure 5.12: DC bus current at the output of proposed emulator converter.

(CH4:5A/div[Pink]; X-axis:2.0 s/div)

TABLE – 5.3
PMSM MOTOR – 2 PARAMETERS[88]

Motor Parameter	Nomenclature	Value
Rated Power	P_m	2.0 kW
Rated Speed	ω_r	2100 rpm
Rated Torque	T_r	9 $N \cdot m$
Rated Current	I_r	15 A
Number of Poles	P	4
Stator Resistance	R_s	0.248 Ω
Stator d-axis Inductance	L_d	8 mH
Stator q-axis Inductance	L_q	32 mH
Magnetic Flux	λ	0.367 Vs/rad
Inertia	J	5.35 kgm^2

Figure 5.12, shows the DC bus current at the output of proposed emulator converter. It can be seen in the Figure 5.12 that, during forward as well as reverse motoring operation, the emulator converter output current is pumped back into DC bus. Similarly, during forward and reverse braking mode of operation, the DC side of proposed converter act as input and draws power from DC bus. The negative current during both braking regions verifies the bidirectional operation of proposed converter.

5.5 PMSM Motor – 2 Results Analysis

The common DC-bus configured ME system presented in Figure 5.5 is also validated with MATLAB/Simulink for the proposed single loop control strategy for the motor specifications tabulated in TABLE – 5.3. The system shown in Figure 5.5 is simulated for all four quadrants to verify the proposed single loop control scheme.

Figure 5.13 shows the simulation results for the PMSM motor under emulation test. The simulation test were carried out in all four quadrants of operation, for the test command

TABLE – 5.4
TORQUE AND SPEED INPUT REFERENCE COMMANDS FOR PMSM MOTOR – 2

Operating Mode	Quadrant	Load Torque (T_L^*)	Rotor Speed ($\omega_m{}^*$)
Forward Motoring	I	3 Nm	200 RPM
Forward Braking	II	-3 Nm	300 RPM
Reverse Motoring	III	-3 Nm	-200 RPM
Reverse Braking	IV	3 Nm	-300 RPM

parameters listed in TABLE – 5.4.

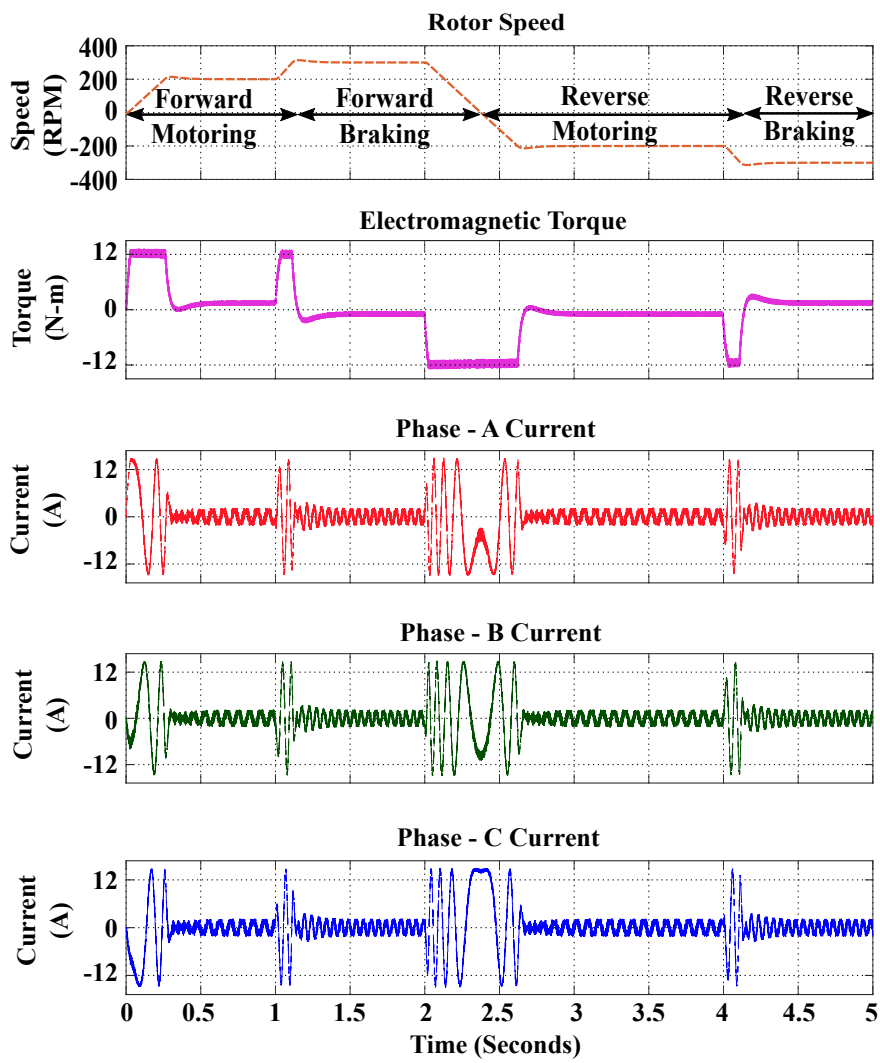

Figure 5.13: PMSM Motor - 2 estimated speed, torque and current reference signals.

Figure 5.13 shows the estimated speed, torque and current signal by PMSM motor model for four quadrant operation of proposed VETM, for the torque and speed input listed in Table - 5.2.

The proposed converter topology, control strategy and PWM scheme is implemented on hardware and tested for the parameters listed in Table - 5.3 and test conditions listed in Table - 5.4 respectively. Figure 5.14 to 5.17 shows experimental results for all four quadrants of operation. Texas Instruments DSP controller TMS320F28379D is used for implementing PMSM motor model and control strategy.

The signal on channel CH-4 in Fig. 5.14 to 5.17 is electromagnetic torque estimated by motor model in controller. This torque signal is sent on DAC pin of controller to display it on oscilloscope. The three-phase current waveform for current drawn from DUT are displayed on, channel CH1, CH2 and CH3.

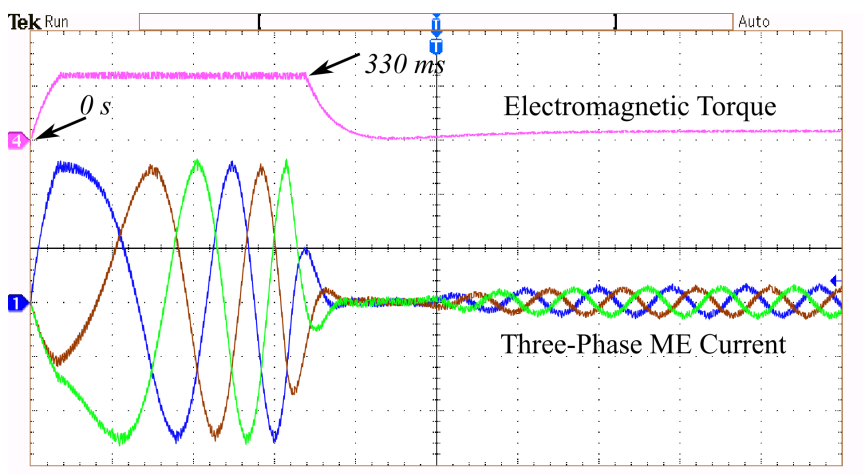

Figure 5.14: Experimental results for forward motoring operation. [CH1,CH2,CH3:5A/div; CH4:1V/div(100mV/Nm); X-axis:100ms/div]

In Fig. 5.14, at time $t = 0s$ sec, during forward motoring operation, reference speed is 200 RPM. Until, motor reaches desired speed, it draws high current resulting in high starting torque as can be seen. At approximately $330ms$, motor attains 200 RPM speed and

remains constant. From this instance onwards, motor starts drawing nominal current and electromagnetic torque drops down and matches with its reference value i.e. $3Nm$.

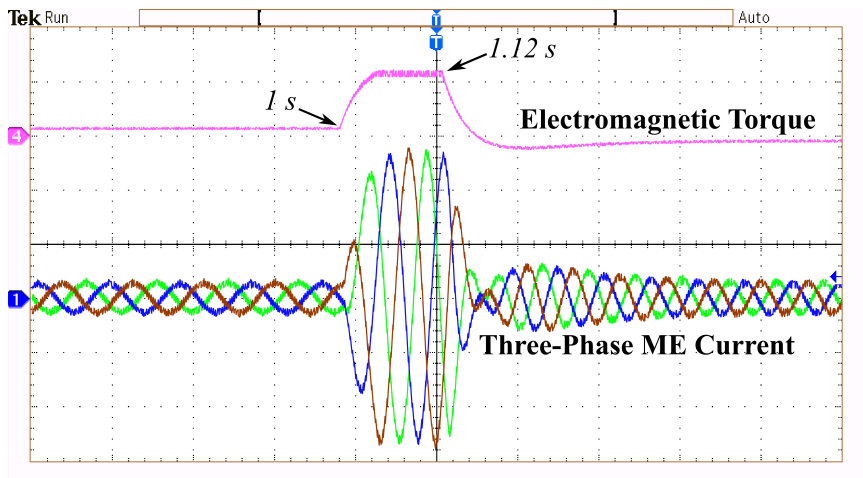

Figure 5.15: Experimental results for forward braking operation. [CH1,CH2,CH3:5A/div; CH4:1V/div(100mV/Nm); X-axis:100ms/div]

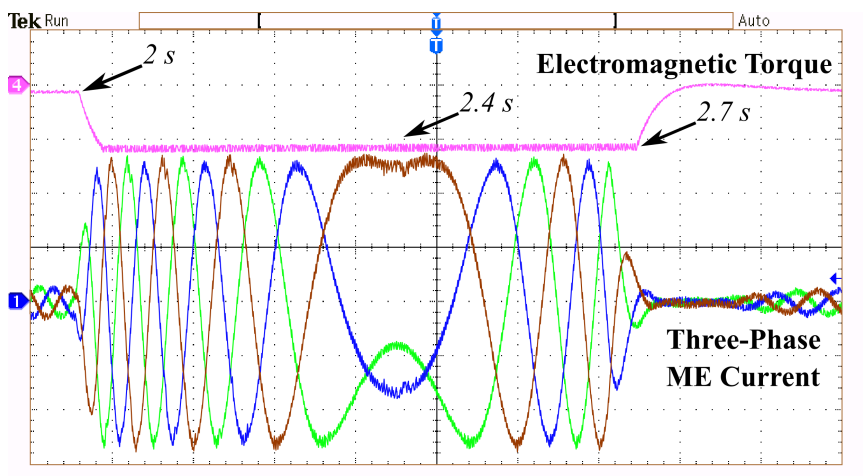

Figure 5.16: Experimental results for reverse motoring operation. [CH1,CH2,CH3:5A/div; CH4:1V/div(100mV/Nm); X-axis:100ms/div]

At time $t = 1s$ sec, the speed reference is increased to 300 RPM, while torque reference is changed to $-3Nm$ to operate motor model in forward braking mode. As shown in Fig. 5.15, until motor reaches desired 300 RPM speed, the electromagnetic torque increases

up to its saturation limit to supply high current demanded. At approximately $1.12s$, motor attains 300 RPM speed and remains constant. At this moment, electromagnetic torque drops down and matches with its negative reference value i.e. $-3Nm$ and model model operates in forward braking mode till $2s$ when next speed and torque command is applied.

At time $t = 2\ s$, the speed reference is decreased to -200 RPM, while torque reference is kept constant to $-3Nm$ to operate motor model in reverse motoring mode. Since before $2s$, the motor model was operating in forward braking region, to transfer to reverse motoring region, motor speed starts decreasing and becomes zero at approximately $2.4s$. Since speed is decreasing, resulting in more current being fed back to drive, as can be seen in Fig. 5.16 from $2s$ to $2.4s$. At $2.4s$ when speed reverses, the torques is already at its negative peak, resulting in reverse motoring mode of operation and all three-phase currents are reversed. At $2.7s$, when the motor model reaches its desired speed, the electromagnetic torque decreases to its negative reference value i.e. $-3Nm$. The motor model operates in reverse motoring region till $4s$ when next speed and torque command is applied.

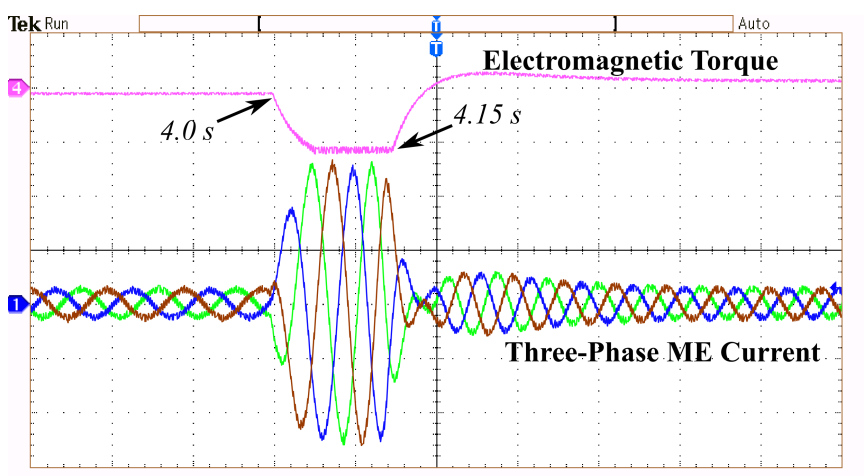

Figure 5.17: Experimental results for reverse braking operation.
[CH1,CH2,CH3:5A/div; CH4:1V/div(100mV/Nm); X-axis:100ms/div]

At time $t = 4s$, to operate motor model in reverse braking region, the speed command is further increased in negative direction to -300 RPM and torque reference is changed from $-3Nm$ to $3Nm$ as shown in Fig. 5.17. While the speed is increased to new reference value in negative direction, the current demand increase. At approximately $4.15s$ the speed reaches to -300 RPM resulting reduced current drawn from drive and the electromagnetic torque jumps from negative reference $-3Nm$ to positive to attain its new reference value i.e. $3Nm$.

It is evident that, with the control scheme presented in previous section, the proposed bidirectional AC-DC converter for VETM system draws the same current as that of estimated by PMSM motor model. In addition, the electromagnetic torque and rotor speed also matches with their estimated values from PMSM model.

5.6 Summary

A detailed mathematical model of PMSM motor as well as proposed converter is presented here. The proposed control strategy based on state feedback linearization method is thoroughly discussed. The simulation and experimental results presented for a 7.5 kW as well as 2.0 kW PMSM motor, validate the proposed common-DC-bus ME system architecture.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

In the industrial production stage of a drive, its control algorithm must be tested for its validity with real machine. Testing with real machine could pose some serious challenges. During the testing, if the control algorithm starts behaving unexpectedly, it may cause serious damage to the real machine or drive. Such hazardous operating conditions can be avoided by replacing a real machine with a power electronic converter based 'Traction Motor Emulator' (TME) test-bench. The TME can be designed to allow the device under test (DUT) to be tested at actual power with the help of a power electronic converter test setup and the motor model. The TME controls the current drawn from the DUT to match with that of estimated by the motor model. The existing TME system comprises of AC-DC followed by DC-AC converter, increasing the number of converter stages in the system. In addition, both the converters require independent control which increases the control complexity. This multistage conversion stage can be eliminated by replacing AC-DC-AC emulator with AC-DC converter supplied by common DC bus to DUT and VM both. Taking into account, this research proposes a novel single-stage, three-phase

bi-directional AC-DC converter topology suitable for TME system.

A simplified, bidirectional, three-phase AC-DC converter for TME system is proposed in this research. The proposed bidirectional converter inspired from classical buck-boost operation, requires just ten unidirectional IGBT switches. The unidirectional IGBT switches prevents any circulating current in the system. The proposed converter also takes out the regenerative converter stage in classical ME system. Also, the proposed common DC-bus-configured ME system requires a single stage control unlike independent control in existing ME system. The proposed converter provides four-quadrant operation and emulation of motor under study.

The common DC-Bus-configured ME system emulating a AC synchronous motor is validated with the MATLAB simulation. For a three-phase system with LCL filter, conventionally a double-loop control is preferred. However, this research proposes a simplified single loop control strategy. The decoupling equation derived from state feedback linearization method are presented here. From the obtained simulation results, it is inferred that, with proposed current control scheme the common DC-Bus-configured motor emulator system emulates the behaviour of a rotational PMSM motor electrically. The advantage of such common-DC-bus configured system is that the dc power source supplies the electric power equal to the total power loss in the ME system.

From the experimental results, it is concluded that, with the proposed single-loop control scheme, the proposed ME converter can be made to draw the same current as a real machine would have drawn, had it been driven by the same DUT. The PMSM motor model is used to estimate the reference current used for controlling the proposed converter. This provides re-configuration ability to ME system. The reconfiguration ability can be verified from the experimental results presented for the two different PMSM motors emulated on the same test bench setup.

Overall, by analyzing experimental results, it is verified that, proposed bidirectional AC-DC converter topology is a feasible alternative for conventional ME system with AC-DC-AC converter, providing simple common control.

6.2 Future Research Scope

This research work can further be extended to analyze the traction motor drives using the traction motor emulators in test environment. From the simulation and experimental results it is verified that by changing the motor parameters the ME system can behave as an all new motor under emulation. This feature can further be extended to emulate the different types of AC motors such as SRM (Switched Reluctance Motor), IM (Induction Motor) etc. using the same common-DC-bus ME system.

In common-DC-Bus power electronic converters system, the DC link capacitor life-cycle is a dominant issue. This research work can further be extended to perform the life-cycle analysis of the DC link capacitor.

For motor drives testing, the behaviour of motor drives under various test such as unbalanced motor phase voltage, loss of phase signal, cogging and crawling torque conditions, motor flux weakening conditions are important to know. Therefore this research work can be further extended to carry out such test on the EV motor drive to better understand the drive performance.

6.3 Future Application Scope

Bidirectional AC-DC power converter can find ways in to wide range of applications. The proposed converter, being a single stage buck-boost AC-DC converter, can be used in –

1. **Vehicle-to-grid (V2G) and Grid-to-vehicle (G2V):** As the automobile industry is focusing towards electric vehicles (EVs), the EVs can serve as future micro-grids supplying excess power (if available) to the grid or charge the EV battery from the grid power source using the same bidirectional power converter.

2. **EV Motor Drivetrain:** With the integrated buck-boost capability, the proposed bidirectional power converter can find its way into EV motor dirvetrain. Having buck-boost converter at the DC side input port would allow using low voltage battery pack, resulting in efficient battery pack management.

3. **Solar Micro-inverter:** A scaled-down version of proposed power converter can also be used in solar micro-inverter applications. Solar micro-inverter is a compact low power DC-AC converter attached to solar panel back cover.

4. **Universal Power Converter:** Given the bidirectional capability and four quadrant operation of proposed converter, it can be used as an Universal power converter as DC-DC, DC-AC, AC-DC or AC-AC converter.

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[88] S. Taniguchi, S. Mochiduki, T. Yamakawa, S. Wakao, K. Kondo, and T. Yoneyama, "Starting procedure of rotational sensorless pmsm in the rotating condition," *IEEE Transactions on Industry Applications*, vol. 45, no. 1, pp. 194–202, 2009.

Appendix A

Publications

List of publications based on this research work —

A.1 Journal Publications

[1] **A. H. Kadam**, and S. S. Williamson, "A common DC-bus-configured traction motor emulator using a virtually isolated three-phase AC-DC bidirectional converter," *in IEEE Access*, vol. 9, pp. 80621-80631, 2021.

DOI: 10.1109/ACCESS.2021.3085029.

[2] **A. H. Kadam**, and S. S. Williamson, "An electric traction system emulator using state feedback linearization single-loop control method," *in Journal of Emerging and Selected Topics in Industrial Electronics*. **(Under Review)**

A.2 CONFERENCE PUBLICATIONS

[1] **A. H. Kadam**, and S. S. Williamson, "Single loop control of a common DC-bus-configured traction motor emulator using state feedback linearization method," *2021 IEEE Southern Power Electronics Conference (SPEC)*, Kigali, Rwanda, 2021, pp. 1–6.

DOI:10.1109/SPEC52827.2021.9709486.

[2] **A. H. Kadam**, R. Menon, and S. S. Williamson, "A novel three-phase bi-directional buck-boost AC-DC converter for PMSM virtual machine system with common DC bus," *IEEE Applied Power Electronics Conference and Exposition-2018 (APEC–2018)*, San Antonio, TX, USA, 2018, pp. 1944–1951.

DOI: 10.1109/APEC.2018.8341284.

[3] **A. H. Kadam**, R. Menon, and S. S. Williamson, "A four-quadrant three-phase AC-DC converter for virtual electric traction machine," *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, TN, India, 2018, pp. 1–6.

DOI: 10.1109/PEDES.2018.8707625.

[4] **A. H. Kadam**, R. Menon, and S. S. Williamson, "Traction inverter performance testing using mathematical and real-time controller-in-the-loop permanent magnet synchronous motor emulator," *IECON 2016 – 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, 2016, pp. 6651–6656.

DOI: 10.1109/IECON.2016.7793156.

Appendix B

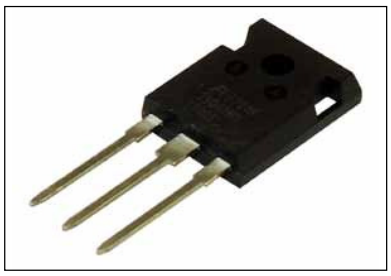
Reverse Blocking IGBT

FGW85N60RB

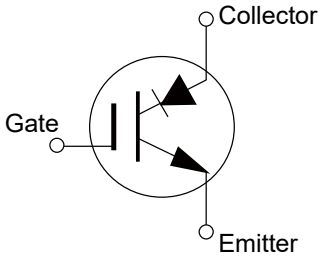
Fuji Electric

FGW85N60RB

Reverse Blocking IGBT
600V / 85A



■ **Equivalent circuit**



■ **Features**

Reverse blocking characteristic for 1 chip by Fuji's original technology.
High eff ciency by applying to T-type 3 level inverter circuit.

■ **Applications**

Uninterruptible power supply
Power conditioner
Battery system

Figure B.1: Equivalent circuit, features and applications.

TABLE – B.1
ABSOLUTE MAXIMUM RATINGS

● Absolute Maximum Ratings at T_j=25°C (unless otherwise specif ed)

Items	Symbols	Characteristics	Units	Remarks
Collector-Emitter Voltage	V_{CES}	600	V	
Repetitive Peak Reverse Voltage	V_{RRM}	600	V	
Gate-Emitter Voltage	V_{GES}	±20	V	
DC Collector Current	$I_{C@25}$	100	A	T_C=25°C,T_j=150°C Note *1
	$I_{C@100}$	85	A	T_C=100°C,T_j=150°C
Pulsed Collector Current	I_{CP}	170	A	Note *2
Turn-Off Safe Operating Area	-	170	A	V_{CE}≤600V,T_j≤150°C
Short Circuit Withstand Time	t_{SC}	10	μs	V_{CC}≤300V,V_{GE}=15V T_j≤150°C
IGBT Max. Power Dissipation	P_{D_IGBT}	600	W	T_C=25°C
Operating Junction Temperature	T_j	-40 ~ +150	°C	
Storage Temperature	T_{stg}	-55 ~ +150	°C	

Note *1 : Current value limited by bonding wire.
Note *2 : Pulse width limited by Tjmax.

TABLE – B.2
ELECTRICAL AND THERMAL SPECIFICATIONS

● Electrical characteristics at T_j= 25°C (unless otherwise specif ed)

Description	Symbols	Conditions		Characteristics min.	typ.	max.	Units
Collector-Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C = 1mA, V_{GE} = 0V		600	-	-	V
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 600V, V_{GE} = 0V	T_j=25°C	-	-	250	μA
			T_j=150°C	-	-	10	mA
Gate-Emitter Leakage Current	I_{GES}	V_{CE} = 0V, V_{GE} = ±20V		-	-	200	nA
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	V_{CE} = +20V, I_C = 85mA		5.5	6.5	7.5	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{GE} = +15V, I_C = 85A	T_j=25°C	-	2.45	2.80	V
			T_j=150°C	-	2.95	-	
Input Capacitance	C_{ies}	V_{CE}=10V		-	5100	-	pF
Output Capacitance	C_{oes}	V_{GE}=0V		-	1150	-	
Reverse Transfer Capacitance	C_{res}	f=1MHz		-	740	-	
Gate Charge	Q_G	V_{CC} = 400V I_C = 85A V_{GE} = 15V		-	300	-	nC
Turn-On Delay Time	$t_{d(on)}$	T_j = 25°C		-	35	-	ns
Rise Time	t_r	V_{CC} = 400V		-	85	-	
Turn-Off Delay Time	$t_{d(off)}$	I_C = 85A		-	175	-	
Fall Time	t_f	V_{GE} = ±15V		-	64	-	
Turn-On Energy	E_{on}	R_G = 10Ω		-	4.7	-	mJ
Turn-Off Energy	E_{off}	L = 500μH Energy loss include "tail" and FWD (FDRW30S120J) reverse recovery.		-	2.4	-	
Turn-On Delay Time	$t_{d(on)}$	T_j = 150°C		-	30	-	ns
Rise Time	t_r	V_{CC} = 400V		-	125	-	
Turn-Off Delay Time	$t_{d(off)}$	I_C = 85A		-	185	-	
Fall Time	t_f	V_{GE} = ±15V		-	66	-	
Turn-On Energy	E_{on}	R_G = 10Ω		-	6.0	-	mJ
Turn-Off Energy	E_{off}	L = 500μH Energy loss include "tail" and FWD (FDRW30S120J) reverse recovery.		-	3.0	-	
Reverse Recovery Time	t_{rr}	V_{CC} = 400V I_C = 85A V_{GE} = ±15V R_G = 30Ω L = 500μH	T_j=25°C	-	165	-	ns
			T_j=150°C	-	330	-	

Thermal Resistance

Description	Symbols	min.	typ.	max.	Units
Thermal Resistance, Junction-Ambient	$R_{th(j-a)}$	-	-	50	°C/W
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	-	-	0.208	