Modified Wavelet-based Pulse Width Modulation Technique for Cascaded H-Bridge Multilevel Converter

By

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An oral defense of this thesis took place on April 25, 2023, in front of the following examining committee:

Examining Committee:

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The above committee determined that the thesis is acceptable in form and content and that a satisfactory knowledge of the field covered by the thesis was demonstrated by the candidate during an oral examination. A signed copy of the Certificate of Approval is available from the School of Graduate and Postdoctoral Studies.

ABSTRACT

Power electronics (PE) converters are crucial for providing a cost-effective, reliable, and efficient solutions for integrating renewable energy sources (RES) into the electrical grid. Over the years, many converter topologies have been developed for low, medium, and high voltage applications. However, they work more efficiently when appropriate modulation techniques are used. Many pulse width modulation (PWM) methods have been presented to decrease output harmonics, such as carrier-based (PWM methods, selective harmonic elimination (SHE), and nearest-level modulation (NLM). Regardless, these methods raise the complexity and expense of the converter, reduce the fundamental component, and increase high-frequency harmonics in the output signal.

In the present work, a novel wavelet-based PWM (WPWM) method is developed for a multilevel converter. This mathematical modulation technique reduces the harmonic content at both low and high frequencies, improves the fundamental component in the output, and reduces switching losses. However, in multilevel converters, the gate pulses generated by WPWM are designed to only shape the output voltage without considering the load balancing between the DC sources or split capacitors. Hence, an additional load-balancing algorithm is necessary. This work proposes a new phase-shifting WPWM method that naturally balances load sharing between all the DC sources or split capacitors in the multi-level converter.

This method operates at a low switching frequency, thereby keeping switching losses low, and reducing total harmonic distortion (THD).

Moreover, since the proposed method is a mathematical closed-form PWM method, it can be evaluated within a finite number of iterations as compared to the open-ended SHE method. The proposed method is simple and runs efficiently in real-time, which enables fast system dynamics during transient conditions. Also, it does not depend on a minor computational time-step. Hence, it can be implemented on a low-cost digital controller. The validity of the proposed method is validated both by MATLAB/Simulink model, LTSpice model, and experimental tests. The results are discussed and compared against other PS-PWM methods to demonstrate the advantages of the proposed method.

Keywords: Power electronics; pulse-width modulation; wavelet; harmonic distortion; multilevel converter

AUTHOR'S DECLARATION

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STATEMENT OF CONTRIBUTIONS

I hereby certify that I am the sole author of this thesis and that no part of this thesis has been published or submitted for publication. I have used standard referencing practices to acknowledge ideas, research techniques, or other materials that belong to others. Furthermore, I hereby certify that I am the sole source of the creative works and/or inventive knowledge described in this thesis.

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LIST OF ABBREVIATIONS

ANPC	Active Neutral-Point Clamped
APOD-PWM	Alternate Phase-Opposition Disposition
BESS	Battery Energy Storage Systems
BJT	Bipolar Junction Transistor
CHB	Cascaded H-bridge Converter
CSC	Current Source Converter
CT	Continuous Time
EMI	Electromagnetic Interference
FB	Full-Bridge
FC	Flying Capacitor
GA	Genetic Algorithms
GE	General Electric
GTO	Gate Turn-off Transistor
HV	High Voltage
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IPD-PWM	In-Phase-Disposition
LSC-PWM	Level-Shifted Carrier PWM
LV	Low Voltage
MCT	MOS-Controlled Thyristor
MC-PWM	Multi-Carrier PWM
MLC	Multilevel Converter
MLI	Multilevel Inverter
MMC	Modular Multi-Level Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MRA	Multi-Resolution Analysis
NLM	Nearest-Level Modulation

NNPC	Nested Neutral-Point Clamped
NPC	Neutral-Point Clamped
NR	Newton-Raphson
PE	Power Electronics
POD-PWM	Phase-Opposition Disposition
PSC-PWM	Phase-Shifted Carrier PWM
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
RMS	Root Mean Square
SCR	Silicon-Controlled-Rectifier
SHE	Selective Harmonic Elimination
SM	Sub-Module
SOC	State of Charge
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VSC	Voltage Source Converter
WPWM	Wavelet-based PWM
ZSC	Impedance Source Converter

Chapter 1. Overview, research goal, motivation, and contribution

1.1 Introduction

This chapter provides a brief overview of power electronic (PE) converters. After that, it presents the research goals of this study. Later, it presents the motivation behind this research and the contributions made followed by an outline of this thesis.

1.2 Introduction to power electronic converters

PE converters transform electrical energy from one state to another utilizing PE switches and appropriate control techniques [1], [2]. They are used in many applications, like power systems, renewable energy systems, electric vehicles, battery energy storage systems (BESS), motor drives, power supplies, and uninterruptible power supply (UPS) systems, as well as home appliances.

The DC-AC PE converters (or inverters) control its signal amplitude and frequency. These converters can be either 2-level or multi-level converters, based on their generated output signal [3]–[5]. The 2-level (H-bridge) converters are primarily suited for low/medium power applications. In contrast, the multi-level DC-AC converters are utilized in medium/high power/voltage applications. Multi-level converters are further classified as consolidated or cell-type converters. In the cell-type multi-level converters, several units of single-phase H-bridge cells are connected in a string to achieve a multilevel output signal. Because of the modular setup cell-type multi-level converters are easy to expand to achieve multi-level output signal. However, all PE converter topologies require suitable pulse width modulation (PWM) technique to operate it efficiently.

1.3 Research goal

The working principle of carrier-based PWM technique is that converter's switches turn ON/OFF by comparing a fundamental frequency reference signal (V_{ref}) with a higher frequency carrier signal (V_{cr}). The reference frequency of V_{ref} is also a desired frequency of the AC output and a carrier signal's frequency V_{cr} contains the anticipated switching frequency. When the amplitude of V_{ref} is greater than V_{cr}, the top switch in one leg of 2-level voltage source converter (VSC) will be ON and bottom switch will be OFF. On the contrary, if the amplitude of V_{ref} is lesser than V_{cr}, the bottom switch in one leg will be ON and top switch will be OFF. Since this technique uses a carrier signal, it is identified as a carrier-based PWM technique. In CHB-MLC, multiple 2-level cells are employed, so multiple carrier signals are required, consequently it is known as multi-carrier based PWM (MC-PWM) method. MC-PWM is a common control method used in the industry these days. Therefore, it is considered the benchmark in all the assessments being presented. The MC-PWM technique, moves energy from the lower-order harmonics to the higher-order harmonics. Consequently, the size of the required filter is reduced. However, the fundamental component in the output signal also been reduced as it is directly connected with the filtration process and increases the switching losses.

A newly developed modulation method is presented herein, which is based on a mathematical equation, called modified wavelet based PWM technique. This method lowers the total harmonic distortion (THD) and improves the fundamental component and decrease the switching losses.

The modified wavelet PWM (modified WPWM) technique is a mathematical technique. It does not use carrier signals, instead it uses a pair of wavelet analysis (equation (1-1)) and synthesis scaling function (equation (1-2)).

$$\varphi_{\mathrm{n}}(\mathrm{t}) = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left[\emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\ \mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right] \quad (1\text{-}1)$$

$$\tilde{\varphi}_{\mathrm{n}}(t) = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left\{\emptyset_{H_{\mathrm{n}}}(t) - \left[\emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\ \mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]\right\} \quad (1\text{-}2)$$

Where, $\mathrm{n} = 1,2,\ldots,\mathrm{N}$;

$\mathrm{j} = 1,2,3\ldots$; and $\mathrm{j} \in \mathbb{Z}$;

m = modulation index.

L = number of levels

This modulation strategy creates the phase angle difference for each H-bridge module's switching pulses (indicated as $\left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)$ in equations (1-1) and (1-2)). This phase angle disposition depends on the total number of connected modules (i.e., N).

The modified wavelet-based modulation technique generates a non-uniform finite number of switching pulses during each cycle. The switching pulses for each module can be generated using the analysis function (equation (1-2)), which creates two samples (stored as a group g). The relationship between the scaling variable j and the time interval of each sample group can be indicated as equations (1-3) and (1-4) respectively. The synthesis function (equation (1-2))

connects both samples and generates the switching pulse. The distance between samples (width of the pulse) in each pair (i.e., the pulse width) will change as the scale j changes.

$$tg_{n1} = \left(\frac{2\pi(2L_n+1)}{4*L}\right)\left[\frac{g}{2} - \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (1\text{-}3)$$

$$tg_{n2} = \left(\frac{2\pi(2L_n+1)}{4*L}\right)\left[\frac{g}{2} + \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (1\text{-}4)$$

Where $j = 1,2,3 \ldots$ and $j \in \mathbb{Z}$;

g = 1, 2, 3, …..

m = modulation index

L = number of levels

The proposed modified WPWM method is an entirely mathematical PWM method with a closed-form solution. It does not depend on a carrier signal. Therefore, this method is much more suitable for implementing on any digital controller, such as a microcontroller, DSP, or FPGA.

1.4 Motivation for this work

Modern electric power infrastructure is being developed globally. Renewable energy sources (RES) like solar and wind are essential to electric power generation in this infrastructure. The BESS can be incorporated with renewable energy sources to increase the sustainability of supply to the load [6], [7]. However, BESS can also be used alone to deliver electricity to an isolated load [8], [9] and its use BESS has grown globally [10], [11]. This system can be

used for diverse applications, such as peak shaving, time-shifting, and spinning reserves [7].

PE converters are essential components for future power systems, but they are known to create distortion/harmonics in the power system because of their switching effects [12]. The harmonic distortion can be reduced within the conversion (operation) when the PE converter operates with a suitable PWM technique. For example, conventional MC-PWM CHB-MLC's output contains significant levels of high-frequency distortion, which can be filtered easily. However, the conversion process is not efficient in high-voltage applications due to the increased switching losses [13]. Designing new converter topologies [14]–[18] is one tactic to reduce THD and increase the PE converter's efficiency. The transformer-less PE converter design eases commissioning and supervision costs. A 2-level VSC design with several PE switches linked in series can be employed to connect a medium/high voltage grid without a transformer to block higher input voltages (Figure 1.1) [19], [20]. This design, however, needs a complicated control scheme to ensure ON/OFF synchronization in all switching actions, which puts an extra load on the controller. Moreover, a lower switching frequency decreases switching losses in higher voltage applications. However, lowering switching frequency raises the magnitude of lower-order harmonics, which boosts the filter size and price of the system [21]. Therefore, multilevel converters are preferred to link DC sources without a transformer to the medium/high voltage AC grid [22]. Multilevel converters like CHB-MLC and

modular multilevel converter (MMC) equip the modular structure, improving scalability and reducing system losses [23]–[25].

The CHB-MLC can be employed either as a star or delta configuration. The use of star configuration is less costly and supplies more acceptable stability with a grid-linked arrangement. A 500-kW star CHB-MLC formation for BESS was successfully used in actual applications [25]. The BESS system can be tied straight to the mega-voltage (MV) grid without a step-up transformer employing the CHB-MLC design [26]. In addition, this strategy can be joined to a battery bank with or without DC/DC converter phase [22], [23]. Moreover, each converter cell has its battery group to manage power flow, helping each call's isolated input voltage need for this topology. The main benefits of this converter design are modularity, fault-tolerant, low-frequency switching function, and increased output voltage quality [27], [28].

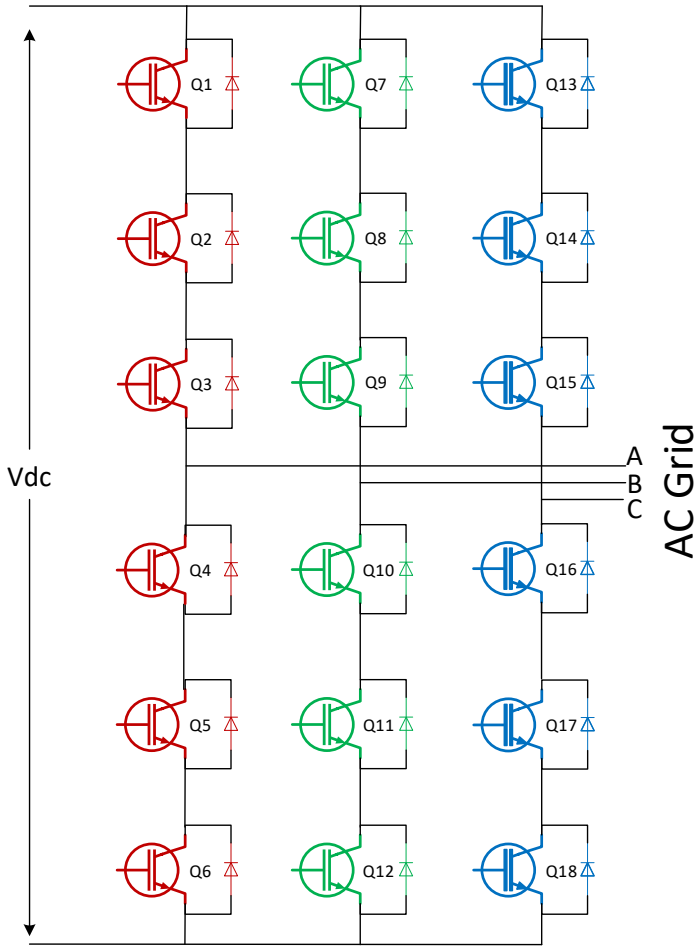


Figure 1.1: 2-level converter connected to the high voltage grid without transformer.

The MMC is another cell-type MLC consisting of several half-bridge or H-bridge power unit series per phase [29]–[31]. It shows benefits like the CHB-MLC. Besides, this design has circulating currents in the upper and lower arms, regulating active power between DC and AC systems. Therefore, it has a better state of charge (SOC) control [32]–[35]. Moreover, this design permits two different kinds of battery connections to the converter, as shown in Figure 1.2 and Figure 1.3. The batteries are connected between the power units per phase in the first configuration. The batteries are tied to the physical DC link in the

second configuration. However, batteries tied in each cell can infuse DC-current into the grid because of the distress voltages in each cell [36]. Furthermore, a circulating current exists between the arms of the DC/AC converter and the batteries, lessening battery life. Therefore, this is a significant problem in this design [37]–[39].

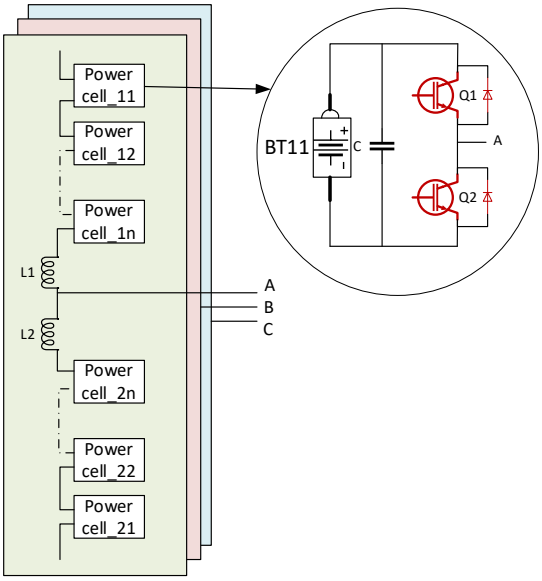


Figure 1.2: Batteries are connected between the power units of each phase in MMC.

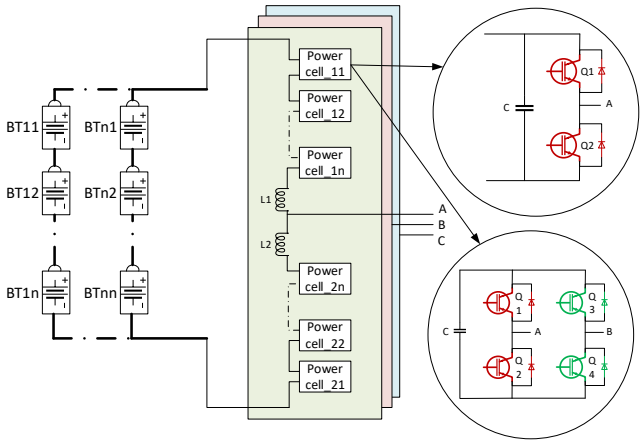


Figure 1.3: Batteries are connected in between the physical DC-link in MMC

Escalating the fundamental frequency element and lowering the THD are the main aims of several PWM techniques [40]–[43]. Other scholars think the transformation in the PWM technique will increase the converter's efficiency in a helpful method. The PWM technique shown in [42], operates the switching action according to the line-to-line voltage in place of the phase voltage in 3ϕ systems. This technique generates 15.47% better-quality output signals and reduced switching losses compared to the conventional PWM method. Another control method utilizes a frequency modulation technique, including soft-switched PWM modulation [43]. This method contains the load-current to estimate a frequency, increasing the converter's efficiency by 20%. Different frequency modulation method expands the converter's efficiency by employing a sinusoidal carrier signal [44], [45]. This method decreased the switching action compared to the standard PWM method and improved the THD of the 1ϕ inverter. Like the standard PWM method, in this study third harmonic injected modulating signal is used instead of sinusoidal signal with high frequency carrier signal [40], [41]. The THD performance improved significantly (47.3%) with this approach. A different PWM method uses the DC input instead of a triangular signal with an inverted-sinusoidal carrier signal [46], [47]. This PWM tactic enhanced the fundamental component (60 Hz) and reduced THD in the output signal. Scientists enhanced the modulation tactic in multilevel converters as well. The modulation methods applied variable frequency on a five-level CHB-MLC with harmonic injected reference signal to enhance the fundamental output and decrease the THD [48]–[50].

Power conversion efficiency has acquired the consideration of many scholars. This efficiency is affected by several elements, such as fundamental components, THD, switching losses, the complexity of the implementation, and more. The focus of research is to improve conversion efficiency while improving the fundamental component and reducing the THD while switching loss is keeping low with a newly developed modified wavelet based PWM technique.

1.5 Thesis Contribution

The major contribution of this thesis is as follows:

1.5.1 Design of a modified-WPWM for the CHB-MLC

Traditionally, MC-PWM technique is used to operate CHB-MLC. This method works effectively at a higher switching frequency to eliminate lower order harmonics which are expensive to filter/eliminate. However, high frequency operation is not ideal for high power applications because of larger power losses. The proposed method generates low switching frequency pulses to minimize switching loss. In addition, it does not introduce lower order harmonics even when it operates at a low switching frequency. Therefore, filtering process for the lower harmonics can be reduced and THD performance of the converter can be improved.

1.5.2 Easily scalable modulation technique

In the MC-PWM method, the carrier signals must be re-arranged when the number of levels needs to be increased for the CHB-MLC. It is not easy to rearrange many carrier signals. The proposed method uses mathematical equations, so the operator must only assign a new equation to the added H-

bridge. It is not as complicated as the MC-PWM method. That means it is easily scalable to N number of levels.

1.5.3 Implementable on an inexpensive digital controller

Other modulation methods like MC-PWM or selective harmonic elimination (SHE) method use a microcontroller which needs smaller time steps. These types of microcontrollers are expensive. It especially increases the cost of the converter in high voltage applications in which several microcontrollers are needed to generate switching pulses. The proposed method is mathematical PWM method which provides a closed-form solution to generate switching pulses. Therefore, it. can be implemented on a low-cost digital controller.

1.5.4 Equal conduction time for all PE switches.

The proposed method displaces switching pulses horizontally to provide equal conduction time for all H-bridge cells. Therefore, conduction losses can be distributed equitably among all switches, leading to an even semiconductor junction temperature distribution. Therefore, the PE switches with low junction temperatures can be fully utilized. Moreover, the equal conduction time distributed the load current equally in all sources to balance it without additional controller.

1.6 Outline of the thesis

This thesis has seven chapters starting from the introduction in Chapter 1, which gives an overview of this research's background, goals, and outcomes. Chapter 2 presents the background and objectives of the research. Chapter 3 provides a review of the modulation techniques and wavelet based PWM

techniques developed for the PE converters. Chapter 4 describes the operation of CHB-MLC and the modeling of the modulation technique. Chapter 5 explains the newly developed modified wavelet-based modulation technique in detail. Chapter 6 compares the MATLAB simulation results of the proposed modified-WPWM method's THD and fundamental components outputs with the frequently employed multi-carrier-based phase shifted (PS-PWM) method's outputs for a single-phase CHB-MLC. Both modulation techniques are implemented using the same switching frequency and the same number of levels of CHB-MLC. The proposed method is validated in Chapter 7 using PSPICE simulation and actual hardware implementation. This simulation study is the second step to validating the results of the proposed technique; after that, the proposed method is evaluated with a single phase 5-level CHB-MLC hardware. Chapter 8 provides the conclusion of this research and future work.

1.7 Summary

This chapter presents an overview of power electronic converters which help to meet research goals. Next, this chapter provided the motivation behind the study followed by the contributions and an outline of the thesis.

The background of the PE converters and modulation techniques have been explained in the next chapter. After that, the research objective of the thesis has been discussed.

Chapter 2. Background and Research Objective

2.1 Introduction

This chapter discusses the various PE converter topologies along with their pros and cons. Furthermore, this chapter introduces the commonly used control techniques to control various voltage source converters (VSCs) topologies. In the end, it provides the pros and cons of various PWM techniques.

2.2 Background of PE converter

PE converters transform electrical energy from one state to another utilizing PE switches and appropriate control techniques [1], [2]. The usage of PE converters has grown since Bell Labs introduced the silicon-controlled-rectifier (SCR) in 1956 [13], [14]. Then, General Electric (GE) presented its prototype of an SCR-based (Silicon controlled rectifier-based) system in 1957 and released it commercially in 1958 [14]. Since then, researchers have developed many PE switches like bipolar junction transistor (BJT), metal–oxide–semiconductor field-effect transistor (MOSFET), insulated gate bipolar transistor (IGBT), gate turn-off thyristor (GTO), and MOS-controlled thyristor (MCT)...etc. [13], [14].

Today, applications in power systems, renewable energy systems, electric vehicles, battery energy storage systems (BESS), motor drives, power supplies, and uninterruptible power supply (UPS) systems, as well as home appliances, use PE converters [15] because the PE converters have the advantages of high efficiency, low maintenance, compact size, and low cost [16].

The DC-AC PE converters (inverters) convert DC power into AC power and control the sinusoidal AC output signal amplitude and frequency. These converters can be either 2-level or multi-level converters based on their generated output signal [3]–[5] (Figure 2.1).

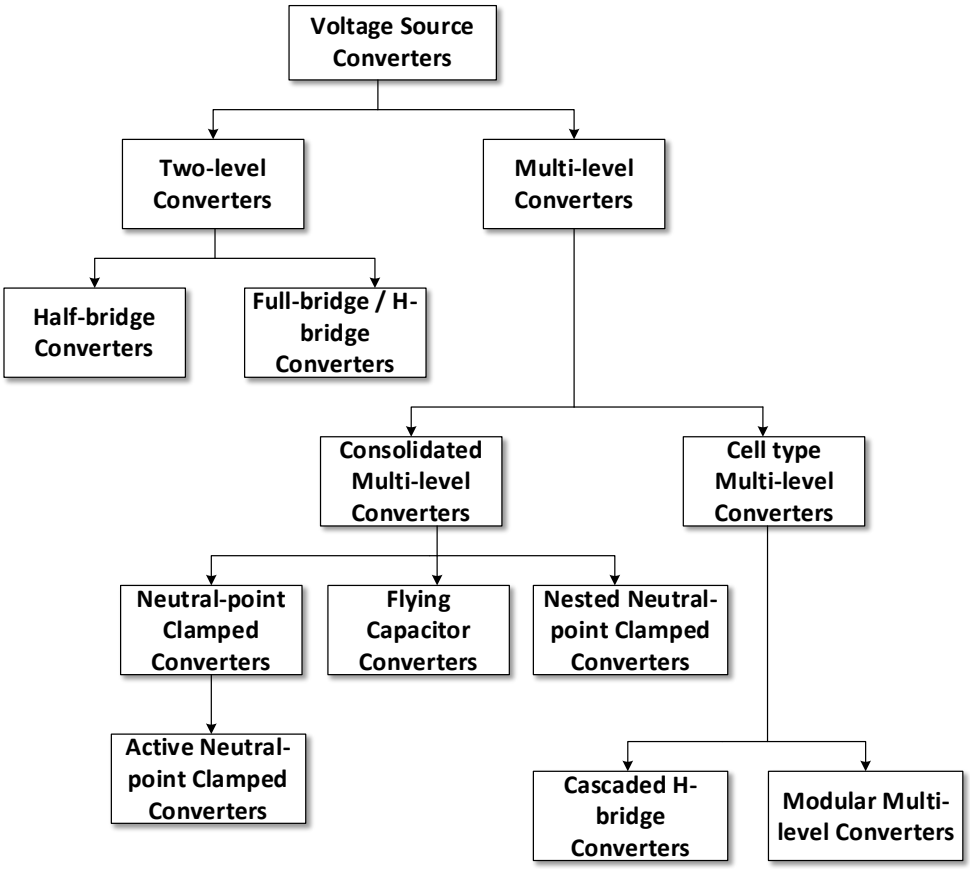


Figure 2.1: Classification of power converters

The 2-level (H-bridge) converters are better suited for low/medium power applications. These converters are either half-bridge (Figure 2.2) or full-bridge/H-bridge (Figure 2.3). These topologies are well known because of their simplicity and ease of control. Moreover, the conduction loss is less, and the efficiency is high since the conduction path is shorter in this topology. This type of inverter is

often employed in low power applications. However, it can also be used to construct multi-level converters for high voltage DC transmission (HVDC) applications [51], [52]. But, it requires extra components across the output terminals of the submodules (single half-bridge) to limit the DC-side fault current in multi-level inverter applications [53].

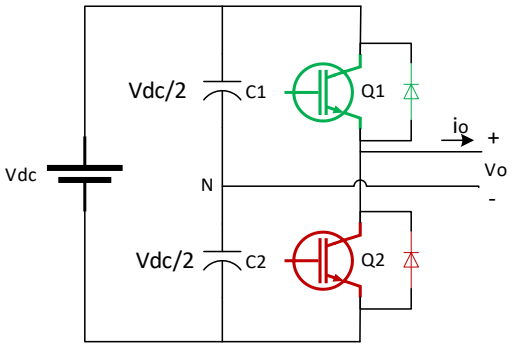


Figure 2.2: Half-bridge converter

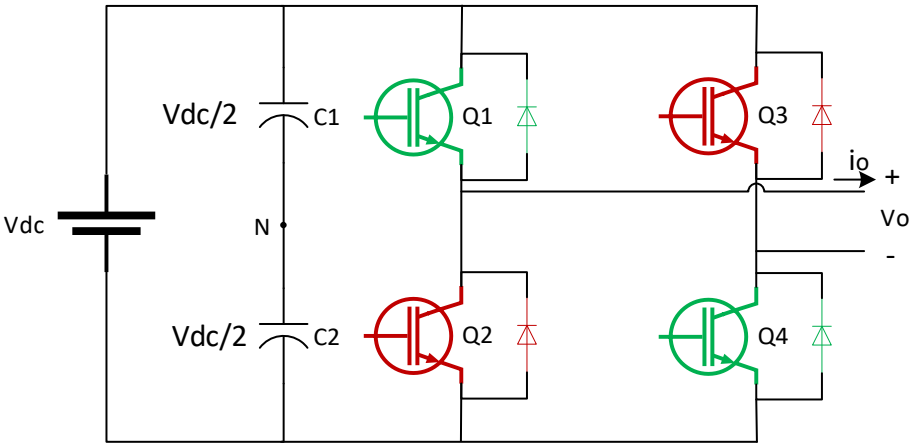


Figure 2.3: Full-bridge (H-bridge) voltage source converters

In contrast, multi-level DC-AC converters are utilized in medium/high power/voltage applications. Multi-level converters are further classified as

consolidated, or cell-type converters as shown in Figure 2.1. The consolidated multi-level converter includes Neutral point clamped (NPC), Active neutral point clamped (ANPC), flying capacitor (FC) and NNPC converter topologies. As shown in Figure 2.4, NCP converter is built of PE switches, clamping and free-wheeling diodes, and DC capacitors. It can be configured as either a 3-level, 4-level, or 5-level topology. This topology has the advantages of reduced dv/dt and lower THD (total harmonic distortion) in the output voltage compared to the 2-level converter. However, unequal power losses among the PE switches have a disadvantage, leading to an uneven semiconductor junction temperature distribution. Therefore, the PE switches with low junction temperature are not fully utilized [54]–[56], which affects the preference of the PE switches in the converter's configuration.

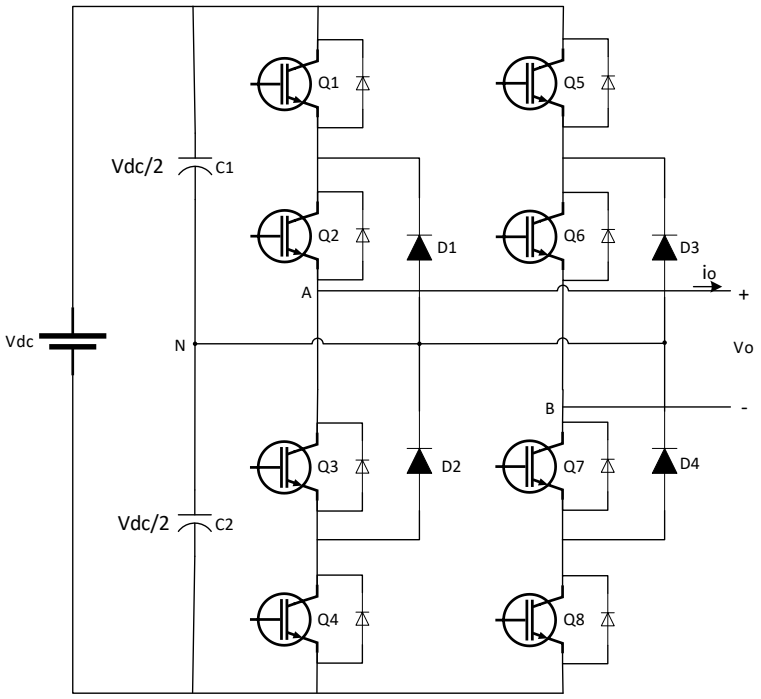


Figure 2.4: Single-phase 3-level NPC converter

The ANPC converter has solved the unequal power loss issue in NPC converter by replacing clamping diodes with active clamping PE switches as shown in Figure 2.5. Active clamping switches provide the additional redundancy switching states to control the neutral-point current, distributing power loss evenly in all switches [54], [57]–[60]. Therefore, the higher power can be utilized from all the PE switches used in this converter topology. However, adding PE switches (clamping switches) increases the price and complexity of the overall converter design.

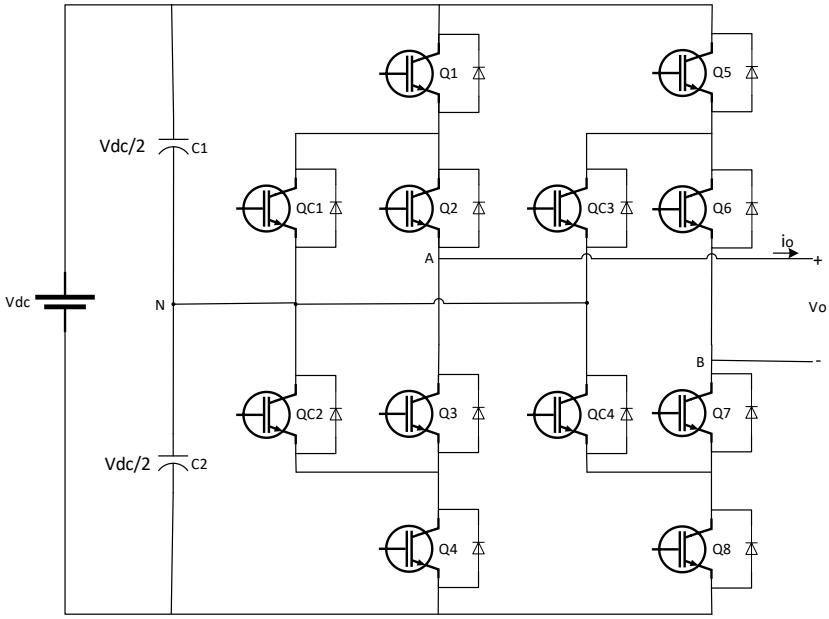


Figure 2.5: 3-level single-phase active NPC converter

Flying capacitor topology (Figure 2.6) is another consolidated type of converter used in the industry. In this topology, four PE switches and freewheeling diodes, and one flying capacitor are connected to generate 3-levels in the output signal. Unlike NPC, the equal voltage stress is inherently distributed

on all the active switches in this converter topology [61], [62]. Also, this topology becomes highly complex with the increasing number of the output voltage levels [63]. Therefore, this topology is employed to achieve a finite number of levels in the output signal. Moreover, multiple DC capacitors are needed in this converter. These flying capacitors have various voltage ratings [61]. Also, each capacitor bank requires separate dedicated charging circuits. In addition, the voltage in the flying capacitor is not constant [64]. It varies according to the circumstances. Therefore, the flying capacitor voltages need to be controlled accurately via the control circuit [63], [65], which expands the complexity of the circuit. There is another topology, Nested NPC converter (NNPC), which is the combination of FC and NPC (Figure 2.7). In this topology, the redundancy of the switching situations presents a vital need for the flying-capacitor voltage regulation.

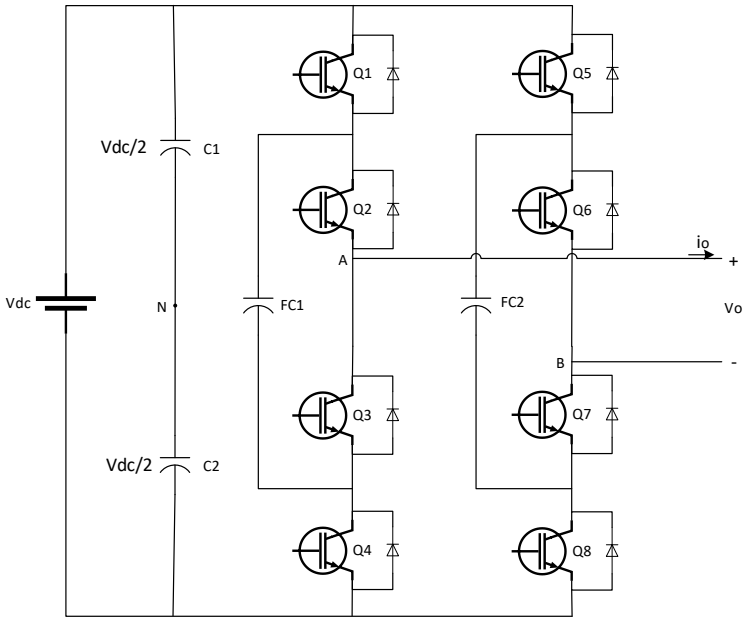


Figure 2.6: Single-phase 3-level flying capacitor converter

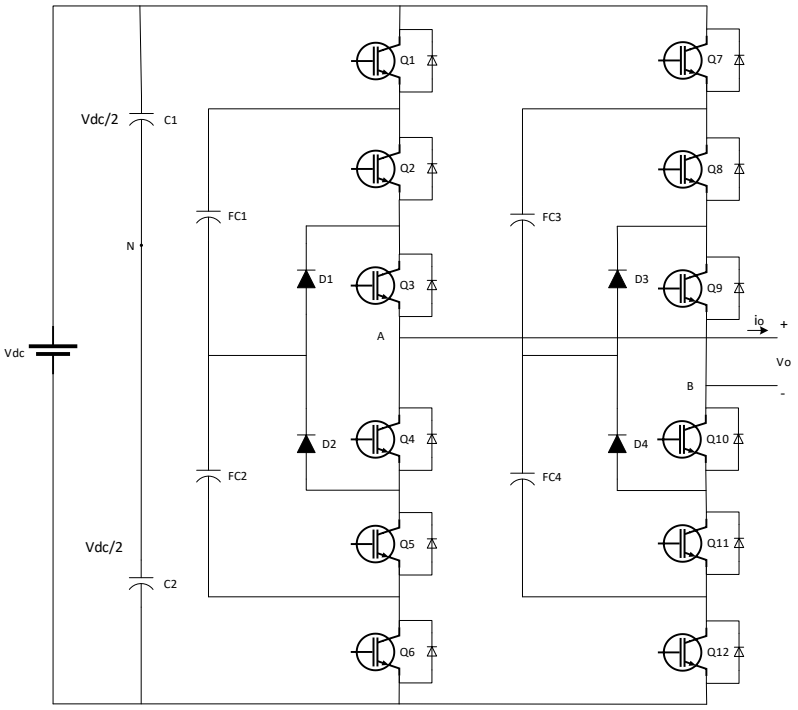


Figure 2.7: Single-phase 4-level nested neutral point clamped (NNPC) converter.

Modular multi-level converter (MMC) (Figure 2.8) and CHB-MLC (Figure 2.9) topologies are considered a cell-type multi-level converter. In this topologies, multiple cells/submodules (SM) are connected in series. There are many submodule (SM) designs that can be used, such as half-bridge SM (HB-SM), full-bridge SM (FB-SM), clamped single-SM(CS-SM), and clamped double-SM (CD-SM). Among all SM designs, the HB-SM is a familiar SM design for MMC and FB-SM is recognisable SM design for CHB-MLC. The primary difficulty in MMC design is the second-order harmonic generation due to the voltage dissimilarity between submodules [66], [67]. This issue is critical when the converter is controlled using a low-frequency modulation scheme. SM capacitors must be large enough to absorb the fundamental and second harmonic power ripples [68]. This issue is critical for low switching frequency applications, such as a

motor drive. Also, the use of a larger capacitor must be avoided because it boosts the general price of the converter [69], [70].

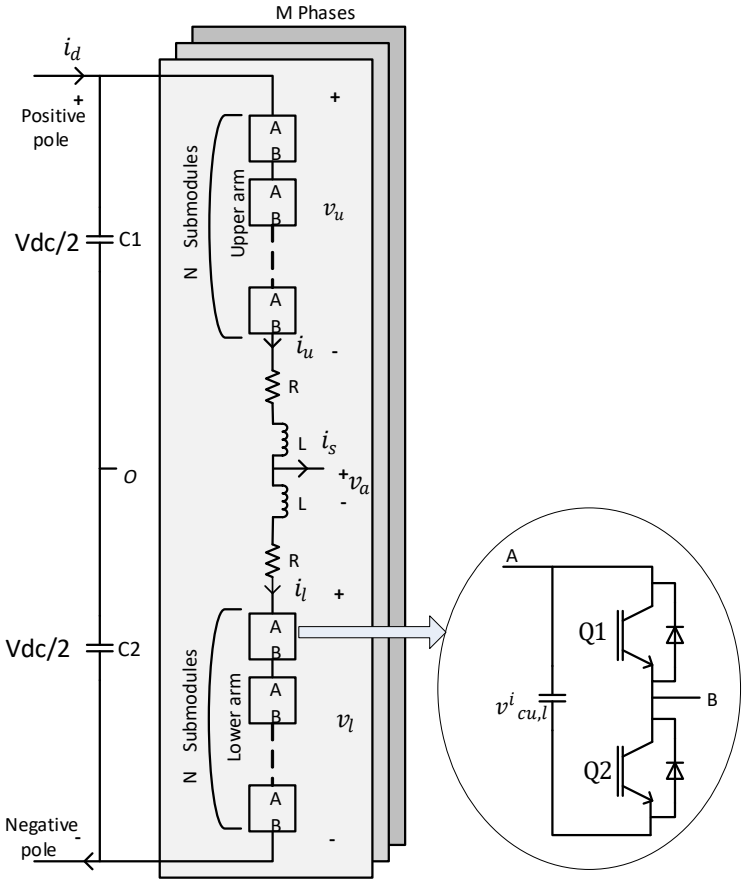


Figure 2.8: Circuit diagram and submodule of an MMC

The CHB-MLC provides modular setup and flexibility to expand levels. Several units of single-phase H-bridge cells are joined in the string to achieve a multilevel output signal in this topology. Generally, the number of H-bridge cells is determined based on their operating voltage and manufacturing price in a practical design. Also, the converter cost can be lowered by using identical H-bridge cells. In this topology, isolated DC supplies are needed to supply each H-bridge cell [19], [71]–[74].

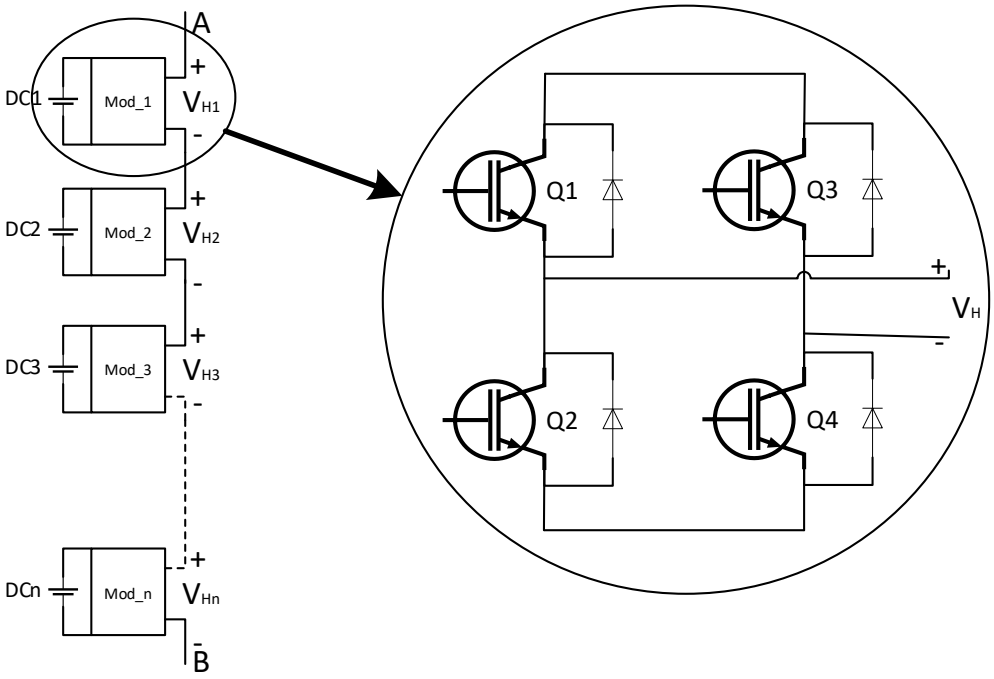


Figure 2.9: CHB multi-level converter.

Many other topologies were developed to enhance the performance and reliability of the converter. The most frequently used topologies are summarised in Table 2.1. Nevertheless, all topologies need suitable modulation techniques to operate efficiently. Some standard modulation techniques are described next.

Table 2.1: Summary of PE converters

Topology	Pros	Cons
H-bridge	• Simple construction	• Suitable for low-voltage applications
Neutral point clamped (NPC) converter	• Generate three-level output signal	• Voltage balance is unequal in the devices and clamping diodes
Active NPC converter (ANPC)	• Equal loss distribution in all devices • Provides additional redundancy switching state	• Generates positive voltage only so it does not block DC-side fault current. • It is not easily expandable for more levels in the output
Flying capacitor (FC) converter	• Higher efficiency as compared to the H-bridge modules in multi-level converter	• Can't block DC-side fault current. • More complex to extend multi-levels
Nested NPC converter (NNPC)	• Combination of NPC and FC converter	• Flying-capacitor voltage regulation is needed
Modular multi-level converter (MMC)	• Provides modular structure. • Multilevel output is easily expandable	• Capacitor charging circuit required. • Difficult to balance capacitor voltage. • Additional controller is required to control circulating current
Cascaded H-bridge multi-level converter (CHB)	• Easily scalable output signal • It can block DC-side fault current	• Isolated input voltage is required

2.3 Modulation techniques

Various modulation techniques are known to generate control pulses for the PE switches. All modulation techniques must control the output signal's fundamental and harmonic components. According to the PE converter topology, various PWM techniques are available, which can improve the converter's efficiency. They are mainly categorized as carrier-based PWM, vector-based, and selective harmonic elimination techniques.

2.3.1 Carrier-based PWM techniques

A higher frequency carrier signal (V_{cr}) is compared with the fundamental frequency reference signal (V_{ref}) to generate switching pulses in the carrier-based modulation technique. In this modulation technique, an amplitude modulation index m_a can control the fundamental-frequency (60 Hz) element in the converter output voltage. It can be expressed mathematically as,

$$m_a = \frac{\hat{V}_{ref}}{\hat{V}_{cr}} \tag{2-1}$$

$\hat{V}_{ref}$ and $\hat{V}_{cr}$ are the peak values of the reference and carrier waves, respectively. The amplitude modulation index (m_a) is usually adjusted by varying the amplitude of $\hat{V}_{ref}$ while the amplitude of $\hat{V}_{cr}$ is kept fixed. Also, the amplitude of the actual voltage can be increased by increasing the m_a above the unity. It is called over-modulation. Overmodulation is mainly avoided to limit the generation of lower-order harmonics in the output signal [75]–[78].

Similarly, the frequency modulation index m_f is defined mathematically as

$$m_f = \frac{f_{cr}}{f_{ref}} \quad (2\text{-}2)$$

Where: f_{ref} and f_{cr} are the frequency of the reference signal and carrier signal, respectively.

This technique can be synchronous or asynchronous type PWM, based on the frequency modulation index. The method is called synchronous type when m_f is an integer number; otherwise, it is anointed asynchronous type PWM [75], [76], [79], [80]. Normally, in this technique the value of m_f is higher than 21. if m_f is smaller than 21, the lower harmonic contents appear in the output signal which increases losses in the transformer and inductors [75], [76], [79], [80].

2.3.2 Vector-based PWM techniques

The space vector modulation (SVM) strategy is more suited to implement on a digital controller. This PWM method was presented for the 3-phase inverter. Also, it can be applied to a multilevel inverter [81]–[84]. The SVM approach defines the switching signals for PE switches used in the inverter by calculating a series of switching states that have been selected to be applied during the sampling period. Hence, this approach deals with the modulation as a mathematical problem obtaining the sequence of switching states and the subsequent duty cycles. This process determines the gate signals by considering VSC as a whole system, whereas the carrier-based PWM technique considers each phase separately. However, it has been confirmed that both PWM methods, space-vector and carrier-based, are equivalent (zero-sequence injection explicitly present in carrier-based PWM and implicitly in SVM), leading to the exact DC-link

utilization and harmonic performance [85]–[87]. The selection of units and the duty cycle calculation is based on the well-known space vector transformation.

2.3.3 Selective Harmonic Elimination

Selective harmonic elimination (SHE) is a non-carrier-based PWM technique. It can be applied to the 1-phase, 3-phase, 2-level, and multilevel VSC [88]–[93]. The concept of Selective Harmonic Elimination Modulation (SHE-PWM) is based on the Fourier series decomposition of the periodic PWM voltage waveform generated by a power converter. In this method, switching angles of semiconductor switches to turn ON and turn OFF are appropriately selected to eliminate the selective low order harmonics [94]–[96]. Therefore, this method provides precise control over a harmonic generation. In a 3-phase system, triplen (multiples of 3) harmonics, like 3rd, 9th, 15th…, etc. are naturally eliminated in line-to-line voltage. Therefore, these harmonics are not required to be eliminated; thus, the switching angles are used to eliminate the only 5th, 7th, 11th…, etc., harmonics as required [97], [98].

Generally, the AC output voltage showcases half- and quarter-wave symmetry. Therefore, even harmonics are eliminated in the AC waveform. Moreover, the output phase voltage waveform (v_o) should be diced N times per half cycle to alter the essential and eliminate N-1 harmonics in the AC output voltage waveform. The generated output voltage may be bipolar or unipolar in this method.

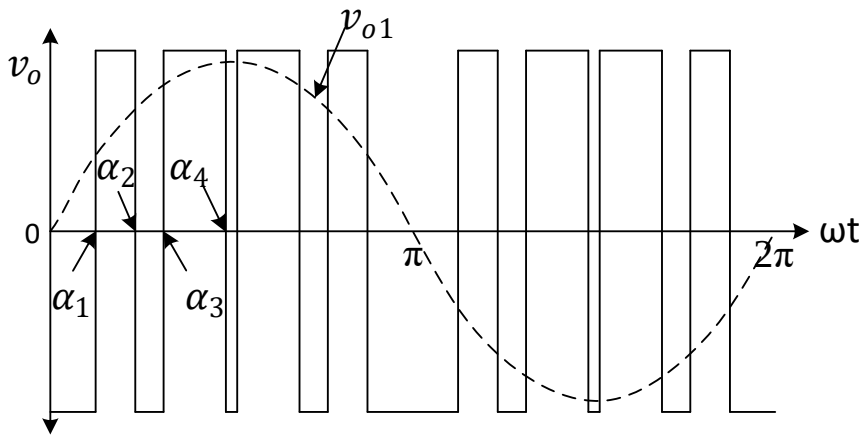


Figure 2.10: Selective harmonic elimination (SHE) technique

In the bipolar SHE technique, the general equations to eliminate an odd (like 3, 5, 7…etc.) harmonics are given as:

$$-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = \frac{(2-\pi\hat{v}_{o1})/v_i}{4} \quad (2\text{-}3)$$

$$-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = \frac{1}{2} \qquad for\ n = 3,5,\ldots,2N-1 \quad (2\text{-}4)$$

Where: $\alpha_1, \alpha_2, \ldots,\alpha_N$ should be $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \frac{\pi}{2}$.

For understanding, consider a case in which three harmonics, 3rd, 5th, and 7th, must be eliminated and the absolute magnitude controlled. To do that, four switching angles (shown in Figure 2.10 $(\alpha_1 - \alpha_4)$) need to be found by solving the following equations:

$$\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) = \frac{(2-\pi\hat{v}_{o1})/v_i}{4} \quad (2\text{-}5)$$

$$\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) = \frac{1}{2} \quad (2\text{-}6)$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) = \frac{1}{2} \quad (2\text{-}7)$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) = \frac{1}{2} \quad (2\text{-}8)$$

Similarly, in the bipolar SHE technique, the general equation to eliminate odd harmonics are given as:

$$-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = \frac{\pi}{4}\left(\frac{\hat{v}_{o1}}{v_i}\right) \quad (2\text{-}9)$$

$$-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = 0 \qquad for\ n = 3, 5, \ldots, 2N-1 \quad (2\text{-}10)$$

Where: $\alpha_1, \alpha_2, \ldots, \alpha_N$ should be $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \frac{\pi}{2}$

Therefore, to eliminate 3rd, 5th, and 7th order harmonics below the threshold needs to be solved to find switching angles (shown in Figure 2.10 $(\alpha_1 - \alpha_4)$):

$$\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) = \frac{\pi}{4}\left(\frac{\hat{v}_{o1}}{v_i}\right) \quad (2\text{-}11)$$

$$\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) = 0 \quad (2\text{-}12)$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) = 0 \quad (2\text{-}13)$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) = 0 \quad (2\text{-}14)$$

Various algorithms have been used to solve the above nonlinear equations, such as the Newton-Raphson (NR) method, particle swarm optimization (PSO), and genetic algorithms (GA) [99]–[101]. The combination of both low and high frequency produces a hybrid modulation method.

Many PWM methods are developed by the scholars. Some of them are summarised in this Table 2.2:

Table 2.2: Summary of PWM techniques

PWM	Pros	Cons
Carrier-based	• Uses higher switching frequency to reduce harmonics filtering process. • Carrier signals can be arranged in multiple ways in multi-level converter	• Switching loss is very high, especially in high voltage applications. • It is not easily scalable in multi-level converter
Vector-based	• Low switching frequency modulation technique	• Complicated to calculate vectors for the multi-level converter
Selective harmonic elimination (SHE)	• Provides fundamental switching frequency	• Can only be implemented in digital control systems. • Extremely difficult to calculate switching angles for the multilevel converter.
Nearest level modulation (NLM)	• Low switching loss	• The harmonic distortion of the output voltage and current waveforms is exceptionally increased. • It needs an SM selection process based on the DC source voltage levels to decrease the voltage surges in the source.

2.4 Summary

This chapter presents the most utilized power electronic converter topologies to understand the flexibility and complexity of expanding for the higher voltage applications. The CHB-MLI provides excellent flexibility since it has a modular structure, as well as each module is made of an H-bridge converter which is simple and easy to control. Moreover, various modulation techniques have been discussed that control the multilevel converters, as well as and expanding them for increasing the applications of the converters. In the end, it explains the pros and cons of various PWM techniques.

The next chapter reviews the commonly used PWM techniques and provides the research gap in previously developed wavelet-based modulation technique (WPWM) for CHB-MLC.

Chapter 3. Literature review

3.1 Introduction

This chapter is focused on the literature review of various modulation techniques for the high voltage power converters. Further, this chapter explains the previously studied wavelet based (WPWM) techniques for the various topologies such as, single phase H-bridge inverter, NPC, and CHB-MLC.

3.2 Literature review

As noted earlier, PE converters are employed in power systems, renewable energy plans, BESS, electric vehicles, and home devices [15], [102]. For such applications, many converter designs exist , including multilevel converters [15], [66], [74], [103]. Each new converter topology has unique challenges like DC voltage balancing, circulating currents, more available switching redundancies, and harmonic generation [67]. Among these issues, harmonic generation is a substantial problem in PE converters.

The resulting harmonics can influence the source- and load-sides of the converter. On the source-side, the harmonics influence power quality. Other sources linked to the primary source are likewise adversely impacted. Further, the source feed-in transformer gets overheated due to the harmonics in the supply line, which diminishes its efficiency and life expectancy. Moreover, the harmonics expand the wires' skin effect, resulting in increased power losses [17], [18]. Harmonics cause over-heating, a rise in the audible noise and create conductor vibrations on the load-side. The systems are impacted negatively because of the increased filtering equipment and reduced efficiency. Besides,

harmonics may harm some fragile loads like computers. Also, they interrupt the radio frequencies, which may influence communications networks. Therefore, the harmonics must be handled on both sides of the power converter by including filters [17]. Extra filters make the system bulky and non-economical [104], [105]. The most effective way to manage harmonics is by developing an efficient converter design and control circuits. Therefore, many topologies were developed to handle harmonics in the PE circuit itself [66]. However, any change in the PE circuit is linked to the increasing complexity and susceptibility of the system [104]. Therefore, it is desirable to restrict harmonics in the system with modulation schemes [106].

Diverse PWM strategies were designed for appropriate PE converter design. They can be fabricated employing analog, digital, or hybrid control systems [102], [107]. However, some advanced PWM techniques like space vector PWM (SVPWM) and selective harmonic elimination (SHE-PWM) can only be implemented in digital control systems [56], [93]. The digital control systems were also developed, along with PE converter designs [15], [102], [108]. They deliver benefits, such as eliminating operating point variations due to analog device aging and temperature drift effects, ease of implementing sophisticated algorithms, and control laws to improve power converters' dynamic performance and efficiency. They are also easily reconfigurable and scalable, as compared to analog systems [109], [110].

PWM techniques were developed to provide proper gating signals for the modern PE converters to synthesize a sinusoidal output voltage. However, only

specific techniques like carrier-based PWM (SPWM), SV-PWM, SHE-PWM, and pseudo-modulation techniques can be applied to the multilevel converters [87], [92], [111].

The carrier based PWM method is commonly used to control PE converters. This approach reduces harmonic content and improves output voltage magnitudes [72], [112]. It is well developed for 2-level converters. Traditionally, triangle carrier signals are approximated with a fundamental frequency reference signal. Also, there are other carrier signals (like UN-shape, inverse sinusoidal, and sinusoidal) that have been used [46], [80], [113], [114].

The carrier-based PWM approach is also employed for the multilevel converter. These approaches are known as multi-carrier based PWM techniques. Multiple carrier signals are utilized for the MLC topology to induce gate signals [72], [114]. They can be split into phase-shifted carrier PWM (PSC-PWM) or level-shifted carrier PWM (LSC-PWM) [46], [59]. These PWM schemes operate with high switching frequency carriers. They induce higher-order harmonics, which can be easily filtered by useful passive filters [105]. The PSC-PWM is expanded to the carrier interleaving angle, which enhances the total harmonic distortion (THD) of the output voltage at the cost of a higher ripple and root mean square (RMS) value [72] in medium/high voltage applications and HVDC.

The LSC-PWM is divided into in-phase-disposition (IPD-PWM), phase-opposition disposition (POD-PWM), and alternate POD (APOD-PWM) methods. The IPD-PWM develops an output voltage with the lowest harmonic distortion than the POD-PWM and APOD-PWM schemes [66], [115]–[117]. It generates an

output line-to-line voltage with the most subordinate harmonic distortion while keeping a fixed switching frequency between the switching devices [116], [118].

Furthermore, an optimal IPD-PWM strategy with an interleaving angle is presented in [69], which enhances the output voltage harmonic range and suspends the load sharing between DC sources or split capacitors. Still, the IPD-PWM strategy creates an additional influential ripple in power supplied by the DC sources in CHB-MLC or sub-modules (SM) capacitor voltage in MMC, which raises the magnitude of circulating currents compared with the PSC-PWM scheme [67], [72].

In general, carrier-based PWM methods utilize high switching frequency or even variable switching frequency carriers to reduce lower harmonics components of the output voltage. Thus, they produce higher switching losses but fewer fundamental components in the output voltage. In addition, each CHB is assigned a separate carrier signal, as in IPD-PWM, to make proper output voltage steps while prearranging equal load sharing. Expensive digital hardware is needed to generate many such carriers. For example, HVDC transmission systems need 200–400 SM/arm to get an operative voltage of ± 320 kV (DC) [119]. Moreover, diverse styles of carrier signals have been proposed by various scholars [46], [80], [113], [120].

The SV-PWM can manage a PE converter at a lower switching frequency than the carrier-based PWM, reducing switching losses [84], [121], [122]. The switching pulses can be generated by calculating the vector position in this strategy. Therefore, it can be produced efficiently on the digital controller [82],

[85], [86], [119]. However, extending the number of power cells in CHB-MLC and MMC converters is challenging.

On the other hand, selective harmonic elimination (SHE) and nearest level modulation (NLM) strategies belong to the fundamental switching frequency modulation schemes [93], [98], [111], i.e., they operate at a low switching frequency, ordinarily equal to the line frequency. However, the execution of the SHE method involves the computation of switching times. The number of switching times drastically rises with the number of voltage levels. The switching times are calculated by solving a system of nonlinear equations [92], [97], i.e., using numerical solution techniques and multiple cascaded iteration loops. In other words, there is no closed-form resolution, and achieving the appropriate timing is very sluggish and, particularly with a growing number of switching timings [90], [96], [123], [124], the SHE algorithm cannot be practically realized in real-time where many modules are used. Moreover, its offline execution is restricted. Due to each angle's high precision, floating-point numbers demand higher memory capacity to store in a suitable lookup table at various modulation indexes [99], [101], [125], [126].

In NLM, the harmonic distortion of the output voltage and current waveforms is exceptionally increased [127]. Further, this modulation strategy needs an SM selection process based on the DC source voltage levels to decrease the voltage surges in the source. The SM selection depends on the current direction and voltage level in the SMs [128]. So, the number of sensors increases with the increase in SMs. The additional usage of sensing components

increases the cost and complexity of the converter [129]. Also, a more powerful and expensive digital controller is needed to implement the NLC since it requires a much smaller time-step [130].

Although fundamental frequency modulation schemes (such as SHE and NLM) are essential because of their low switching losses, they need a higher sampling frequency than carrier-based methods to generate an output voltage approximating its reference [111], [131].

3.2.1 Wavelet-based PWM technique

Another PWM technique, called wavelet-based PWM (WPWM), does not require any carrier signal. This WPWM method was first introduced for the 2-level inverter by Drs. S. A. Saleh and M. A. Rahman in 2009 [132]–[135]. In this modulation technique, scale-based linearly combined scaling ($\varphi_{\mathrm{j}}(\mathrm{t})$) and synthesis scaling ($\widetilde{\varphi_j}(t)$) functions are used to generate switching pulses. These equations are explained in equations (3-1) and (3-5), respectively. The scaling function $\varphi(t)$ generates two samples at td1 (equation 3-3) and td2 (equation 3-4), and store them in a group d, where d = 0, 1, 2…D. The synthesis scaling function ($\widetilde{\varphi_j}(t)$) use this pair of samples to create ON and OFF switching pulses [132], [133].

$$\varphi_{\mathrm{j}}(\mathrm{t}) = \emptyset_{\mathrm{H}}\left(2^{\mathrm{j}+1}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(2^{\mathrm{j}+1}\left(\mathrm{t} - 1 + 2^{-(\mathrm{j}+1)}\right)\right) \quad (3\text{-}1)$$

Where: $\emptyset_H$=Harr scaling function

The generalized form of above equation is shown as:

$$\varphi_{j,k}(t) = \varphi_1\left(2^{j+1}t - k\right) \quad (3\text{-}2)$$

$$t_{d1} = d + 2^{-(j+1)} \quad (3\text{-}3)$$

$$t_{d2} = d + 1 - 2^{-(j+1)} \quad (3\text{-}4)$$

Where j=1, 2, 3…

The equation (3-5) represents the synthesis scaling functions, which synthesize the two samples to generate switching pulses.

$$\widetilde{\varphi_j}(t) = \emptyset_H(t) - \varphi_j(t) \quad (3\text{-}5)$$

Where j=1, 2, 3…

$\emptyset_H$=Harr scaling function

The width of the switching pulses has been varied by changing the value j during each dilation. The pulse width has been increased by increasing the value of j and decreased the pulse width by decreasing the value of j. The increasing and decreasing patterns of j have been tracked using scale time interval factor γ, which is calculated using equation (3-6). The value of γ depends on the sign reversal of the first derivative of $S_M(t)$. This method operates a 2-level inverter at 1.8 kHz switching frequency.

$$\gamma_d = \gamma_{d-1} + \frac{S'_M(t_{d2})}{|S'_M(t_{d2})|}\sum_{m=1}^{j} m2^m(t_{m2} - t_{m1}) \quad (3\text{-}6)$$

Where $t_{m1} = dT_\emptyset + 2^{-(m+1)}$

$t_{m2} = (d+1)T_\emptyset - 2^{-(m+1)}$

$T_{\emptyset}$ = Interval of support of the Haar scaling function at $j = 0$

$S_M(t)$ = Sinusoidal reference-modulating signal

$S'_M(t)$ = first derivative of $S_M(t)$

Furthermore, the other researchers also studied the WPWM method for a 2-level converter, which provides a higher fundamental component and low THD in the output signal. Since the method does not require any carrier signal, it is easy to implement on digital computational hardware. This method was further extended (in 2014, 2015) to 1-phase and 3-phase NPC converters which uses the same equations that Drs. Saleh and Rahman proposed with additional logic circuit [136], [137]. However, they increased complexity and generated spurious pulses. Moreover, this method was proposed for a 2-level bidirectional converter which provided similar results as a 2-level converter [138].

Some other researchers also investigated this method for CHB-MLI. One proposed method in 2016 [139], utilized Dr. Saleh and Rahman's equations of H-bridge converter for the single phase CHB-MLC. Therefore, it needed an additional component to generate switching pulses for the CHB-MLC. The pulse generator circuit for the 5-level and 7-level CHB-MLC is shown in Figure 3.1and Figure 3.2, respectively. The additional circuit increases the power losses and made it more complex [139]. This method also created vertically shifted gate pulses (Figure 3.3) which provides unequal conduction time in between each H-bridge module. This method uses a higher switching frequency, which increases switching losses as well [140], [141]. Moreover, both proposed methods need an

additional charge regulator to control charge in all connected sources equally in the system.

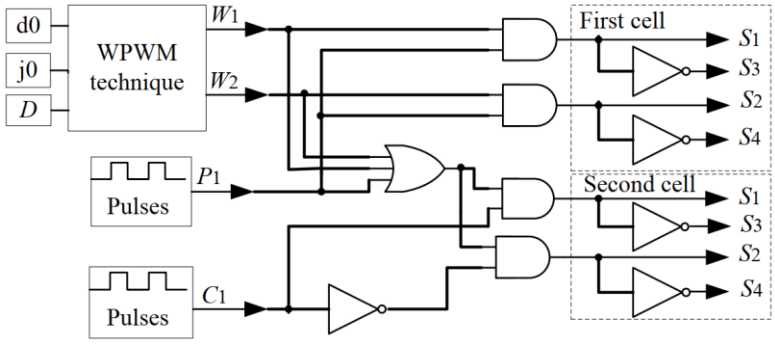


Figure 3.1: Logic control scheme for the switches of 5-level converter with WPWM technique [139]

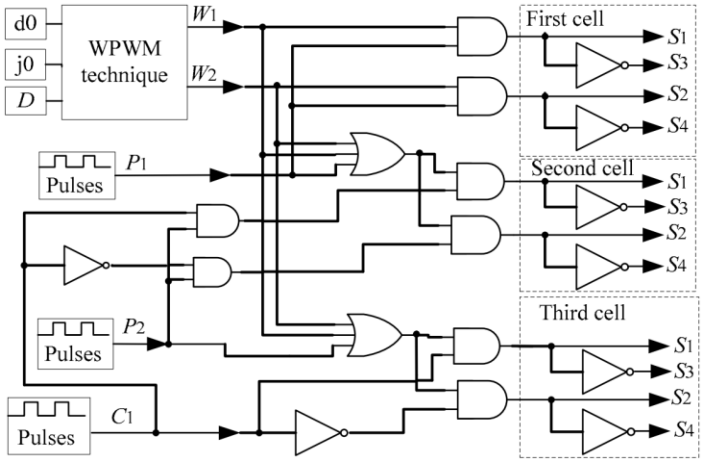


Figure 3.2: Logic control scheme for the switches of 7-level converter with WPWM technique [139]

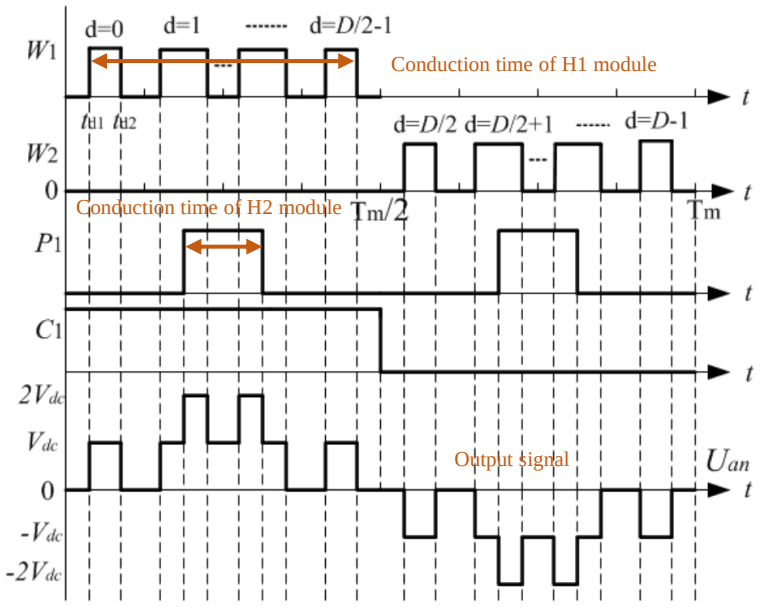


Figure 3.3: WPWM operation principle of five-level inverter [139]

Furthermore, Dr. Saleh implemented this method on CHB-MLI in 2017 [140]. In this research, previously discussed, scale-based linearly combined scaling ($\varphi_{\mathrm{j}}(\mathrm{t})$) and synthesis scaling ($\widetilde{\varphi_j}(t)$) functions are assigned to each H-bridge which are connected in series with each other. The basis functions were updated for each H-bridge to generate switching pulses. For example, 7-level CHB-MLI has 3-modules connected in series which need same number of basis functions. The equation to generate switching pulses for the first modules was $\tilde{\varphi}\left(2^{\mathrm{j}}\mathrm{t}-\mathrm{k}\right)$. This equation was updated by replacing the value of j, which becomes $\tilde{\varphi}\left(2^{(\mathrm{j}+1)}\mathrm{t}-\mathrm{k}\right)$. Similarly, the equation for the third module in 7-level CHB-MLI was $\tilde{\varphi}\left(2^{(\mathrm{j}+2)}\mathrm{t}-\mathrm{k}\right)$. The link between the number of output voltage levels M and the number of sets of wavelet equations $\tilde{\varphi}\left(2^{\mathrm{j}}\mathrm{t}-\mathrm{k}\right)$ is resolution segmentation (σ), can be indicated as:

$$M = 2\sigma + 1; M, \sigma \in Z, and\ \sigma \geq 2 \quad (3\text{-}7)$$

This is the similar equation to calculate number of levels for the symmetrical CHB-MLC. The value of σ represents the number of H-bridge module connected in series. To operate CHB-MLC, each H-bridge require requires a specific range of scales depends on the number of connected modules. The exact ranges of the scale j for σ s can be picked as:

For 2-H bridges: $\sigma = 2;\ j \in \{2, 4, 6, \dots, J\}$

For 3-H bridges: $\sigma = 3;\ j \in \{2, 5, 8, \dots, J\}$

.

.

For σ -H bridges: $\sigma = \sigma;\ j \in \{2, 2 + \sigma, 2 + 2\sigma, \dots, J\}$ (3-8)

The location of each sample which are used to synthase the switching pulses can be calculated as:

$$(\mathrm{t}_{d1})_\sigma = 2^{(\sigma+1)} + \mathrm{d}_\sigma + 2^{-(j+\sigma)} \quad (3\text{-}9)$$

$$(\mathrm{t}_{d2})_\sigma = 2^{(\sigma+1)} + \mathrm{d}_\sigma + 1 - 2^{-(j+\sigma)} \quad (3\text{-}10)$$

Where $d_\sigma = 0, 1, 2, \dots, D_\sigma - 1$, and D_σ is the number of sample groups created by scaling function at σ. In this method, the generated switching pulses are vertically displaced with each other as shown in the figure.

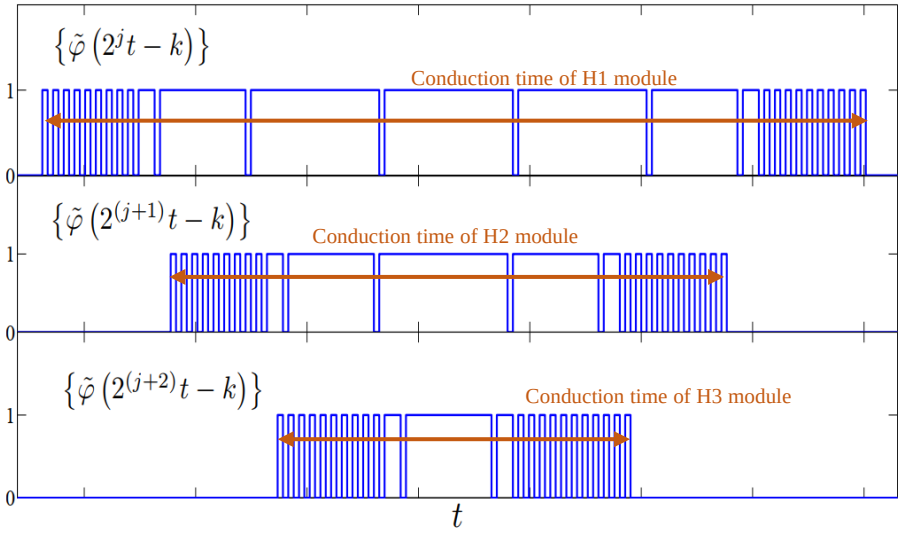


Figure 3.4: Switching pulses generated for the 7-level CHB-MLI using WPWM method [140]

In this method, 52 switching pulses are generated per modulation signal (60 Hz) [140], which triggers high switching loss, that impacts on efficiency of the converter in high voltage applications. In addition, each module has a different conduction time, means unequal conduction losses among the H-bridge modules (PE switches), leading to an uneven semiconductor junction temperature distribution. Therefore, the PE switches with low junction temperature are not fully utilized [54]–[56], which affects the preference of the PE switches in the converter's configuration. Moreover, the equation presented to track increase/decrease the value of j is quite complex, specifically when it is used for the CHB-MLC.

3.3 Summary

This chapter explained how various modulation techniques were implemented to increase the performance of various PE converter topologies. Later in this chapter, previously studied equation of the wavelet-based

modulation techniques was discussed. Afterwards, their limitations and research gap were provided. The next chapter will explain the operation of cascaded H-bridge MLC and the modeling.

Chapter 4. Operation of Cascaded H-bridge MLC and modeling

4.1 Introduction

This chapter explains the operation of 2-level H-bridge converter and cascaded H-bridge multi-level inverter (CHB-MLI). A 2-level H-bridge converter cannot be used for high voltage applications because of the limited voltage blocking capability of semiconductor switches. However, it is employed to build a cascaded H-bridge multi-level inverter (CHB-MLI) topology for the high voltage applications. Later in this chapter, sample based PWM technique is explained with simulation results.

4.2 Operation of a 2-level converter

The standard low voltage (LV) inverter (voltage source inverter (VSI)) is a 1-phase, which produces two-level in the output, which is used for LV applications. A classic configuration of a 1-phase H-bridge (HB) inverter is shown in Figure 2.3. This VSI is effortless to run. A suitable control method can be used with this VSI to generate the 3-level, +v_d, 0, and -v_d signal in the output. There are 4-switches used to form 2-legs of the HB.

The output signal can be generated in modern converters by controlling switching using the multi-pulse PWM concept. As shown in Figure 4.1, the PWM signal can be induced by comparing the reference signal (v_{ref}) with a respective triangle carrier waveform (v_{cr}), which is like the switching frequency. The v_{ref} is a sinusoidal signal at the desired frequency of the sinusoidal output voltage waveform.

An amplitude modulation index can control the converter output voltage's fundamental frequency (60 Hz) component. It can be represented mathematically as equation (4-1),

$$m_a = \frac{\hat{V}_{ref}}{\hat{V}_{cr}} \tag{4-1}$$

The frequency modulation ratio m_f can be represented as equation (4-2).

$$m_f = \frac{f_{cr}}{f_{ref}} \tag{4-2}$$

Where: $\hat{V}_{ref}$ and $\hat{V}_{cr}$ are the peak values of the reference and carrier waves, respectively.

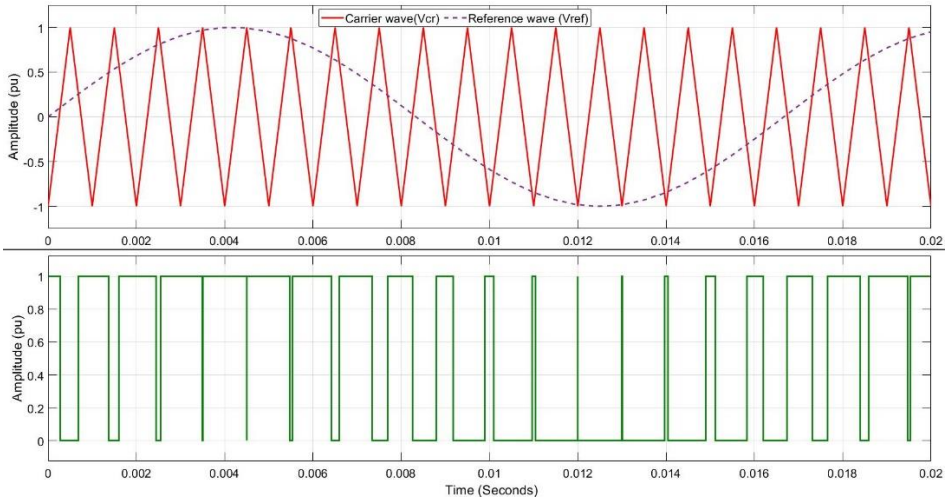


Figure 4.1: Carrier-based sinusoidal PWM technique (upper) and Generated control signal (bottom)

Generally, the amplitude modulation index (m_a) can be adjusted by changing the amplitude of $\hat{V}_{ref}$, while the amplitude of $\hat{V}_{cr}$ is kept constant. The operation switches Q1-Q4 can be controlled by switching pulses generated by comparing the reference wave with the carrier wave in the SPWM technique. In

this OWM concept, when the $v_{ref} > v_{cr}$, the upper switch Q1 and lower switch in the other leg Q4 are turned ON. At the same time, the other two switches, Q2 and Q3, are turned OFF, which generates $+v_d$ output voltage. Similarly, when $v_{ref} < v_{cr}$, the switches Q1 and Q4 are OFF while Q2 and Q3 are ON, and $-v_d$ generates in the output. Commonly, this topology is employed using higher switching frequency signals to handle harmonics efficiently. However, since a higher switching frequency increases losses, this topology is preferred to control with a lower switching frequency when used as a power cell/submodule/unit in CHB-MLC topology. The output voltage is described as equation (4-3).

$$v_o = \frac{4V_{dc}}{\pi}\left(sin(\omega t) + \frac{1}{3}sin(3\omega t) + \frac{1}{5}sin(5\omega t) + \cdots\right) \quad (4\text{-}3)$$

Where: V_{dc} is a DC voltage

The peak of the fundamental element is shown in equation (4-4), and the value of the root mean square (RMS) signal is expressed in equation (4-5).

$$V_{o1\_peak} = \frac{4V_d}{\pi} \approx 1.27V_{dc} \quad (4\text{-}4)$$

$$V_{o1\_rms} = \frac{V_{o1p}}{\sqrt{2}} = \frac{2\sqrt{2}V_d}{\pi} \approx 0.9V_{dc} \quad (4\text{-}5)$$

Where: V_{o1_peak} is the highest value of the produced voltage

V_{o1_rms} is RMS voltage

4.1.1 Operation of a 2-level converter

The applications of HV cannot use 1-phase LV inverters due to the limited voltage blocking ability of semiconductor switches. Therefore, the CHB-MLI

topology is employed for these types of applications. Figure 4.2 illustrates the 3-phase CHB-MLI. This configuration uses several HB modules/cells connected in series to produce an enhanced AC output voltage with lower harmonic contents. The most important thing is that this design needs an isolated DC supply to feed each H-bridge power cell. These DC supplies can be obtained from batteries, PV arrays, and diode rectifiers.

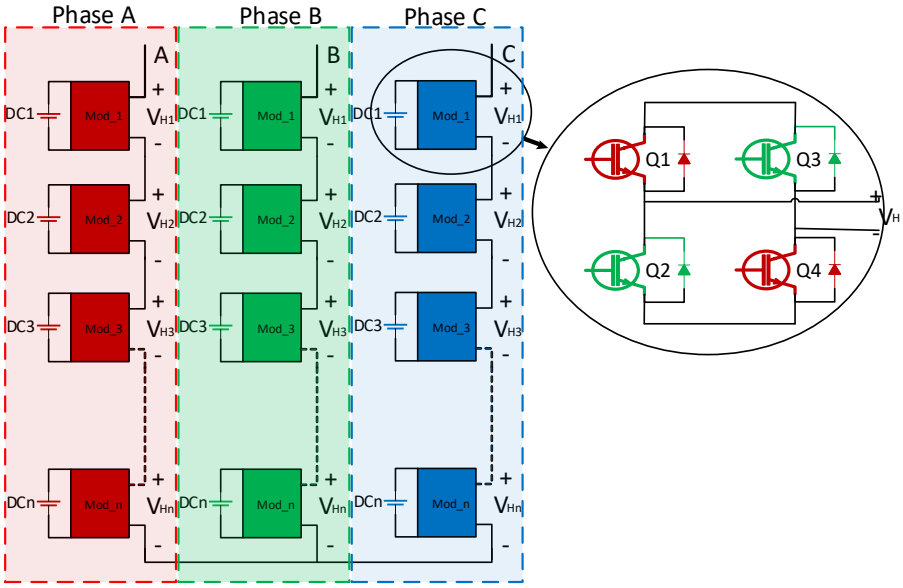


Figure 4.2: 3-phase CHB-MLI

There are two ways to implement the symmetrical or asymmetrical CHB-MLI configurations based on the DC source configuration.

4.1.1.1 Symmetrical type CHB-MLC

The symmetrical design of CHB-MLI uses multiple isolated DC sources with identical amplitudes. Similarly, as shown in the Figure 4.3, a CHB-MLI with 3-series connected cells uses isolated DC input sources of the same amplitudes to produce a 7-level output signal. These 7-levels are measured as *0, ±E, ±2E,*

and ±3E. The following equation is used to decide the number of levels in this configuration:

$$M = (2H + 1) \tag{4-6}$$

where “M” and “H” are the number of output levels and the number of H-bridge power cells per phase leg, respectively. Also, the “M” is always an odd number.

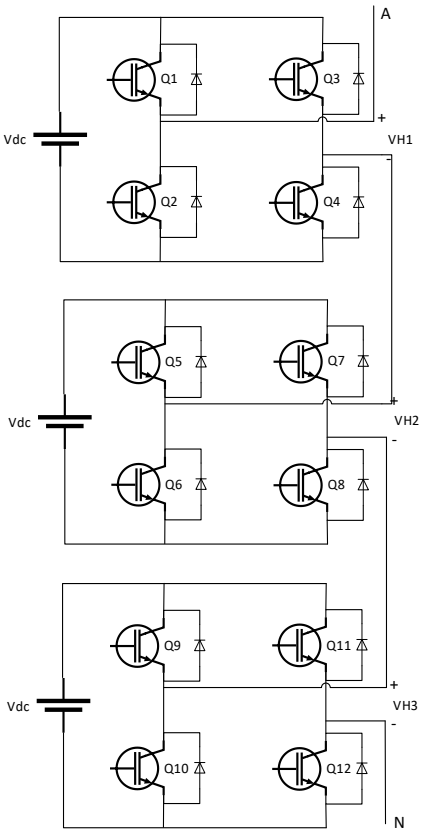


Figure 4.3: Single-phase 7-level symmetrical type CHB-MLI

The various switching conditions can produce some voltage levels, a familiar trend in multi-level converters, increasing the switching pattern design alternatives for better operation. The symmetrical type CHB-MLI configuration

with two power units can produce a 5-level phase voltage in the output signal. In this configuration, each switching condition and developed voltage level are in Table 4.1.

Table 4.1: Switching condition for symmetrical type CHB-MLI

Switching condition				Output voltage		
				v_{H1}	v_{H2}	v_{phase}
0	1	0	1	$-v_{dc}$	$-v_{dc}$	$-2v_{dc}$
0	1	1	1	$-v_{dc}$	0	$-v_{dc}$
0	1	0	0	$-v_{dc}$	0	
1	1	0	1	0	$-v_{dc}$	
0	0	0	1	0	$-v_{dc}$	
0	0	0	0	0	0	0
0	0	1	1	0	0	
1	1	0	0	0	0	
1	1	1	1	0	0	
1	0	0	1	$+v_{dc}$	$-v_{dc}$	
0	1	1	0	$-v_{dc}$	$+v_{dc}$	
1	0	1	1	$+v_{dc}$	0	$+v_{dc}$
1	0	0	0	$+v_{dc}$	0	
1	1	1	0	0	$+v_{dc}$	
1	0	1	0	0	$+v_{dc}$	
1	0	1	0	$+v_{dc}$	$+v_{dc}$	$+2v_{dc}$

4.1.1.2 Asymmetrical type CHB-MLC

The asymmetrical type CHB-MLI uses various scale isolated DC sources as shown in Figure 4.4. Each cell produces three different voltage levels in this sort of structure. Therefore, the highest voltage levels depend on the DC sources' peak value. There are binary and trinary systems to think of DC levels in a CHB-

MLI. In the binary method, it uses V_{dc1} = E, V_{dc2} = 2E, and V_{dc3} = 4E. This sequence of input amplitudes of voltages results in 15 levels in the phase-voltage of CHB-MLI. Equation (4-3) denotes the output voltage-level in this design.

$$M = (2^{H+1} - 1) \tag{4-7}$$

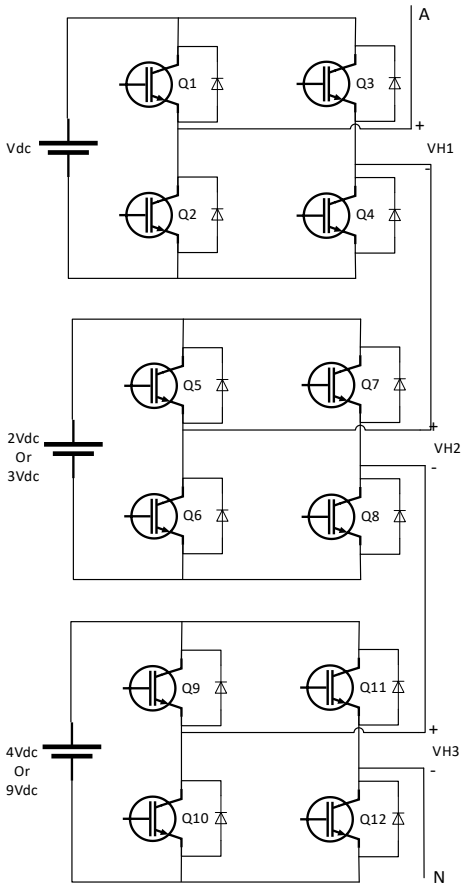


Figure 4.4: Single-phase asymmetrical type CHB-MLI

Table 4.2: Switching condition for asymmetrical type CHB-MLI

Switching Condition				Output voltage		
				v_{H1}	v_{H2}	v_{phase}
0	1	0	1	$-v_{dc}$	$-2v_{dc}$	$-3v_{dc}$
0	0	0	1	0	$-2v_{dc}$	$-2v_{dc}$
1	1	0	1	0	$-2v_{dc}$	
0	1	0	0	$-v_{dc}$	0	$-v_{dc}$
0	1	1	1	$-v_{dc}$	0	
1	0	0	1	$+v_{dc}$	$-2v_{dc}$	
1	1	1	1	0	0	0
1	1	0	0	0	0	
0	0	1	1	0	0	
0	0	0	0	0	0	
0	1	1	0	$-v_{dc}$	$+2v_{dc}$	$+v_{dc}$
1	0	0	0	$+v_{dc}$	0	
1	0	1	1	$+v_{dc}$	0	
0	0	1	0	0	$+2v_{dc}$	$+2v_{dc}$
1	1	1	0	0	$+2v_{dc}$	
1	0	1	0	$+v_{dc}$	$+2v_{dc}$	$+3v_{dc}$

In trinary method, all input sources are set as: V_{dc1} = E, V_{dc2} = 3E, and V_{dc3} = 9E. This configuration produces voltages with 27-levels in the output phase signal. Equation (4-8) expresses the upper limit of output signal levels.

$$M = 3^H \tag{4-8}$$

The asymmetrical type CHB-MLI configuration with two power units can produce the output signal's 7-level or 9-level phase voltage. The 7-level asymmetrical type configuration with two power cells has input sources of $V_{dc1} = E$, $V_{dc2} = 2E$; it can generate different voltage levels in each switching state described in Table 4.2.

The modular structure of CHB-MLI collapsed. The asymmetrical type CHB-MLI uses lesser switches than the symmetrical type CHB-MLI. However, it has some disadvantages because of the unequal input DC voltages. Moreover, switching pattern designing for this topology is much more complex than symmetrical type CHB-MLI because of the reduced redundant switching conditions. Therefore, this topology can be suitable for limited industrial applications.

4.3 Mathematical analysis

In a CHB-MLI, the voltage difference of PE switches is each cell's output voltage. Then, two individual switching functions control each cell and equation (4-9) sets the voltage level in each cell $V_{o\_cell_i}$ as:

$$V_{o\_cell_i} = V_{dc}(Q_{1_{cell_i}} - Q_{3_{cell_i}}) \quad (4\text{-}9)$$

Where switching functions are $Q_{1_{cell_i}}$ and $Q_{3_{cell_i}}$, and V_{dc} is a DC input of each HB. A switching function, Q_i is defined as equation (4-10), where i =1, 2, ⋯, n..

$$Q_i = \begin{cases} 1; when\ Q_i\ is\ ON \\ 0; when\ Q_i\ is\ OFF \end{cases} \quad (4\text{-}10)$$

The overall output voltage of a CHB-MLI is produced as shown in equation (4-11) for the symmetric structure, and equation (4-12) for the asymmetric configuration.

$$V_o = V_{dc} \sum_{i=1}^{n} (Q_{1_{cell_i}} - Q_{3_{cell_i}}) \quad (4\text{-}11)$$

$$V_o = \sum_{i=1}^{n} (Q_{1_{cell_i}} - Q_{3_{cell_i}})\, V_{dc_i} \quad (4\text{-}12)$$

Thus, equation (4-13) shows the 7-level symmetric CHB-MLI's output voltage.

$$\begin{cases} V_{o1} = V_{dc}(Q_{1_{cell_1}} - Q_{3_{cell_1}}) \\ V_{o2} = V_{dc}(Q_{1_{cell_2}} - Q_{3_{cell_2}}) \\ V_{o3} = V_{dc}(Q_{1_{cell_3}} - Q_{3_{cell_3}}) \end{cases} \quad (4\text{-}13)$$

Similarly, equation (4-14) illustrates the output voltage of 15- and 27-level asymmetric CHB-MLIs.

$$\begin{cases} V_{o1} = V_{dc_1}(Q_{1_{cell_1}} - Q_{3_{cell_1}}) \\ V_{o2} = V_{dc_2}(Q_{1_{cell_2}} - Q_{3_{cell_2}}) \\ V_{o3} = V_{dc_3}(Q_{1_{cell_3}} - Q_{3_{cell_3}}) \end{cases} \quad (4\text{-}14)$$

4.4 Sampling-based modeling of MC-PWM technique

The AC signal is a continuous-time (CT) signal in power systems. However, a digital control system needs discrete-time signals to enforce a control algorithm for the PE converter. Therefore, an analog-to-digital (A/D) converter must convert the analog input signal into a digital signal. The sampling methodology does the conversion of the A/D signal. A pulse sequence is formed at a discrete-time interval from the analog signal in this process. Conversely, the controller output is a discrete-time signal, and most real-time applications require CT signals; consequently, a digital-to-analog (D/A) converter is needed.

The A/D conversion can be correlated to the most frequently used MC-PWM method for CHB-MLC. In this method, multiple high-frequency carrier signals (usually, triangle signals) and the fundamental frequency reference signal (usually, sinusoidal signals) are CT signals. These carrier signals are compared

with the reference signal to generate switching pulses for the PE switches. The spectrum of the multi-switching signal shows specific harmonics forming sidebands around multiples of the carrier signal (e.g., $4m_f \pm 1$, $4m_f \pm 5$…). These frequency sidebands are formed when a band-limited signal is broken down into samples with a sampling frequency at the center of these frequency groups. The phase voltage and harmonics for the 5-level CHB-MLI are shown in Figure 4.5.

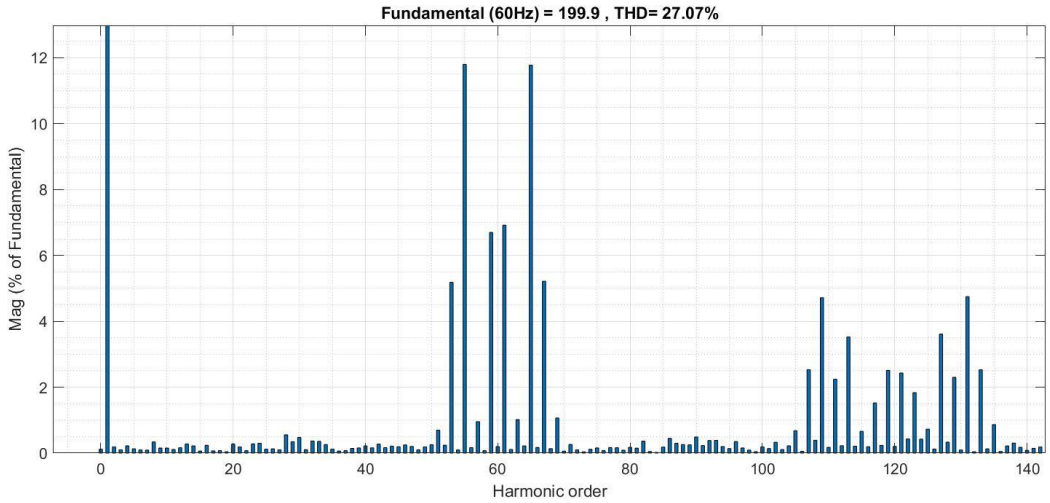


Figure 4.5: The spectrum of the multi-switching signal

The carrier-based PWM is shown in Figure 4.6. This method produces a control pulse when the amplitude of the carrier signal is less than the reference signal's amplitude. As shown in Figure 4.6(bottom) unit impulse signals are formed at each reference and carrier signals cross-over point. Each impulse signal can be defined. These impulse signals are not generated at equally spaced intervals. Therefore, they can be noticed as non-uniform samples of the reference signal. Every single triangle pulse generates two samples, first when it

is rising up and second when it is falling down. Therefore, the samples are at twice the sampling frequency (f_s). Even the spacings between these samples divide in a recurring type for each half cycle (positive and negative cycles) of the reference signal. The good quality converter output signal must be as near as attainable to the reference signal, which can be interpreted as the entire switching pattern (pulsating output signal) as a restoration strategy of the reference signal with higher amplitude.

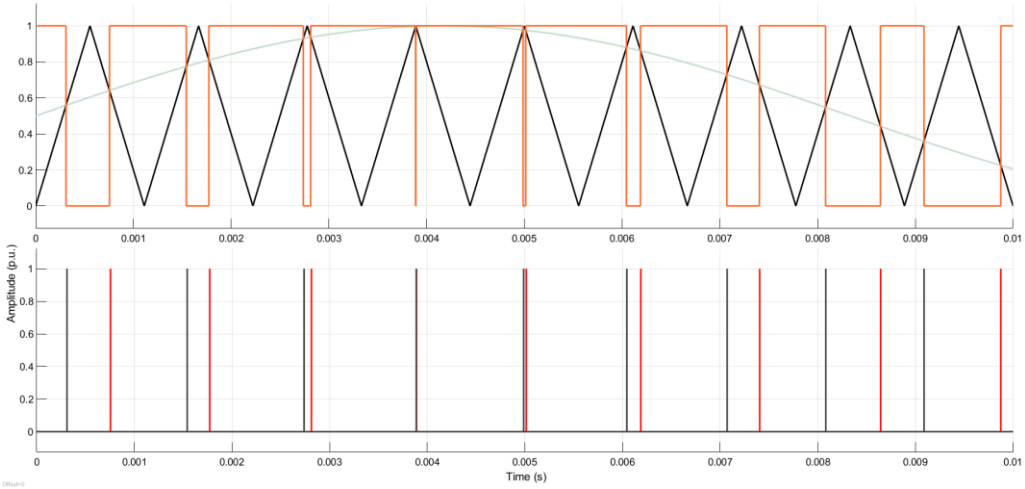


Figure 4.6: Multi-switching PWM technique (upper), unit impulse signals (bottom)

The entire reference signal for the MC-based PS-PWM approach is given as a block diagram in Figure 4.7. For power unit 1, the $x_{ref_1}(t)$ is a sinusoidal reference (CT) signal, and Cr_1 is a triangular carrier signal. These carrier signals create two samples per rotation. One sample ($Cr_{1_{rise}}[n]$) was formed at the junction point of the rising place of the triangular signal and reference signal $x_{ref_1}(t)$. Likewise, the other one, $Cr_{1_{fall}}[n]$, formed at the junction point of the falling place of the triangular signal and reference signal. The generated discrete

signal ($x_{1_{data}}[n]$) is sampled data for power unit 1. An identical methodology applies to the reference signal for the N number of units with the various phase-shifted carrier signals. Generalized variables $x_{ref_i}(t)$, $Cr_{i_{rise}}[n]$, $Cr_{i_{fall}}[n]$, and ($x_{1_{data}}[n]$) express reference signal, rising edge carrier signal, falling edge carrier signal, and discrete signal, respectively, for the N number; of units, where i = 1, 2, 3, …

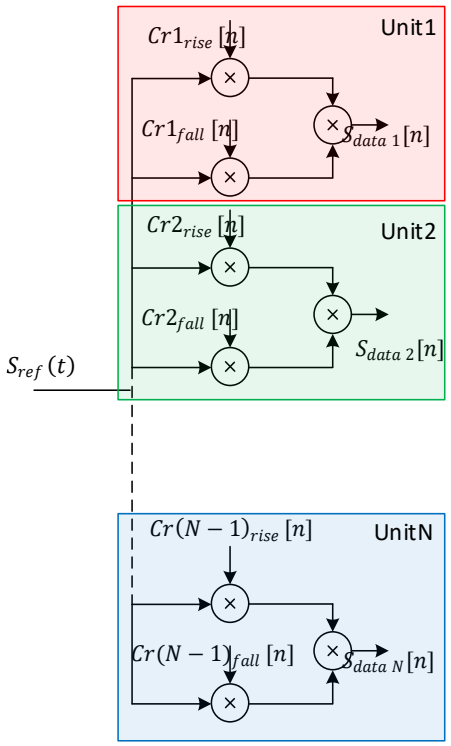


Figure 4.7: Block diagram of sampling of a reference signal for the MC-based PS-PWM technique

The non-uniform samples have a periodic pattern because of the reference signal's cyclicity and stability. This characteristic of sampling is known as successive non-uniform sampling. The samples are separated into K number

of samples in each group for the individual power unit. These sample groups have a steady period of T_p, which can be expressed as:

$$T_p = KT_Q \tag{4-23}$$

Where T_Q is the Nyquist period. Also, $T_Q \leq \frac{T_m}{2}$ and $T_m = \frac{1}{f_m}$. Each sample group has a subsequent sampling time $\{t_s\}, s = 0, 1, 2 \ldots., (\mathrm{N}-1)$. The sampling time for one period of the persistent samples are described by:

$$\{t_s\} + nT_p, 0, 1, 2 \ldots., (\mathrm{N}-1), \mathrm{n} \in (-\infty, \infty) \tag{4-24}$$

The sampled signal can be reconstructed from the samples by interpolation or filtering to form switching pulses for the PE switches.

4.5 Reconstruction of switching pulses using interpolation

Interpolation is a technique for finding unknown or misplaced samples of a signal using a weighted average number of known samples from the nearest points. The number of unknown or misplaced points depends on the digital controller's time step (t_s). In the SPWM technique, the intersection of the sinusoidal signal and the falling/rising edge of the carrier signal creates two samples. Consider that the amplitude of these two samples is 1.0 p.u. Also, in between these two samples, the value of some unknown points may need to be evaluated using the interpolation technique to re-construct the exact switching pulse of the converter. The process of sampling a reference signal and reconstruction of switching pulses for the MC-based PS-PWM technique is presented in Figure 4.9.

The Lagrange interpolation is one of the diverse interpolation functions evaluated. In this approach, if the line interpolator passes through two points, $x(t_0)$ and $x(t_1)$:

$$\hat{x}(t) = p_1(t) = x(t_0) + \frac{x(t_1)-x(t_0)}{t_1-t_0}(t - t_0) \quad (4\text{-}25)$$

The above equation can be expressed in the form of a Lagrange polynomial as:

$$p_1(t) = \frac{t-t_1}{t_0-t_1}x(t_0) + \frac{t-t_0}{t_1-t_0}x(t_1) \quad (4\text{-}26)$$

The above equation is the Lagrange formation of a line interpolator of the weighted blend of two lines, as shown in Figure 4.8.

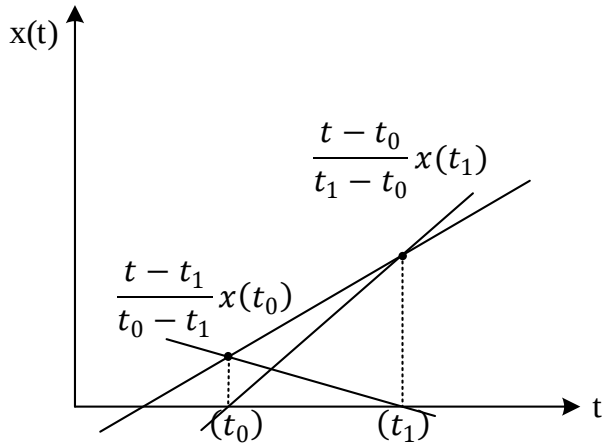


Figure 4.8: Lagrange form of a line interpolator

In general, the Lagrange polynomial, of order N, passing through N+1 samples $\{x(t_0), x(t_1), \ldots x(t_N)\}$ is given by the polynomial equation as:

$$P_N(t) = L_0x(t_0) + L_1x(t_1) + \cdots + L_Nx(t_N) \quad (4\text{-}27)$$

where each Lagrange coefficient $L_{\mathrm{N}}(t)$ is itself a polynomial of degree N, which is written as:

$$L_{\mathrm{i}}(t) = \frac{(t-t_0)\ldots(t-t_{i-1})(t-t_{i+1})\ldots(t-t_N)}{(t_i-t_0)\ldots(t_i-t_{i-1})(t_i-t_{i+1})\ldots(t_i-t_N)} = \prod_{\substack{n=0 \\ n\neq i}}^{N} \frac{t-t_n}{t_i-t_n} \tag{4-28}$$

The $P_N(t_i) = L_i(t_i)x(t_i)$ since Lagrange polynomial coefficient $L_{\mathrm{i}}(t)$ becomes unity at the i^{th} known sampling point and zero at every new known sample point.

The general form of Lagrange's interpolation polynomial can be written as:

$$P_N(t) = \sum_{i=0}^{N} x_i L_i(t) = \sum_{i=1}^{N} x_i \left(\prod_{\substack{n=0 \\ n\neq i}}^{N} \frac{t-t_n}{t_i-t_n} \right) \tag{4-29}$$

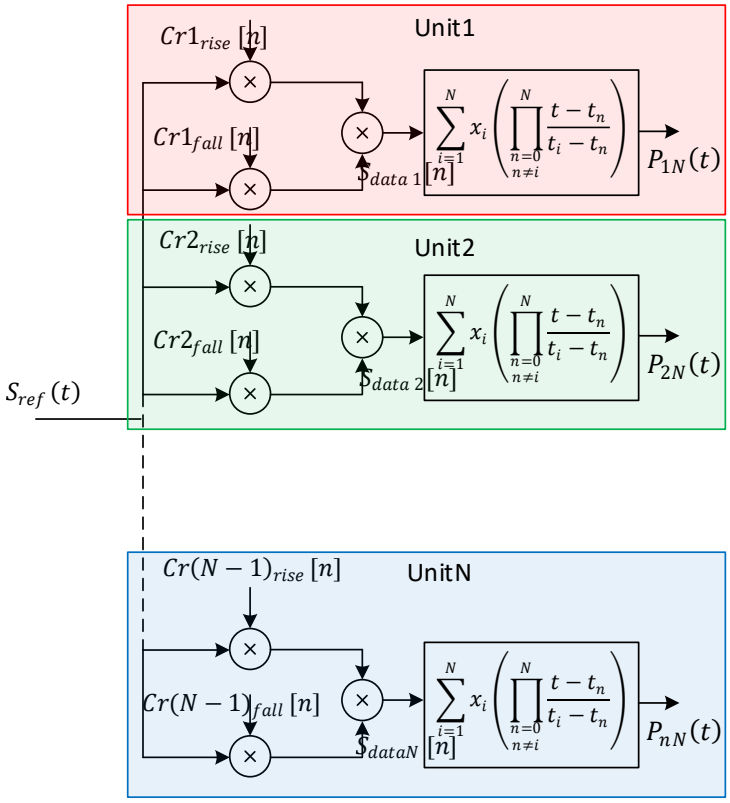


Figure 4.9: Block diagram of sampling and reconstruction of switching pulses

The interpolating function $P_N(t)$ is implemented for a pair of samples, showing the changes from OFF to ON to OFF for the PE switches. Figure 4.10 indicates that the pulse generated using the interpolating function is almost identical to the switching action (square pulse) suitable for the PE switch.

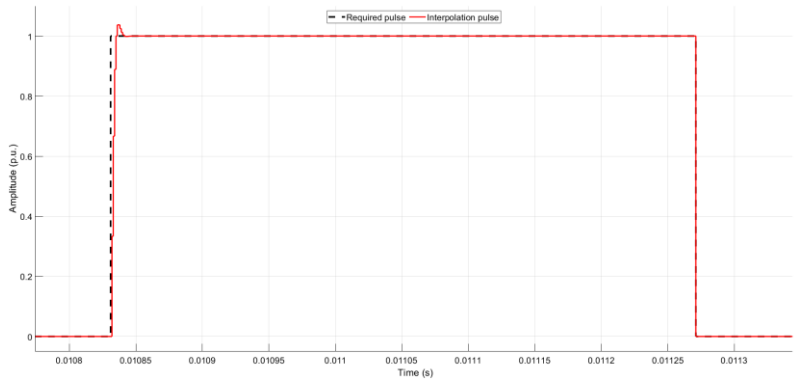


Figure 4.10: Switching pulse generated with traditional and interpolation methods.

4.6 Validation of the MC-PWM model

The mathematical model of the MC-PWM technique can be validated by comparing it to the standard MC-based PS-PWM strategy for the 5-level CHB-MLI.

4.3.1 Switching pulses

The MC-based PS-PWM strategy manages the switching action so that the required output voltage can be reproduced. A similar mathematical model can be made using the interpolation process's sampling and reconstruction of the pulses. Figure 4.11 and Figure 4.12 show the classic PS-PWM switching pulses and pulses produced by the interpolation methodology for each leg in both power units, respectively. The pulses generated using the interpolation method have a

higher amplitude at the rising edge than the definitive pulses. Therefore, each approach was applied to the 5-level CHB-MLI to verify the output signals shown in Figure 4.13. The 5-level output signal has equal positive and negative pulses for both techniques, generating almost identical output signal amplitude. Also, discharge currents for both units are naturally balanced, which can be shown in Figure 4.14.

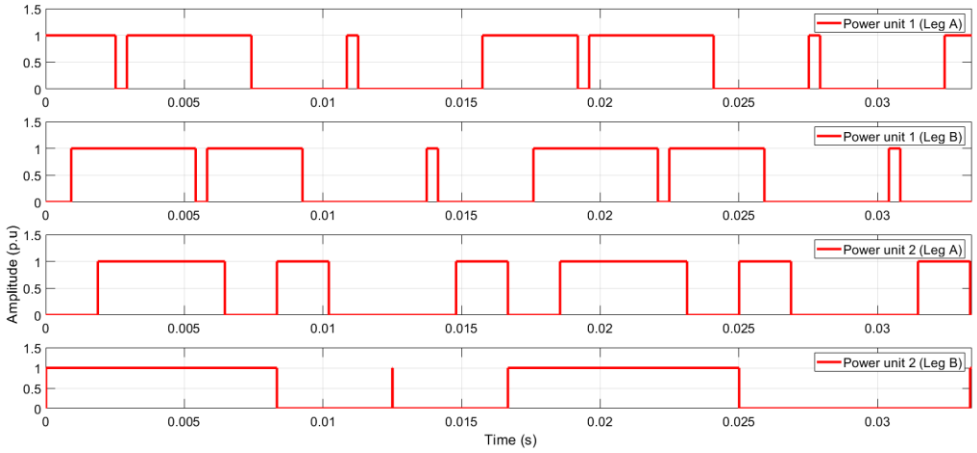


Figure 4.11: Switching pulses generated with traditional PS-PWM method for 5-level CHB-MLC

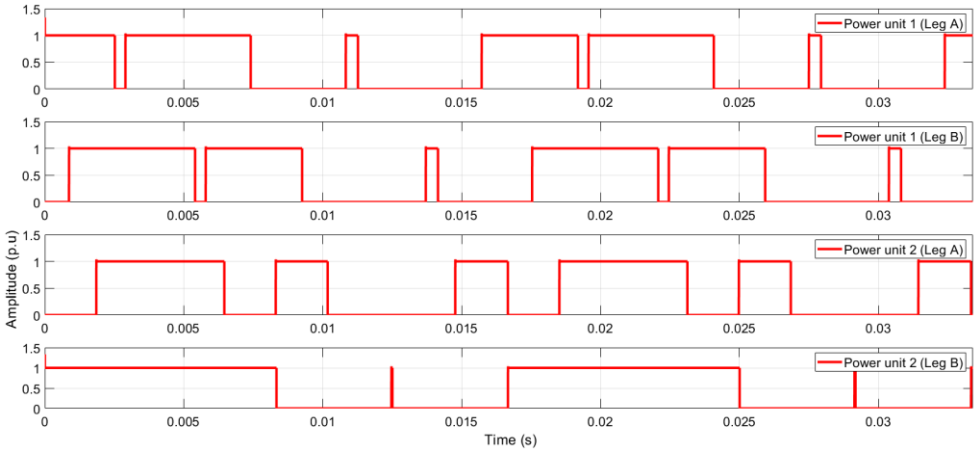


Figure 4.12: Switching pulses generated using interpolation method for 5-level CHB-MLC

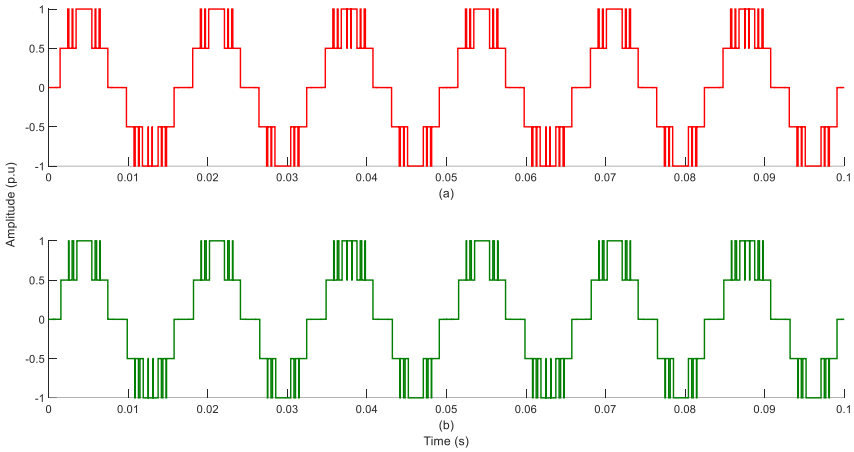


Figure 4.13: Output voltage of 5-level CHB-MLC using (a) PS-PWM and (b) interpolation method

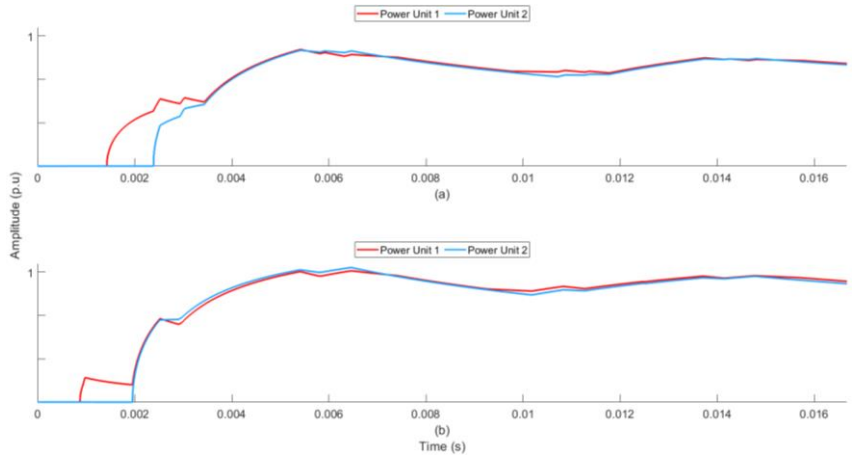


Figure 4.14: Discharging current of each power unit in 5-level CHB-MLC using (a) PS-PWM method (b) Interpolation method.

Moreover, both procedures were studied using Fourier analysis, and its resultant spectrum is shown in Figure 4.15. Both methods inject a comparable number of harmonics in the line as they have THD of 32.15% and 32.48% for PS-PWM and interpolation pulses, respectively.

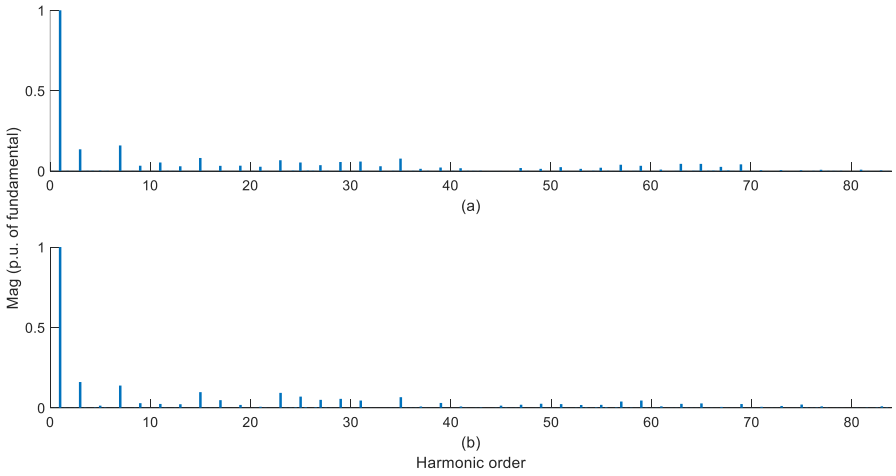


Figure 4.15: Harmonics in the output signal for (a) PS-PWM and (b) interpolation method

4.7 Summary

This chapter explained the operation of 2-level H-bridge CHB-MLI. Also, symmetrical, and asymmetrical configuration of CHB-MLI are discussed. After that, a sample-based model of the MC-PWM technique was discussed. In this modeling, non-uniform samples were created like the pulses generated by the traditional SPWM method. Using Lagrange's polynomial method, the two closest samples are considered to re-construct the switching pulses. In the end, simulation results were analyzed for a 5-level single-phase CHB-MLI.

Chapter 5. Wavelet-based modulation technique for CHB-MLI

5.1 Introduction

This chapter introduces modulation technique with give emphasis to wavelet-based sampling theorem. Furthermore, this chapter clarifies the analytical process of developing the proposed modified wavelet-based modulation technique for CHB-MLC. Also, this chapter compares the presented modified wavelet-based modulation strategy to the other developed wavelet-based methods.

5.2 Modulation techniques for inverter

The square-wave modulation technique is simple and generates an excellent fundamental frequency component in the output. The modulation techniques ensures that the inverter generates the fundamental component as close to a preferred sinusoidal wave as possible. In this modulation type, the switching frequency is identical to the line frequency Hence, the switching loss is significantly low. However, the magnitude of the output signal is uncontrolled. This issue was addressed with a single-pulse-width modulation technique. Like a square wave, this method has a single pulse per cycle. Though, the width of the pulse can be varied to control the average magnitude of the output signal. Because of a single pulse per cycle, both methods have an elevated level of harmonic distortion in the output.

The magnitude and harmonic distortion can be simultaneously controlled by generating multiple pulses in the output signal using the multiple-pulse-width modulation approach. The multiple pulses per cycle can be formed with the

SPWM procedure in which each next pulse has a distinct width. Usually, these switching pulses can be generated by comparing a sinusoidal waveform (continuous-time signal (CT)) with the high-frequency triangular signals. This strategy is implemented using a digital control system in modern PE converters. The execution is more challenging since many carrier signals are a necessity.

By way of explanation, in the square-wave strategy, the pulses' width is varied while keeping the equivalent number of pulses constant per cycle to enhance the input (DC bus) utilization. Therefore, the fundamental component increases. Besides, this new modulation strategy is a mathematical-based PWM method that provides a closed-form solution. Hence, it is easy to implement using digital controllers for CHB-MLI. Moreover, this modulation scheme balances all isolated input sources instinctively, which further reduces the compilation load on the controller.

5.3 Wavelet-based sampling theorem

Various wavelet basis functions were used to process signals with complicated time-frequency appearances. These wavelets were employed to process signals and images. Many wavelets can create dyadic-type MRAs (multi-resolution analysis). This type of MRA is beneficial for even sampling and reconstruction of signals. However, this type of wavelets can not be used for the PE converters where variable switching pulses are necessary for the efficient converter's performance. Hence, a specific class of MRA is needed, which can sustain non-uniform sampling and reconstruction procedures of the signal. This section provides details on how to sample a signal using wavelet basis functions.

When a continuous-time (CT) signal, $x_c(t)$ needs to be studied using wavelet functions, it uses a cluster of two wavelet basis functions, namely scaling functions, and wavelet functions. Consider a Haar scaling function $\phi(t)$ to perceive the connection between these two operations. The mathematical form of the Harr scaling function is represented as equation (5-1), and the graphical representation is shown in Figure 5.1.

$$\phi(t) = \begin{cases} 1, & 0 \le t \le 1 \\ 0, & elsewhere \end{cases} \tag{5-1}$$

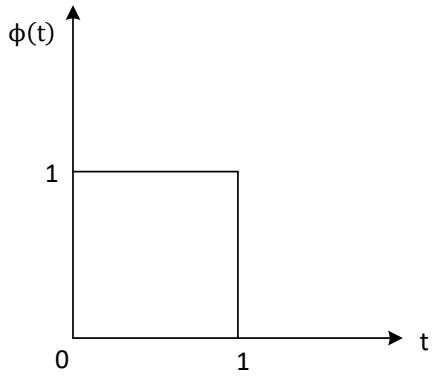


Figure 5.1: Haar scaling function.

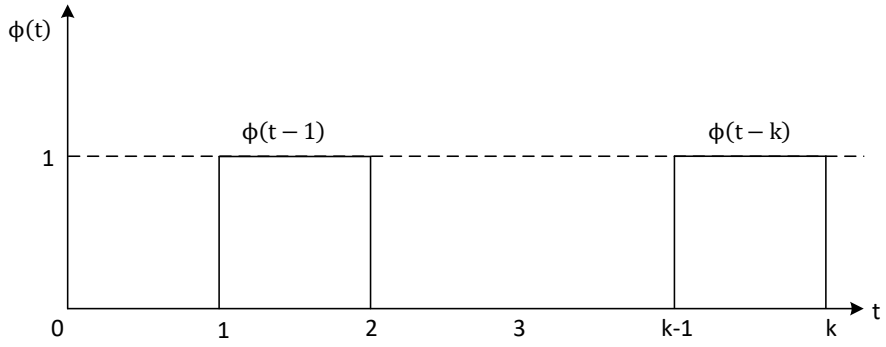


Figure 5.2: Translation of Haar scaling function.

Typically, any scaling function can generate basis functions that span a set of closed space $\{V_n\}$ where $n \in \mathbb{Z}$. This function can restate as $\phi(t-1)$, $\phi(t-2)$…etc. It has a generalized form, $\phi(t-k)$. The translation of this function over time is displayed in Figure 5.2, which is a time-limited function and has finite energy, $\int_{-\infty}^{\infty} |f(t)|^2\, dt$. Moreover, the density and completeness conditions require an orthogonal complement space W_n for each V_n. Each orthogonal complement space W_n is spanned by another set of basis functions generated by $\phi_n(t)$. Such a set of basis functions defines a wavelet function $\Psi(t)$ associated with $\phi(t)$.

Mathematically, the Haar wavelet function can be defined as:

$$\phi(t) = \begin{cases} 1, & 0 \le t \le 1/2 \\ -1, & 1/2 \le t \le 1 \\ 0, & \text{elsewhere} \end{cases} \qquad (5\text{-}2)$$

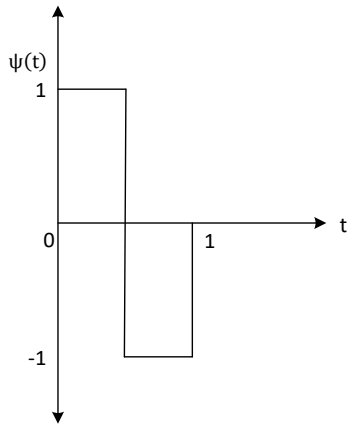


Figure 5.3: Haar wavelet function

Not just Harr wavelets, but any wavelet basis functions needed to span each W_j can be developed per scale j by integer translations of the wavelet function $\psi(t)$, which are known as wavelet basis functions shown in equation (5-3).

$$\psi_{j,k} = 2^{\frac{j}{2}}\psi(2^j t - k) \tag{5-3}$$

Each space V_n and W_n can be expressed as a linear span of wavelet basis functions as equations (5-4) & (5-5).

$$W_j = \underset{k}{\text{span}}\{\psi_{j,k}\} \tag{5-4}$$

$$V_j = \underset{k}{\text{span}}\{\phi_{j,k}\} \tag{5-5}$$

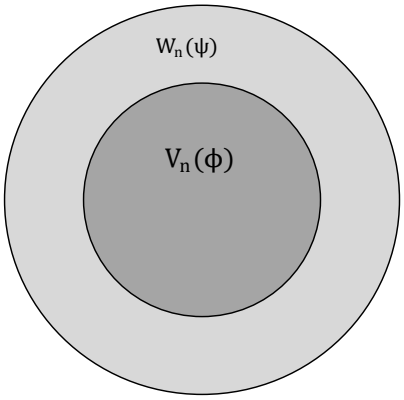


Figure 5.4: Spaces covered by scaling and wavelet function.

It is noted that wavelet and scaling spaces must be dense and complete in $L^2(\mathbb{R})$. A grouping of scaling spaces $V_n(\phi)$ and wavelet spaces $W_n(\psi)$ forms an MRA (Figure 5.4). The density and totality of both spaces can be used to associate them with MRA as the scale *j* transformations, which can be translated into making scaling space $V_q(\phi)$ as equation (5-6).

$$V_q(\phi) = V_{q-1}(\phi) \oplus V_{q-1}(\psi) \tag{5-6}$$

Where, $\oplus$ is the orthogonal operand.

If a CT signal $x_c(t)$ is contained in a space V_q, it can be created using basis functions developed at scale q as equation (5-7).

$$x_c(t) = \sum_{k\epsilon\mathbb{Z}} (c_\phi)_k \phi(t-k) + \sum_{j=0}^{q} \sum_{k\epsilon\mathbb{Z}} (c_\psi)_{k,j} \psi_j(t-k) \tag{5-7}$$

Where coefficients $(c_\phi)_k$ and $(c_\psi)_{k,j}$ denote projecting the signal on scaling and wavelet spaces and are described as equations (5-8) and (5-9).

$$(c_\phi)_k = < x_c(t), \tilde{\phi}(t-k) > \tag{5-8}$$

$$(c_\psi)_{k,j} = < x_c(t), \widetilde{\psi_j}(t-k) > \tag{5-9}$$

$\tilde{\phi}(t)$ is the dual scaling function, and $\widetilde{\psi_j}(t)$ is the dual wavelet function.

Thus, this generalized form is used to expand a signal $x_c(t)$ in terms of a wavelet-based MRA, as shown in equation (5-10).

$$x_c(t) = \sum_{j=0}^{q-1} \sum_{k\epsilon\mathbb{Z}} < x_c(t), \tilde{\phi}(t-k) > \phi(t-k) \tag{5-10}$$

The representation $< x_c(t), \tilde{\phi}(t-k) >$ defines a generalized sampling of the CT signal $x_c(t)$. The set of basis functions $\{\phi(t-k)\}_{k\epsilon\mathbb{Z}}$ spans an approximation space per scale j.

5.4 Concept of building non-dyadic-type MRA

As said earlier, wavelet basis functions and their corresponding transforms are valuable and efficient instruments for describing signals with irregular and varying qualities. That is accomplished by employing groups of synthesis basis functions which can be generalized in the following equation:

$$x(t) = \sum_k \sum_j \langle x(t), \Psi_{j,k}(t) \rangle \widetilde{\Psi}_{j,k}(t) \quad (5\text{-}11)$$

Where, $\Psi_{j,k}(t) = \psi(2^j t - k)$: analysis wavelet function

$\widetilde{\Psi}_{j,k}(t) = \widetilde{\psi}(2^j t - k)$: synthesis wavelet function

$x(t)$: CT signal to be analyzed

Where j stands for the scaling parameter and k stands for the shifting parameter— $j, k \in Z$, where Z is the set of integer numbers.

The analysis and synthesis of waveform using wavelet-basis functions is defined in the MRA. The basic idea of creating an MRA is to specify a scale j such that groups of basis functions can span a grouping of entire and dense spaces. Two spaces are spanned per scale j by a group of a scaling function $V_j(\phi)$ and one set of a wavelet function $W_j(\Psi)$:

$$MRA(j) = V_j(\phi) \oplus W_j(\Psi) \quad (5\text{-}12)$$

Where, $\oplus$ is the orthogonal operand

This MRA can be utilized to extend a signal $f(x)$ with packs of basis functions up to scale j , as equation (5-13):

$$f(x) = \sum_k \sum_j \langle x(t),\ \emptyset_{j,k}(t) \rangle \tilde{\emptyset}_{j,k}(t) + \sum_k \sum_j \langle x(t),\ \Psi_{j,k}(t) \rangle \tilde{\Psi}_{j,k}(t) \qquad (5\text{-}13)$$

The qualities of an MRA depend on the scaling function, where different wavelet basis functions can create dyadic type MRAs. These dyadic MRAs can sustain invariant sample reconstruction beats. In power converters, uneven sampling is needed, as shown in Figure 5.5, for a sinusoidal reference signal. Uniform sampling in a PE converter is redundant and avoided so that it may suffer from execution difficulties, such as increased output harmonics and/or imperfect regulation. As a result, new MRA forms are needed to support the nonuniform sampling reconstruction technique that retains nonuniform recurrent sampling (i.e., sampling of sinusoidal signal to generate valid gating signal for PE switches, as shown in Figure 5.5).

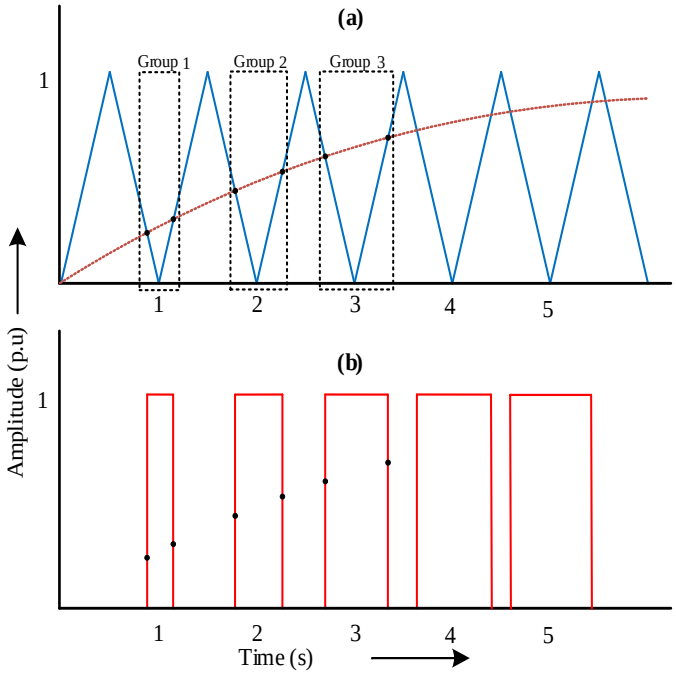


Figure 5.5: SPWM sampling technique (a) SPWM (b) switching pulses

A multi-switching technique such as SPWM is employed frequently in PE inverters to develop an appropriate switching pattern to drive their power switches, which is accomplished by comparing a high-frequency carrier with the lower frequency sinusoidal reference signal to form the preferred nonuniform instances, as shown in Figure 5.5(a). When the modulating signal is higher than the carrier signal, it generates two samples (two edges low to high; then, high to low), shown as groups. These generated groups are used to synthesize an ON-switching pulse, as shown in Figure 5.5(b).

5.5 Modified wavelet-based modulation technique for CHB-MLI

As described before, cascaded H-bridge MLI consists of a series connection of 2-level H-bridge low voltage converters. Each 2-level converter is referred to as a power cell/unit/sub-module (SM) or H-bridge module and consists of four semiconductor switches (S1, S2, S3, and S4) and one DC source/capacitor. Each pair of two switches within the same leg are switched in a complementary form. For example, switches S1 and S2 are in one leg and switches S3 and S4 are in another leg. When S1 is ON, S2 is OFF; similarly, when S3 is ON, S4 is OFF. Therefore, only two switches will be considered at a time for simplicity. The H-bridge module can be turned ON in one of three distinct ways: positive ($+V_{dc}$), negative ($-V_{dc}$) and controlled (0V). The output connections of each SM within the same phase are cascaded together. With the proper modulating technique, the output voltages of the SM have successively added to the synthesis of the desired staircase AC output/resulting voltage waveform.

There are two techniques to achieve this. The first technique modulates the output voltage directly based on comparing the modulating (reference signal) signal to level-shifted carriers (LS-PWM). However, balancing between loads supplied by each H-bridge cell is not ensured, and an external swapping algorithm (load balancing) between the H-bridge cell is required. The second technique uses phase-shifted PWM (PS-PWM), which can naturally swap the H-bridge modules and deliver the desired AC output voltage over the complete range of the modulation index.

As exhibited in the previous section, in WPWM, the dual scale basis function $\varphi(t)$ can develop nonuniform samples required for the PE converters. However, it suffers from the identical drawback as in the level-shifted carrier, where a load balancing algorithm is needed. Therefore, it cannot be directly applied to the cascaded H-bridge MLC without modification. Also, the frequency of the PWM cannot be defined with this function, and the modulation index is not mentioned as well.

The proposed technique can generate variable voltage by varying the control parameter and the scaling variable in the basis function as equation (5-14).

$$\varphi_j(t) = \emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\ t - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right) \quad (5\text{-}14)$$

Where m = control parameter, j = 1, 2, 3, … and $\emptyset_H$ = Haar scaling function

However, this function can be applied only to the 2-level H-bridge module. For the N number H-bridge modules, "N" number of modified dual-scale basis functions are required with phase-shift between each H-bridge module. These N number of equations are formulated in equation (5-15).

$$\varphi_1(t) = \left(\frac{2\pi(2L_1+1)}{4*L}\right)\left[\emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\ t - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]$$

$$\varphi_2(t) = \left(\frac{2\pi(2L_2+1)}{4*L}\right)\left[\emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\ t - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]$$

$$\varphi_3(t) = \left(\frac{2\pi(2L_3+1)}{4*L}\right)\left[\emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\ t - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]$$

.

.

$$\varphi_n(t) = \left(\frac{2\pi(2L_n+1)}{4*L}\right)\left[\emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\ t - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right] \quad (5\text{-}15)$$

Where, $n = 1,2,\dots,N$;

$j = 1,2,3\dots$; and $j \in \mathbb{Z}$;

m = modulation index.

L = number of levels

The generalized equation can be written as equation (5-16).

$$\varphi(t) = \left(\frac{2\pi(2L_n+1)}{4*L}\right)[\varphi_n(t-k)] \quad (5\text{-}16)$$

Where $j = 1,2,3 \ldots$ and $j \in \mathbb{Z}$;

k = 1, 2, 3…

m = modulation index

L = number of levels

The proposed modification for the WPWM is displayed in the first term in equation (4-16). Each H-bridge module requires two equations. One equation is required to generate positive output ($+V_{dc}$), and another equation is needed to generate negative output ($-V_{dc}$). For example, consider a 2-level H-bridge module as shown in Figure 5.6 when switches Q1 and Q4 are turned ON by switching pulses, generated by a modified WPWM equation (at the same time switches Q2 and Q3 are OFF), which produces ($+V_{dc}$) in the output. Similarly, when switches Q2 and Q3 are turned ON by switching pulses, generated by another modified WPWM equation (at the same time, switches Q1 and Q4 are OFF), which produces ($-V_{dc}$) in the output.

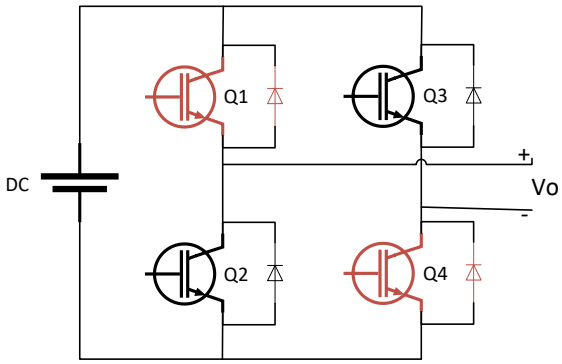


Figure 5.6: Operation of H-bridge module

This modulation technique creates the phase angle difference for each H-bridge module pulse (indicated as $\left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)$ in equation (5-16). This is done without affecting the closed-form representation of WPWM, and hence, it still runs in real-time without iterations. This phase angle disposition depends on the total number of modules (i.e., N).

The modified function $\varphi(\mathrm{t})$ creates a group of two samples during each dilation (j) and shift (k) for the same module. The exact process applies to all modules. The modified function decides the time/locations of the first and second samples of the sample group (g). The relation between the scaling variable (j) and the time interval of each sample group can be indicated in equations (5-17) and (5-18).

$$tg_{n1} = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left[\frac{g}{2} - \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (5\text{-}17)$$

$$tg_{n2} = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left[\frac{g}{2} + \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (5\text{-}18)$$

Where $\mathrm{j} = 1,2,3 \ldots$ and $\mathrm{j} \in \mathbb{Z}$;

g = 1, 2, 3, ….

m = modulation index

L = number of levels

Furthermore, the AC fundamental component is still controllable using the control parameter m. In equation (5-18), the variable m is the control variable, j is

a scaling variable that decides the width of the pulses, and variable g decides the distance between two pulses. The modulation index m controls the essential component of each 2-level module. Also, the scaling variable j decides the width of each pulse. The initial value of $j = 1$ provides the minimum width of the pulse. The maximum value can provide the maximum possible pulse width to prevent over modulation. The value of j varies during each dilation of the H-bridge module signal $\mathrm{x}_{c_n}(\mathrm{t})$ to vary the pulse width. The variables j and k decide the location of the starting and stopping points of the pulses. Therefore, controlling the starting and stopping points of the pulses decrease the harmonics and improves the fundamental component in the output voltage.

The suggested modification can also be described as follows: rather than shifting the pulses by shifting their ON switching edges (edge1 or edge2) (Figure 5.7 and Figure 5.8), the center point of each pulse is shifted, which provides a more accurate relative starting and stopping time of the pulses between different H-bridge modules concerning each other. Hence, a proper stepped output voltage can be generated.

The shifting of pulses in each H-bridge module for dilation of modulating signal (sinusoidal signal) $\mathrm{x}_{c_n}(\mathrm{t})$, in the modified WPWM, the values of j and g improve the accuracy of the pulse location. In equations (5-17) and (5-18), shifting variable g uses the center of gravity of the pulse concept (the middle point of the pulse) and shifts only its center point. Therefore, each pulse's suitable start and stop edges around its respective center point are created.

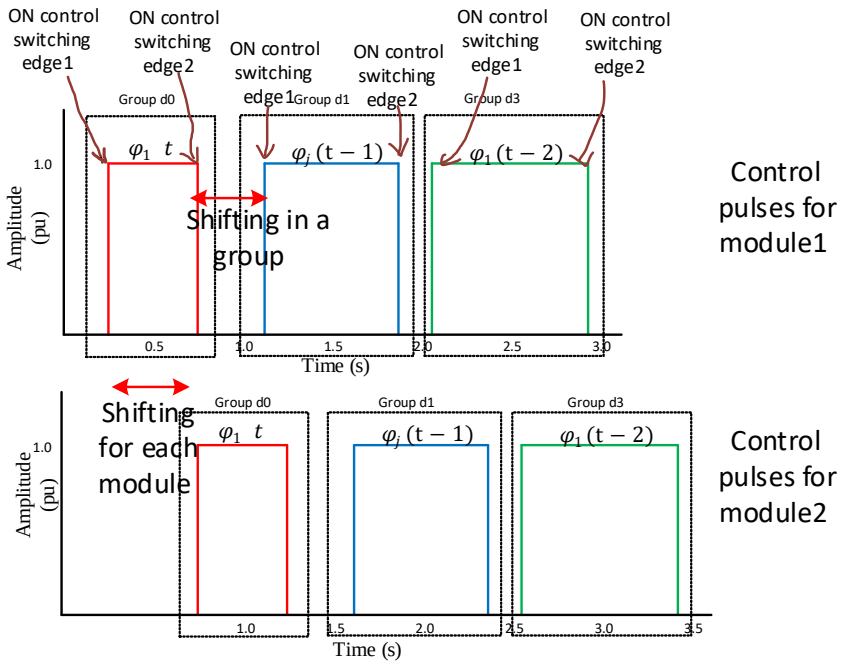


Figure 5.7: Shifted using edges of modified WPWM for the CHB-MLI

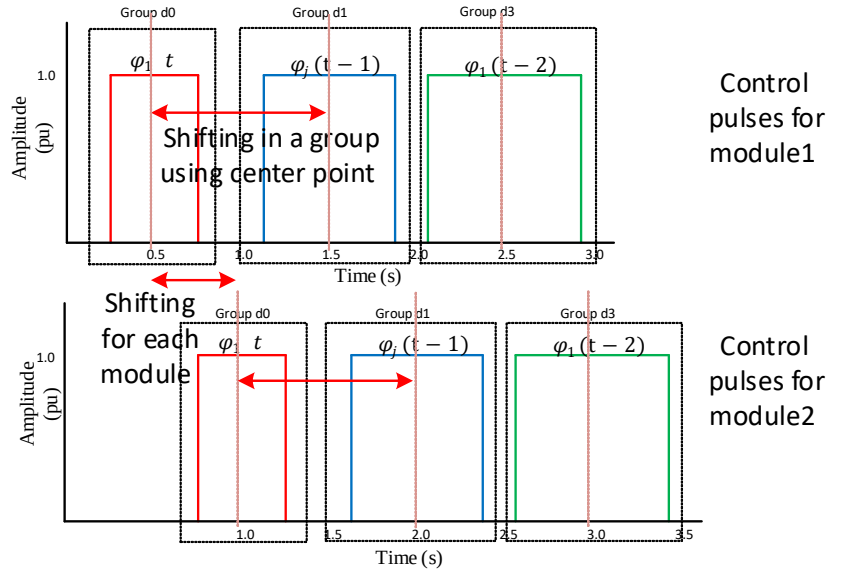


Figure 5.8: Shifted using center point of modified WPWM for the CHB-MLI

The modified wavelet-based modulation technique generates a nonuniform, finite number of switching pulses during each cycle, represented in Figure 5.8 with a different color for each cycle. The switching pulses for each

module can be generated by using the analysis function, which creates a group of two samples and the synthesis function connects both samples. The distance between samples in each pair (i.e., pulse width) will change as the scale j changes. A simple form of the synthesis function can be described in equation (5-19).

$$\tilde{\varphi}_1(t) = \left(\frac{2\pi(2L_1+1)}{4*L}\right)\left\{\emptyset_{H_1}(t) - \left[\emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\ \mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]\right\}$$

$$\tilde{\varphi}_2(t) = \left(\frac{2\pi(2L_2+1)}{4*L}\right)\left\{\emptyset_{H_2}(t) - \left[\emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\ \mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]\right\}$$

.

$$.\tilde{\varphi}_{\mathrm{n}}(t) = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left\{\emptyset_{H_{\mathrm{n}}}(t) - \left[\emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\ \mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)\right]\right\}$$

(5-19)

In general, it can be written as:

$$\tilde{\varphi}_n(t) = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)\left\{\emptyset_{H_n}(t) - \ \varphi_n(t)\right\} \quad (5\text{-}20)$$

Where $\emptyset_{H_n}(t) =$ Haar scaling function.

$\varphi_n(t)$ = dual basis function.

n = 1, 2, …, N,

j = 1, 2, 3…., and j ∈ $\mathbb{Z}$

The proposed WPWM method is an entirely mathematical PWM method with a closed-form solution. It does not rely on carrier signals, making it more suitable to implement on a low-cost digital controller such as a microcontroller, DSP, or FPGA.

5.6 Concept of proposed method

The presented modified wavelet-based PWM method is appropriate for CHB-MLC. This method balances the energy delivered by each DC source, permitting equal load sharing between them. Accordingly, no additional strategy is required to balance the discharge rate of all sources. That indicates it reduces the complexity and expense of the controller.

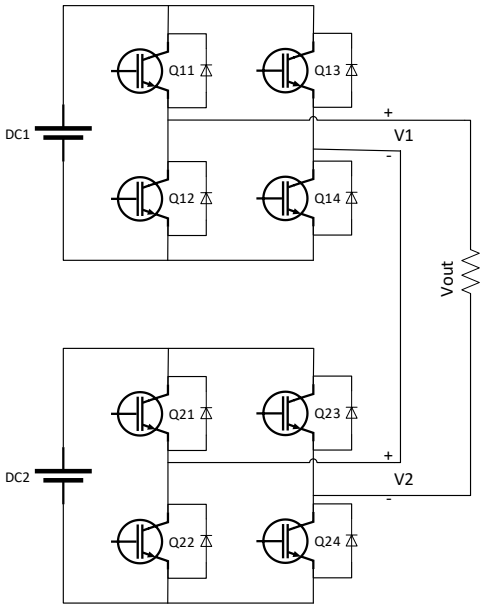


Figure 5.9: Single-phase 5-level CHB-MLI

The discharges of all DC sources can be balanced by allowing a proportional conduction time (T_{con}) for each module. That is shown in Figure

5.10. Also, this can be analyzed with equations, wherein the values in the parentheses (square brackets) generate an equal number of switching pulses that allow equal conduction time for all modules (T_{con}) in Figure 5.10. Also, it provides identical pulse shifting (T_{sh}) in Figure 5.10) between all modules that $\left(\frac{2\pi(2L_n+1)}{4*L}\right)$ can calculate. Identical spacing between each module pulses and equal conduction time of all modules balances the discharge rate of all sources naturally without an additional energy balancing algorithm.

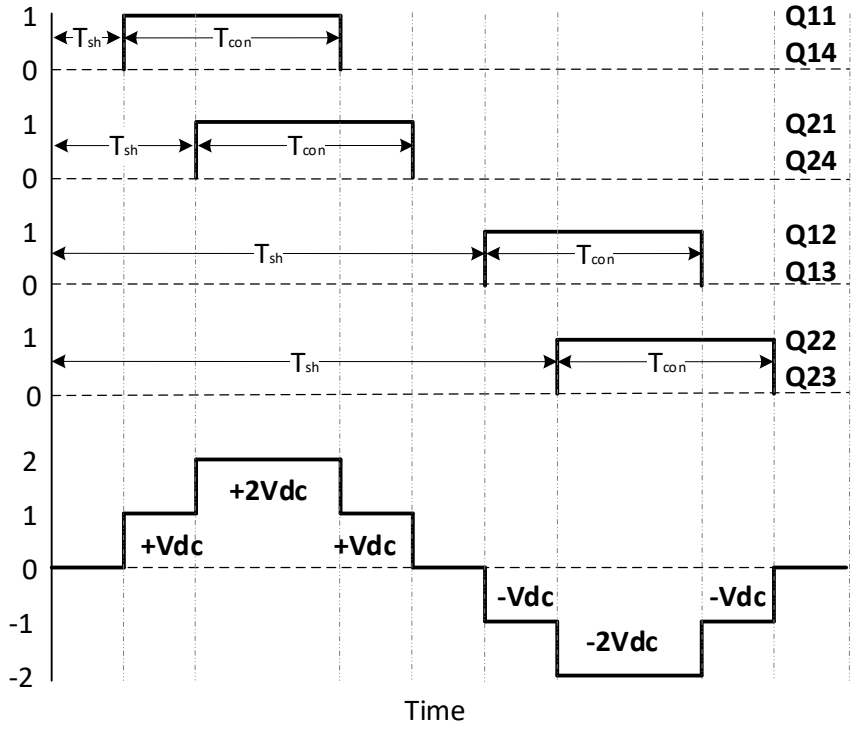


Figure 5.10: Switching pulses and the output voltage of the 5-level CHB-MLI

The output voltage and the switching pulses are applied to the semiconductor switches, as shown in Figure 5.10. Each module needs two equations; one equation generates control pulses for the switches, Q11 & Q14, and the other equation generates control pulses for the switches Q12 & Q13.

When pulses are applied to the switches Q11 & Q14 or Q21 & Q24, it generates $+V_{dc}$. Likewise, when switching pulses are applied to the Q11, Q14, Q21, and Q24, it generates $+2V_{dc}$. Similarly, it generates $-V_{dc}$ when control pulses are applied to the switches Q12 & Q13 or Q22 & Q23. Also, when switching pulses are applied to the Q12, Q13, Q22, and Q22, it generates $-2V_{dc}$. Therefore, four equations are required to generate switching pulses for the 5-level CHB-MLC.

Furthermore, the proposed method provides a variable modulation index. That means output power can be controlled by adjusting the modulation index. In equation (4-15), the modulation index can be changed by changing the variable's value (m). When the value of the modulation index varies, it alters the conduction time of the modules. A smaller modulation index has a shorter conduction time, producing low output power. In this way, the required output power can be generated by the variable modulation index.

Moreover, the suggested method does not require any carrier signal. In most instances, up-down counters can generate triangular carrier signals in the digital controller. For M-level of CHB-MLC requires M-1 numbers of carrier signals. A high-speed digital controller is required to generate numerous carrier signals. However, modified WPWM does not use any carrier signals. It is a mathematical method with a closed-form solution; therefore, all calculations can be conducted within a single iteration, implying that the algorithm does not require high computational power. Also, the proposed method does not rely on a smaller time-step of the digital controller. It can be executed on a low-cost digital controller and decreases overall system cost.

Additionally, the turn ON and OFF times are precisely controlled by adjusting variable j in equation (5-15). Also, in this proposed method, precise switching time can be calculated using equations (5-17) and (5-18). Therefore, a mathematical equation can be formulated to calculate the converter's proper switching and conduction losses. Additionally, this method can be applied to the M number of modules, translating into a lower THD in the output signal. That means a smaller filter size is required, which reduces the complexity of the overall circuit and the system cost.

5.7 Validation of generated pulses using a proposed modulation technique

The pulses generated using the proposed modified wavelet modulation technique for a 5-level CHB-MLI are shown in Figure 5.11. In this Figure 5.11(a) and (b) generate a positive half cycle in the output signal using power cells 1 & 2. Similarly, Figure 5.11(c) and (d) generate a negative half cycle through both power cells.

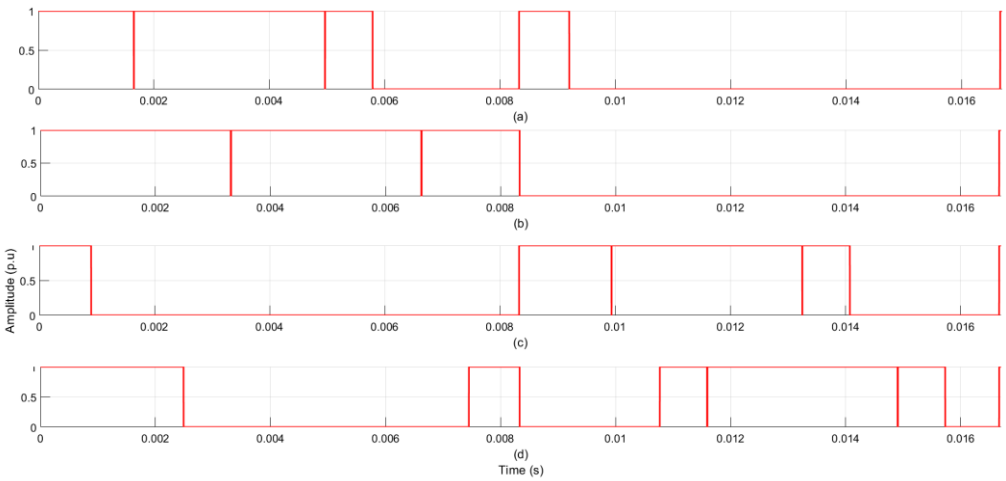


Figure 5.11: Switching pulses for 5-level CHB-MLI

Moreover, these pulses have equal ON and OFF times for switches used for power unit 1 and power unit 2. The approximate ON/OFF time ensures the equal conduction time of both power units. Therefore, sources connected to both power units have equal discharge rates and natural balance. Hence, the source balance technique is no longer required, reducing the converter's cost and complexity. More results have been discussed in a later chapter to validate the proposed modulation strategy.

5.8 Previous WPWM and proposed modified-WPWM methods.

WPWM technique was used with CHB-MLC for the fist time in 2016 [139]. This configuration used old scaling and synthesis functions to generate switching pulses. This pair of equations generates switching pulses for 2-level H-bridge only. Therefore, additional logic circuit was needed which is shown in Figures 3.1 and 3.2. The additional logic circuit increase the complexity of the converter with higher number of levels. Also, it increases the possibility of component failure and increases losses in the control circuit. In addition, it has higher switching loss since it uses a higher switching frequency.

In 2017, Dr. Saleh implemented this method on CHB-MLC which uses only mathematical equations to generate switching pulses for all modules [140]. In this method each H-bridge has two pair of equations as descried for 2-level inverter. However, the value of scaling parameter (j) is different as shown in equations (3-8) to (3-10) for all H-bridges. In this method 52 switching pulses are generated per modulation signal (means switching frequency = 3.12 kHz) [140],

which triggers higher switching losses, that impacts on the efficiency of the converter in high voltage applications.

For example, if the turn-on time of the switch, $t_{on} = 18ns$. The current passing through the switch, $I_{D(on)} = 10A$, and the voltage, $V_{DD} = 200V$.

The Energy loss during the turn-on can be calculated as:

$$E_{on} = I_{D(on)} V_{DD} t_{on} \frac{1}{2} = (10\text{A})(200\text{V})(18\text{ns})\frac{1}{2} = 18\mu J \quad (5\text{-}21)$$

Turn-on power loss: $P_{on} = E_{on} f_{sw} = 18\mu J * 3.12\ kHz = 0.056\ W$ (5-22)

Similar power loss happened during turn-off as well, $P_{off} = 0.056\ W$

So, the total switching loss in each switch is $0.112\ W$

Moreover, in this method the switching pulses are vertically shifted. As a result, each module has a different conduction time, means unequal conduction losses among the H-bridge modules (PE switches). It is leading to an uneven semiconductor junction temperature distribution. Therefore, the PE switches with low junction temperature are not fully utilized.

The proposed method utilizes pair of equations for each H-bridge to generate switching pulses. Unlike the above methods, the switching pulses generated with proposed method are horizontally shifted for each H-bridge. The horizontal shift provides equal conduction time for each H-bridge which also helps in self-balancing the load current, and all switches are equally utilized. Moreover, the shifting of pulses in each H-bridge module for dilation of modulating signal (sinusoidal signal) $\mathrm{x}_{c_n}(\mathrm{t})$, in the proposed method, the values

of j and g improve the accuracy of the pulse location. In equations (5-17) and (5-18), shifting variable g uses the center of gravity of the pulse concept (the middle point of the pulse) and shifts only its center point. Therefore, each pulse's suitable start and stop edges around its respective center point are created.

In addition, the proposed method uses 180 Hz switching frequency without introducing lower harmonics in the output signal. Therefore, the switching loss is very low which improves the efficiency pf the converter.

The energy loss during the turn-on can be calculated as:

$$E_{on} = I_{D(on)} V_{DD} t_{on} \frac{1}{2} = (10\text{A})(200\text{V})(18\text{ns})\frac{1}{2} = 18\mu J \quad (5\text{-}23)$$

Turn-on power loss: $P_{on} = E_{on} f_{sw} = 18\mu J * 0.18\, kHz = 0.003\, W$ (5-24)

Similar power loss happened during turn-off as well, $P_{off} = 0.003\, W$

So, the total switching loss in each switch is $0.006\, W$

5.9 Summary

In this chapter, wavelet-based sampling theorem, concept of Haar wavelet and building a non-dyadic type MRA are shown. After that, the purpose and creation of a proposed, newly developed modified wavelet-based modulation technique for CHB-MLC were discussed. Also, developed analysis and synthesis scaling functions are presented, which generate the precise switching signals for the PE switches for the CHB-MLC. In the end, the method is compared with previously applied WPWM method on CHB-MLC.

The next chapter explains an implementation of the proposed method. Then, it is validated using the MATLAB simulation model of 5, 7 and 9-levels CHB-MLC and examine the results.

Chapter 6. MATLAB Simulation

6.1 Introduction

A CHB-MLI converts the DC input signal into an AC output signal. This transformation can be attained by turning ON/OFF the PE switches in a proper sequence. Diverse strategies were designed to operate this converter to generate an AC output signal. This converter is often used in medium/high voltage applications. However, the primary consideration is the generation of harmonics, and the power loss incurred during switching, specifically in high voltage applications. In general, achieving converter outputs with possibly the lowest harmonics is traded against the switching scheme's increased complexity and the inverter's efficiency (increasing switching losses). A possible procedure for reducing harmonic components and switching losses is to create a modulation method that balances multiple input sources and executables on a digital controller.

This chapter compares the proposed modified-WPWM method's THD and fundamental components outcomes with the frequently employed multi-carrier-based PS-PWM method's outcomes for single-phase CHB-MLI. Both modulation techniques are implemented using the same switching frequency and the same level of CHB-MLI.

6.2 Implementation of modified wavelet-based modulation technique:

PE switches, such as MOSFET/IGBTs, need pulses that can rapidly turn them ON/OFF in an inverter circuit. During a positive half-cycle, the current flows from the positive terminal to the load's negative terminal, and in the other half-

cycle current flows in the opposite direction. In the CHB-MLI, the current duration stays the same in the load, except the switching pattern for the multiple H-bridge units ensures the multiple levels in the output signal. The modified wavelet-based modulation technique can integrate this practical control logic implementation for the CHB-MLI. This technique ensures the output's lowest unwanted frequency signal and highest fundamental frequency signal. In this method, switching pulses are generated for each power unit in two steps:

1. First, an analysis function $\varphi_{\mathrm{n}}(\mathrm{t})$ creates a pair of samples separated by non-uniform time intervals.
2. In the second part, synthesis function $\tilde{\varphi}_n(t)$ is used to synthesize the generated pair of samples to create a switching pulse.

One analysis and one synthesis scaling function are used for each power unit. The shifting function generates the required phase displacement between two power units $\left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4L}\right)$. This technique ensures easy implementation, and minimum energy is distributed in the harmonic components.

This modulation technique aims to create a non-dyadic type MRA for each power unit. This product is done by sampling the reference modulation signals using a phase-shifted version of the analysis scaling function in a non-uniform recurrent behavior and reconstructing them with the inverter switching pattern. As mentioned earlier, practical implementation is divided into two parts.

1. In the first part, the actual frequency duration $\mathrm{T}_{\max}$ is considered to generate non-uniform recurrent samples. $\mathrm{T}_{\max}$ is the period of the

reference/modulating signal S_{ref}. A pair of samples are created for each power unit by a dilated and shifted version of the analysis function $\varphi_{\mathrm{n}}(\mathrm{t})$. Each pair of samples is stored in a group.

2. In the second part, each power unit's switching pulses are generated by synthesizing the pair of samples using the synthesis scaling function $\tilde{\varphi}_n(t)$.

The time interval for the created samples group is defined in equation (6-2). These samples are formed by the analysis scaling function per dissection (i.e., by varying the value of the scaling variable j) and shifted (i.e., by varying the value of the shifting variable k).

$$t \in [tg_{n1}, tg_{n2}] \tag{6-1}$$

$$\varphi(\mathrm{t}) = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4*L}\right)[\varphi_{\mathrm{n}}(\mathrm{t}-\mathrm{k})] \tag{6-2}$$

where: $\varphi_{\mathrm{n}}(\mathrm{t}) = \varphi(\mathrm{t}) = \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\mathrm{t}\right) + \emptyset_{\mathrm{H}}\left(\frac{2^{\mathrm{j}+1}}{2-m}\,\mathrm{t} - \left(1 - \frac{1}{2^{j+1}/_{2-m}}\right)\right)$

The variables tg_{n1} and tg_{n2} represent the locations of the sample group's (g) first and second samples instances on the time scale. The duration for each sample group for the scaling function is defined by the variable j. Mathematically these can be represented as equations (6-3) & (6-4).

$$tg_{n1} = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4L}\right)\left[\frac{g}{2} - \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \tag{6-3}$$

$$tg_{n2} = \left(\frac{2\pi(2L_{\mathrm{n}}+1)}{4L}\right)\left[\frac{g}{2} + \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \tag{6-4}$$

Where $j = 1,2,3 \ldots$ and $j \in \mathbb{Z}$;

g = 1, 2, 3, …..

m = control variable

L = number of levels

The regaining of the reference/modulation signal (in the form of switching pulses from its non-uniform samples) is done with the dilated and shifted interpretations of the synthesis scaling function. The interval of each dilated and shifted interpretation of the synthesis scaling function is described as:

$$\tilde{\varphi}_n(t) = \left(\frac{2\pi(2L_n+1)}{4*L}\right)\{\emptyset_{H_n}(t) - \varphi_n(t)\} \quad (6\text{-}6)$$

where:

$$\varphi_n(t) = \varphi(t) = [\varphi_n(t-k)] = \emptyset_H\left(\frac{2^{j+1}}{2-m}t\right) + \emptyset_H\left(\frac{2^{j+1}}{2-m}\,t - \left(1 - \frac{1}{2^{j+1}/2-m}\right)\right)$$

Therefore, both analysis and scaling functions at scale j and shift k have similar support intervals. This function is identical to the Haar scaling function property used to create a scale-based linearly combined function. The ON-switching pulse, using a synthesis scaling function $\tilde{\varphi}_n(t)$ at scale j and shift k, is defined as

$$ON_{\tilde{\varphi}_n} = tg_{n2} - tg_{n1} \quad (6\text{-}7)$$

The modified wavelet-based modulation technique can be implemented using the steps shown in section 6.3.

6.3 Simulation of a modified-wavelet-based modulation technique for CHB-MLI

The implementation steps of modified-wavelet-based modulation technique for a single-phase CHB-MLI is described in this section. Following steps are used to implement this technique in Simulink.

Step 1: Assign the value of the sample time variable (Sam), frequency of the reference signal variable (fm), and required level (Lev) in the output based on the power unit used in the CHB-MLI.

Step 2: Initiate the step-time at $t = 0\ us$. The scaling parameter begins with $j = 1$, control parameter $m = 1$ for maximum output, and shifting parameter $k = 3$. The variables g1 and g2 can be considered shifting parameters initiated as $g1 = 3$ and $g2 = 3$. The values of $g1$ and $g2$ can be updated using the shifting parameter k. The converter output can be controlled by varying the value of scaling parameter j and control variable m.

Step 3: If $t < T_{max}$, the program calculates the value for samples tg_{n1} and tg_{n2} using equations (6-8) and (6-9). The calculated values will be stored in a group to create the ON-switching pulses:

$$tg_1 = \left(\frac{2\pi(2L_n+1)}{4L}\right)\left[\frac{g}{2} - \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (6\text{-}8)$$

$$tg_2 = \left(\frac{2\pi(2L_n+1)}{4L}\right)\left[\frac{g}{2} + \left(\frac{1}{2} - \frac{1}{2^{j+1}/_{2-m}}\right)\right] \quad (6\text{-}9)$$

Where $j = 1,2,3\ldots$ and $j \in \mathbb{Z}$; g = 1, 2, 3, …. m = control variable

Step 4: The ON-switching pulses can produce a positive signal in the output when $t < {}^{T_{max}}/_{2}$.

Step 5: Set the condition, as shown in the flowchart (Figure 6.1), to update the shifting parameter value and generate the control signal.

Step 6: Check the condition if $t < T_{max}$. If the condition is true, start from step 3; or, if the condition is false, go to step 2.

Step 7: Repeat the above steps to generate control signals for the other power unit used in the single-phase CHB-MLI.

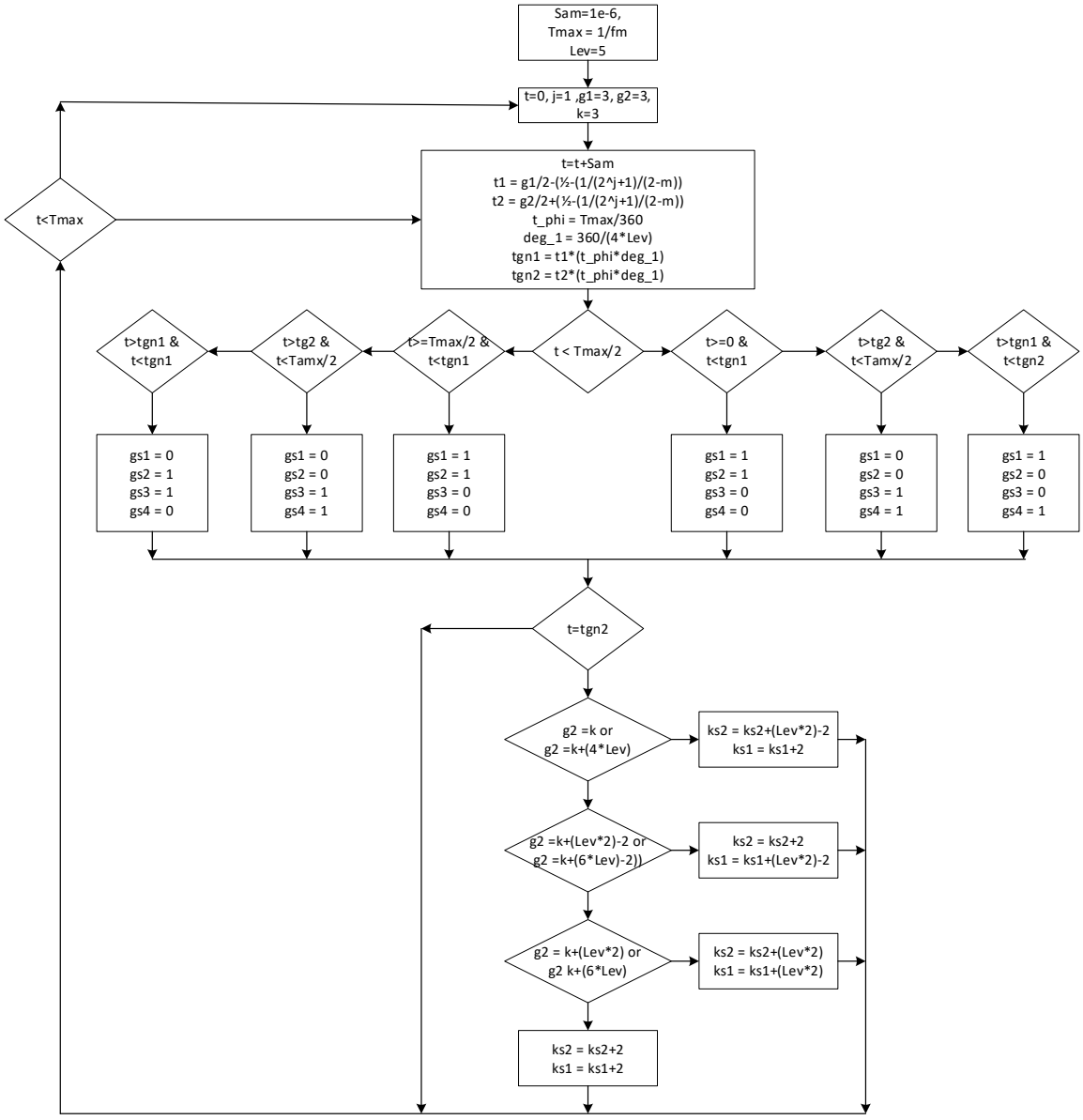


Figure 6.1: Flow chart of modified-WPWM for implementation

6.4 Simulations and results of single-phase modified-WPWM

The proposed modified WPWM strategy for a CHB-MLI has been verified with MATLAB Simulink simulation studies to investigate the performance of this control scheme. This strategy has been applied to a 5-level, 7-level, and 9-level single-phase CHB-MLI, and produced results are compared with the PS-PWM

modulation technique to validate. This comparative study tested the fundamental component and harmonics in the output signal for resistive, inductive, and dynamic loads. The switching frequency of 180 Hz was used. The DC bus voltage is ±200 V, measured at the converter's output terminals before the output filter.

6.4.1 Simulation with 10 kΩ resistive load

A linear 10 kΩ resistive load is selected for simulation study to test the performance of a multi-level CHB converter controlled with the proposed modified WPWM control scheme. This study is performed to investigate the steady-state operation of the converter with the proposed control method and compared with the PS-PWM method. The CHB-MLI supplies a 10 kΩ resistive load. The resistive load voltage and current are shown in Figure 6.2 to Figure 6.7. The results show that the modified-WPWM method generates identical positive and negative cycles like the PS-PWM method. Also, the pulsating output waveforms generated by the PS-PWM and modified-WPWM schemes have equal amplitude and frequencies at all levels.

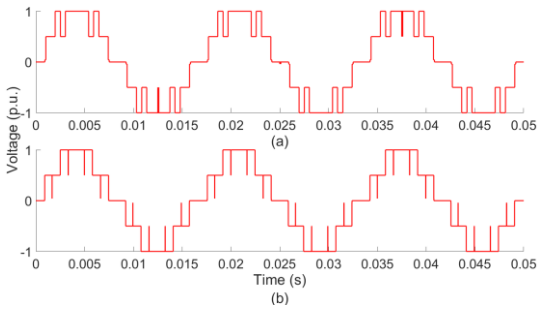


Figure 6.2: Output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

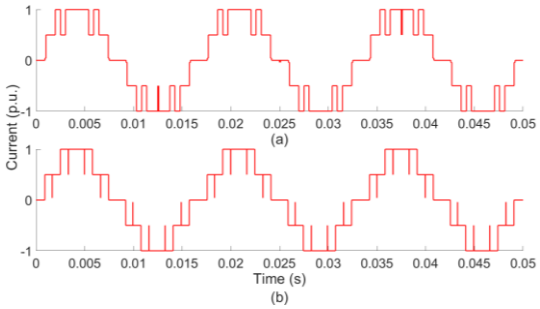


Figure 6.3:Output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

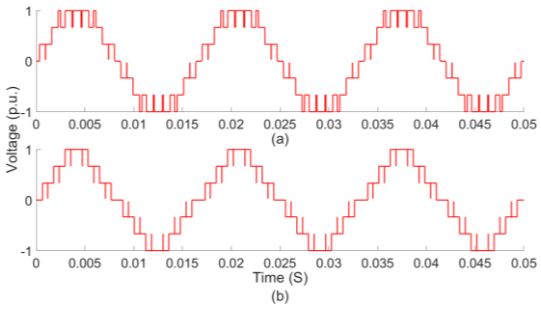


Figure 6.4: Output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

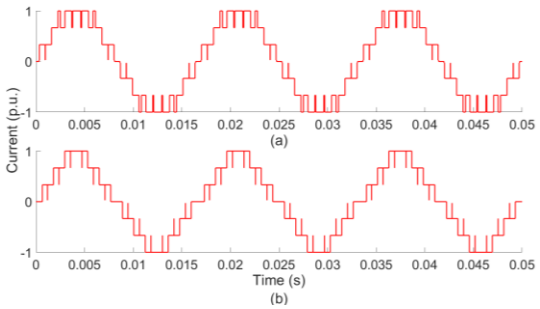


Figure 6.5: Output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

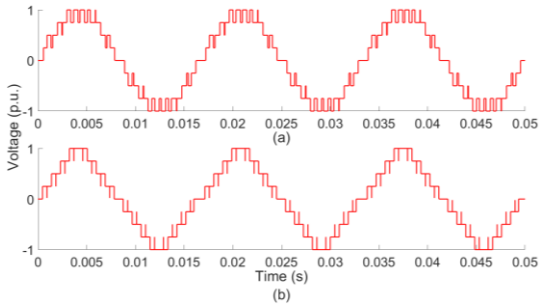


Figure 6.6: Output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

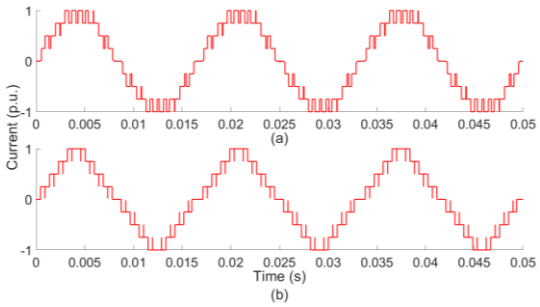


Figure 6.7: Output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

Power converters generate a considerable number of harmonics. These harmonics decrease the efficiency and life expectancy of the other corresponding electrical equipment. In practice, reducing harmonics at the modulation stage is

always beneficial. This study is conducted to observe the proposed method's harmonic performance of the converter. The harmonic spectra of load voltage and current are obtained using a MATLAB FFT function to determine their THDV and THDI factors. The FFT results of all levels are shown in Figure 6.8 to Figure 6.13. These graphical representations show (highlighted with a rectangle box) that the spectrum generated with the modified-WPWM has a lower amplitude than the harmonics generated by the PS-PWM technique. Therefore, modified-WPWM has lower THD, which is shown in Table 5-1. The voltage and current THD values of the 9-level, 7-level, and 5-level modified-WPWM are 15.81%, 17.67%, and 20.57%, respectively. All harmonics are measured before the output filter at the output terminal.

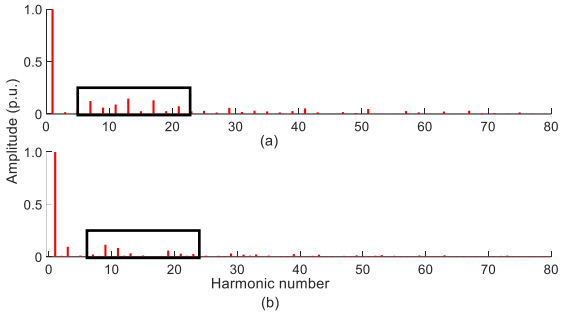


Figure 6.8: Harmonics in the output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

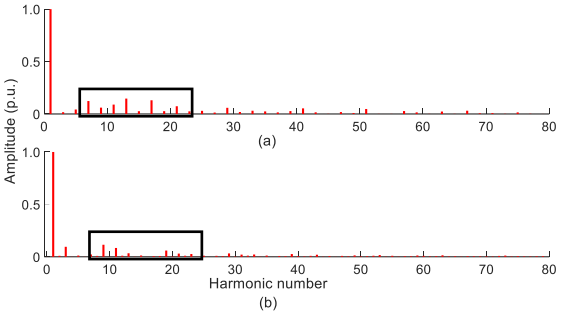


Figure 6.9: Harmonics in the output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

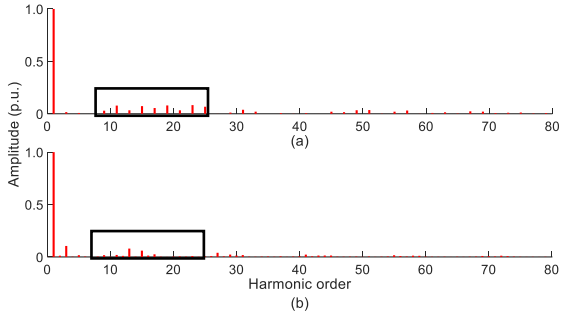


Figure 6.10: Harmonics in the output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

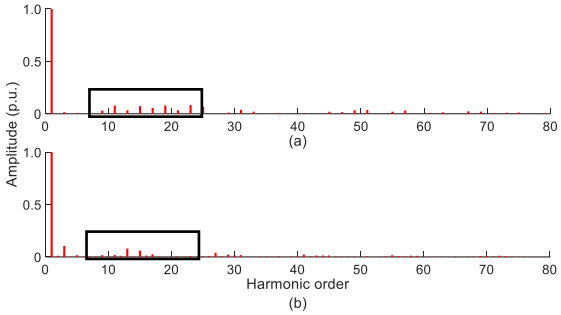


Figure 6.11: Harmonics in the output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

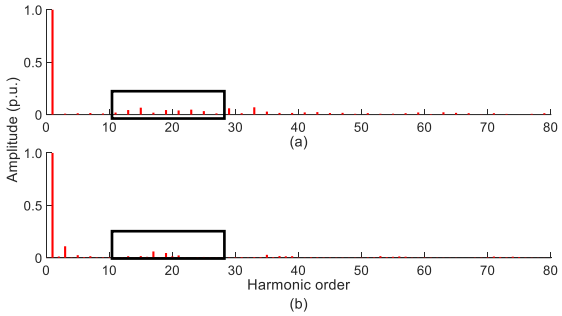


Figure 6.12: Harmonics in the output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

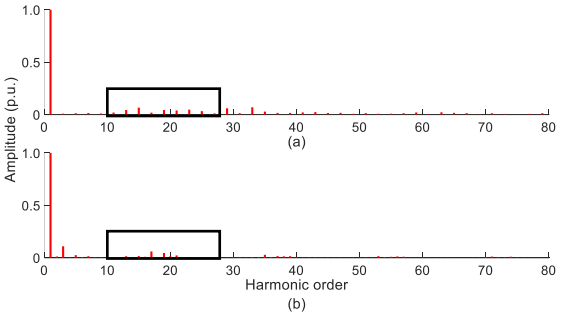


Figure 6.13: Harmonics in the output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

Table 6-1 summarizes the THD generated by the 5, 7, and 9-level CHB-MLI when they are controlled with the carrier-based PS-PWM and modified-

WPWM method. Identical data is used for the graphical comparison (Figure 6.14) of the harmonic in the output voltage.

Table 6.1: Harmonics in the output voltage for a 5, 7, and 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

	PS-PWM THD (%)	**Modified-WPWM THD (%)**
5-Level	31.40	20.57
7-Level	22.84	17.67
9-level	18.20	15.81

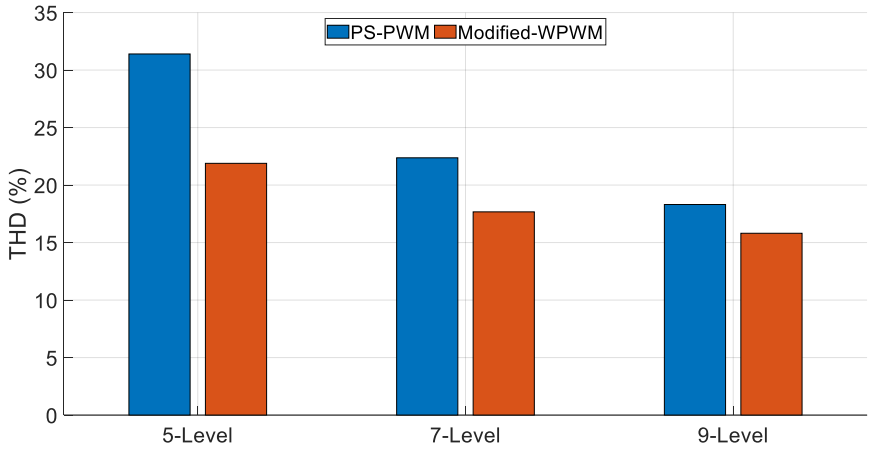


Figure 6.14: The comparison of voltage harmonics for 5, 7, and 9-level CHB-MLI for the PS-PWM and modified-WPWM.

Furthermore, the testing is extended to validate the charge balancing feature of the modified-WPWM technique. The charge balancing is one of the significant challenges in CHB-MLI, mainly when employed in renewable energy harvesting or energy storage systems. Figure 6.15 to Figure 6.17 show the result of each source's current discharging in the 5, 7, and 9-level CHB-MLI. These results are shown for the modified-WPWM and PS-PWM techniques. The PS-

PWM method naturally balances the source discharge current. Similarly, the modified-WPWM method can balance all source discharge current without other control logic. However, minor vertical displacement can be seen in Figure 6.15(b), Figure 6.16(b), and Figure 6.17(b).

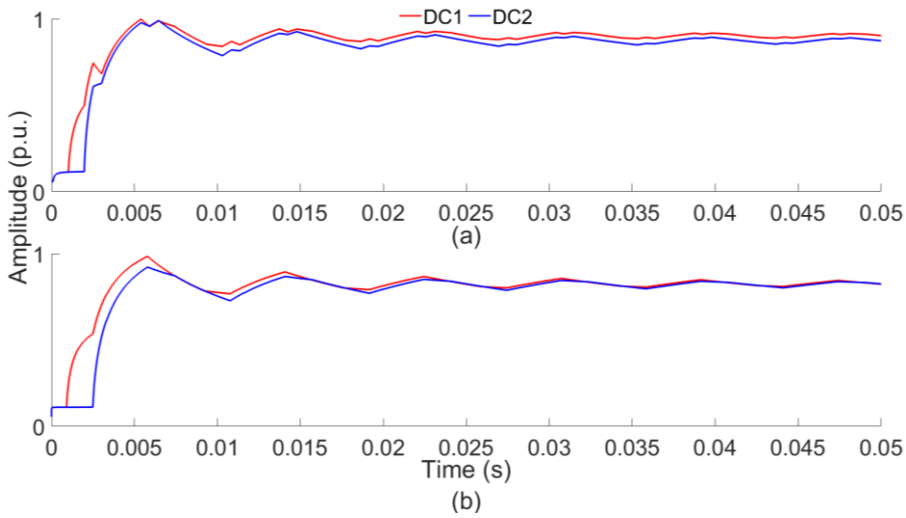


Figure 6.15: RMS value of discharging current of all sources in 5-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

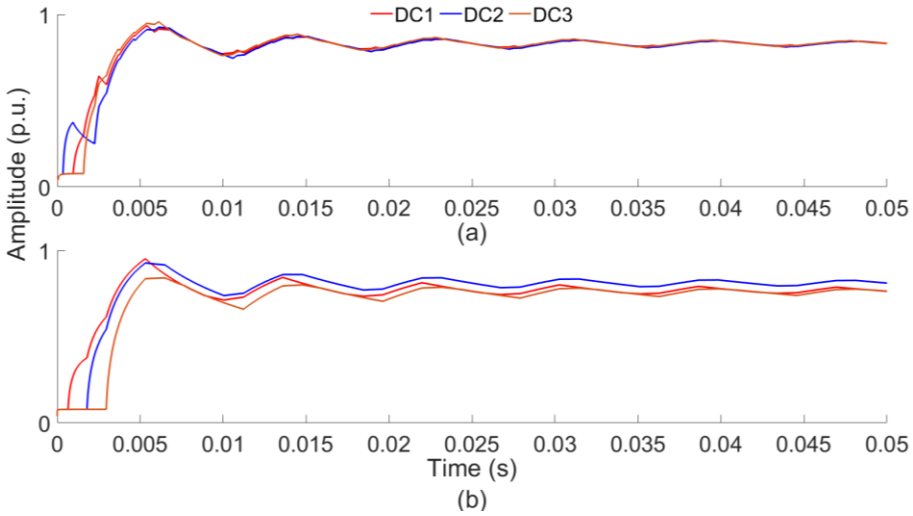


Figure 6.16: RMS value of discharging current of all sources in 7-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

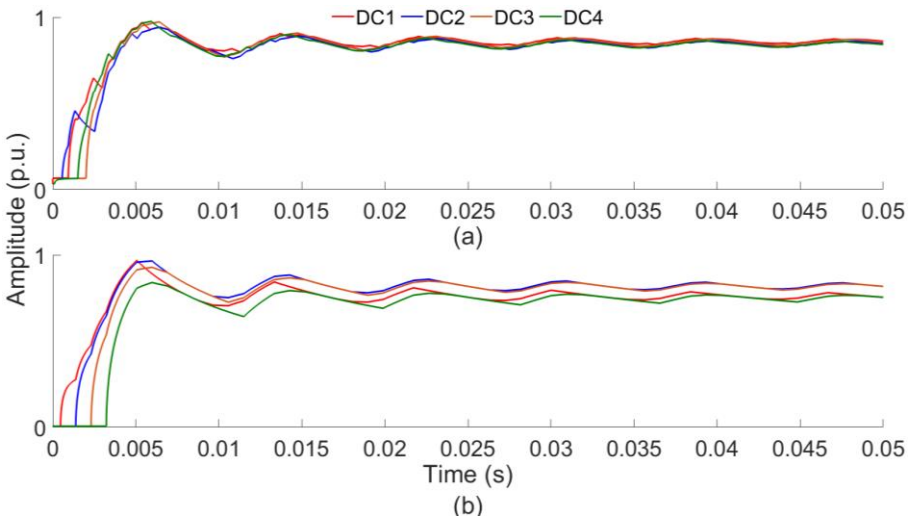


Figure 6.17: RMS value of discharging current of all sources in 9-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

6.4.2 Simulation with R-L Load

The simulation model of modified-WPWM is verified with a series R-L load, 8+j5.6 kΩ on the output side of the CHB-MLI. For this study, 5-7-, and 9-levels CHB-MLI are used. Figure 6.18 to Figure 6.23 show the measured load voltage $V_l(t)$ and current $I_l(t)$ before the harmonic filters. The results are approximated with the PS-PWM-based CHB-MLI converter to ensure the performance of the presented strategy. The result shows minor inconsistency (Highlighted with a rectangular box) in the quarter cycle of the output voltage signal of all 5-, 7-, and 9-level PS-PWM-based CHB-MLI. However, this is not seen in the modified WPWM-based CHB-MLI.

The waveform of the load current for PS-PWM and modified-WPWM-based CHB-MLI is displayed in Figure 6.21 to Figure 6.23. There is no variation seen in the load current for both methods. However, the modified WPWM-based CHB-MLI shows a more refined output signal than the PS-PWM method.

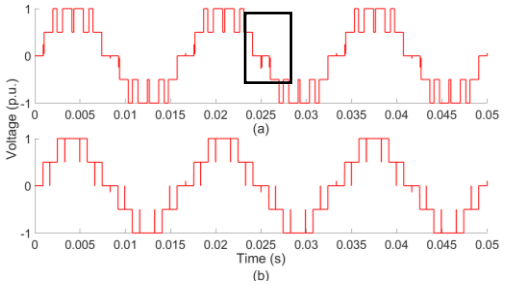


Figure 6.18: Output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

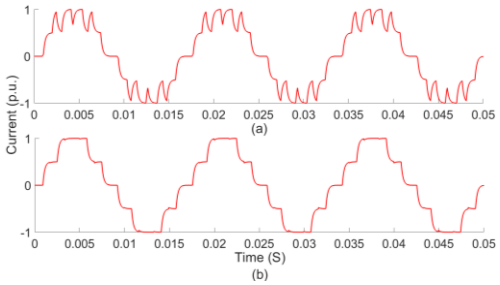


Figure 6.19: Output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

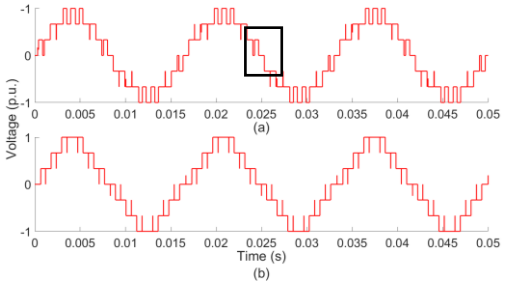


Figure 6.20: Output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

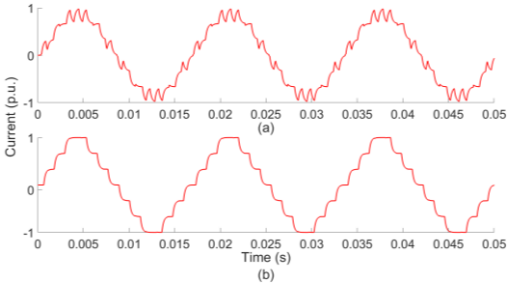


Figure 6.21: Output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

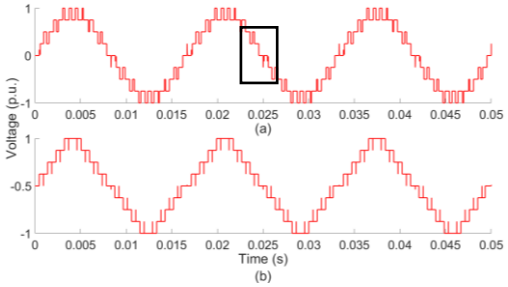


Figure 6.22: Output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

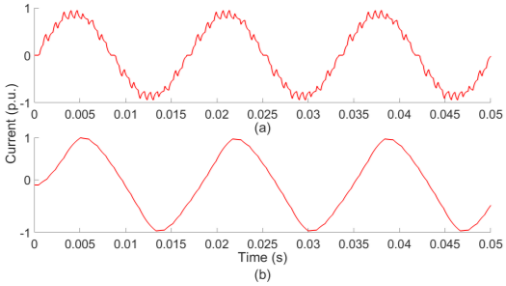


Figure 6.23: Output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

The voltage and current harmonic spectrum for the 5-, 7-, and 9-level CHB-MLI are illustrated in Figure 6.24 to Figure 6.29. In all levels of CHB-MLI, both voltage and current have smaller amplitude and lesser harmonic spikes for the modified-WPWM-based system. Therefore, the efficiency is higher for this system than the PS-PWM-based system.

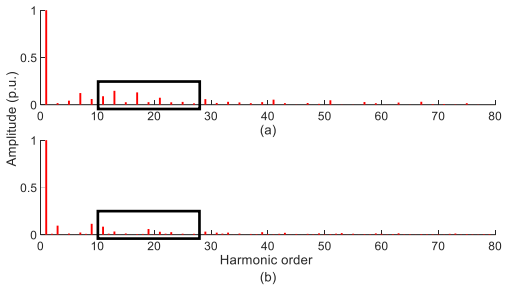


Figure 6.24: Harmonics in the output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

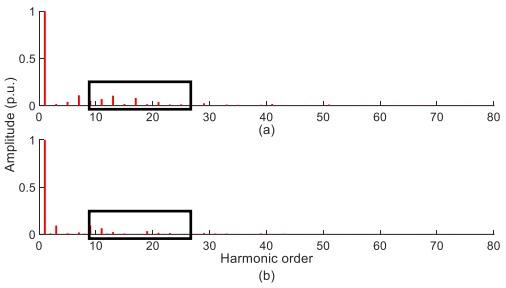


Figure 6.25: Harmonics in the output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

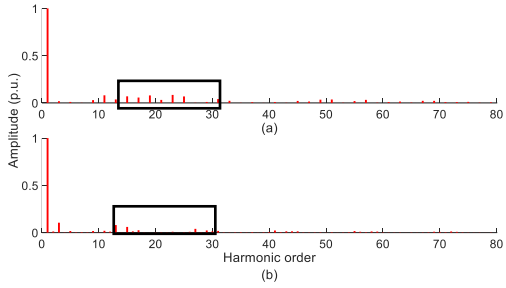


Figure 6.26: Harmonics in the output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

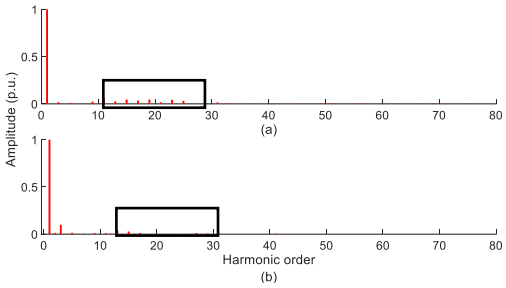


Figure 6.27: Harmonics in the output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

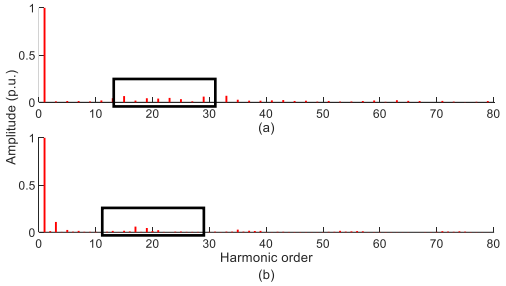


Figure 6.28: Harmonics in the output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

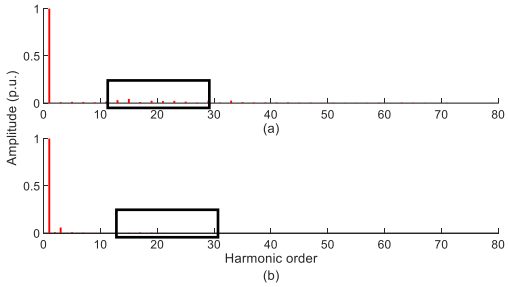


Figure 6.29: Harmonics in the output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

Table 6.2 shows the numerical representation of the THD generated by the 5, 7, and 9-level CHB-MLI. These results are generated when all three configurations of CHB-MLI are controlled with the carrier-based PS-PWM and

modified-WPWM method. Identical data is used for the visual comparison (Figure 6.30 and Figure 6.31) of the harmonic in the output voltage.

Table 6.2: Harmonics in the output voltage for the CHB-MLI with RL load (a) PS-PWM (b) modified-WPWM.

	PS-PWM THD (%)	**Modified-WPWM THD (%)**
5-Level	31.42	20.93
7-Level	22.84	17.69
9-Level	18.20	15.81

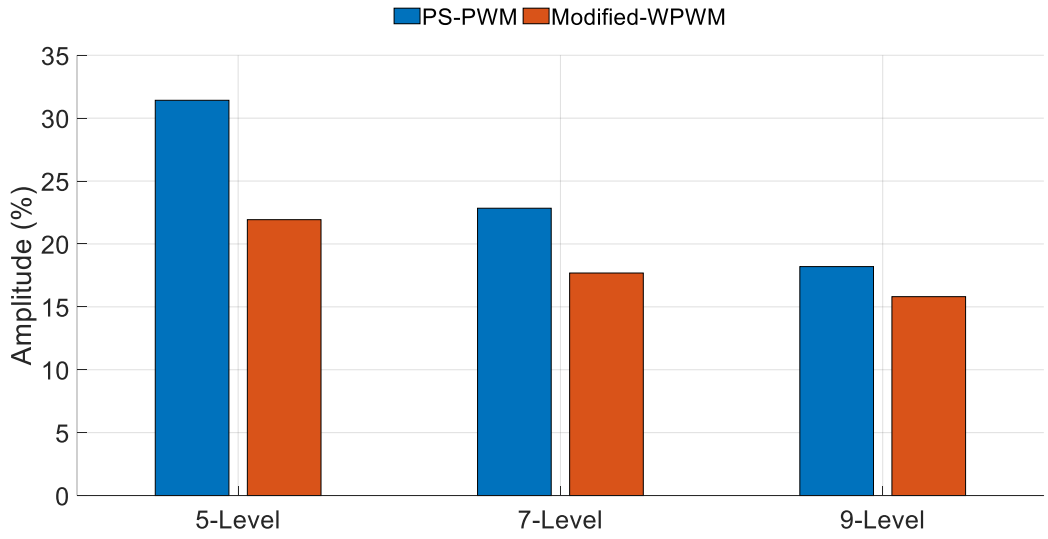


Figure 6.30: The comparison of voltage harmonics for 5, 7, and 9-level CHB-MLI for the PS-PWM and modified-WPWM.

Table 6.6.3: Harmonics in the output current for the CHB-MLI with R load (a) PS-PWM (b) modified-WPWM.

	PS-PWM THD (%)	**Modified-WPWM THD (%)**
5-Level	20.68	16.09
7-Level	12.25	11.62
9-Level	8.57	6.06

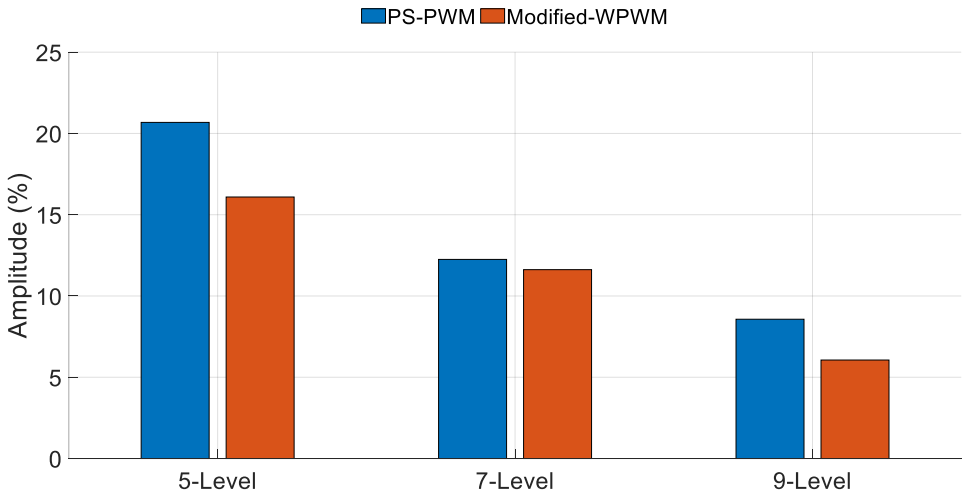


Figure 6.31: The comparison of current harmonics for 5, 7, and 9-level CHB-MLI for the PS-PWM and modified-WPWM.

Like the simulation with R-load, this simulation also estimated discharging current of all sources for modified-WPWM and PS-PWM-based systems. The results are displayed in Figure 6.32 to Figure 6.34. The results are equivalent for both techniques. All sources have equal discharging rates except for slight vertical displacement in source current in Figure 6.33 and Figure 6.34.

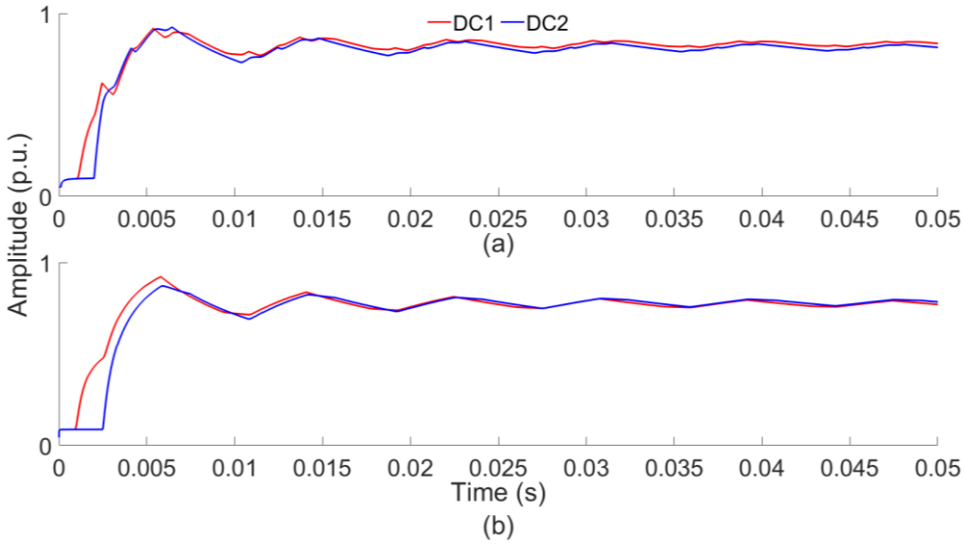


Figure 6.32: RMS value of discharging current of all sources in 5-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods

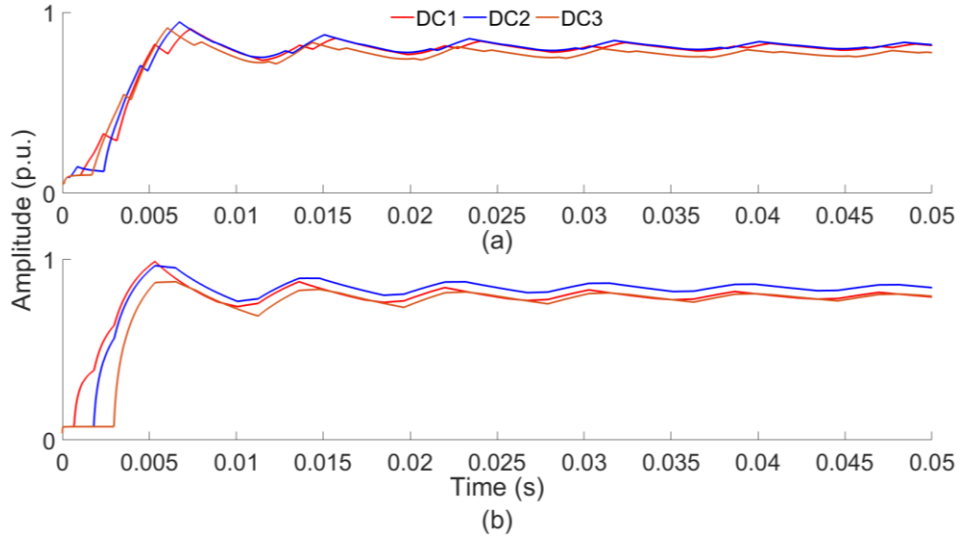


Figure 6.33: RMS value of discharging current of all sources in 7-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

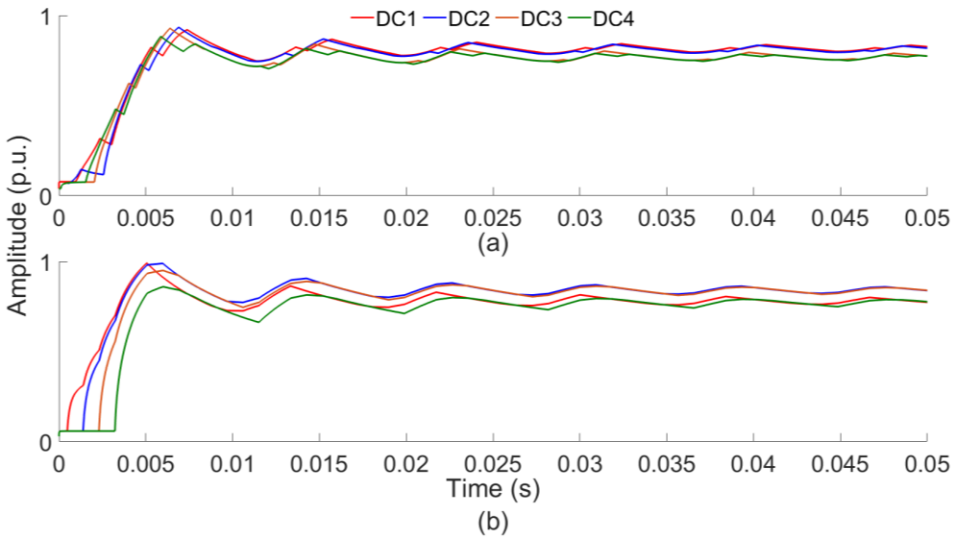


Figure 6.34: RMS value of discharging current of all sources in 9-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

6.4.3 Simulation with a Non-linear Load

This study analyzes the performance of modified-WPWM in open-loop steady-state conditions with a non-linear load. A full-bridge rectifier is a non-linear load for all 5, 7, and 9-level CHB-MLI. A single-phase full-bridge rectifier circuit supplies power to the 10 kΩ resistive loads in each case. The output voltage $V_l(t)$ and current $I_l(t)$ are measured at the common coupling point of DC/AC and AC/DC converter terminals. The simulation results of the 5-, 7-, and 9-level CHB-MLI with non-linear load are displayed in Figure 6.35 to Figure 6.40. The pulsating output waveform for the voltage and current have a similar amplitude and frequency to the PS-PWM method.

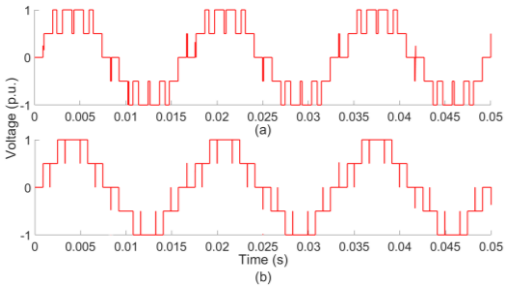


Figure 6.35: Output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

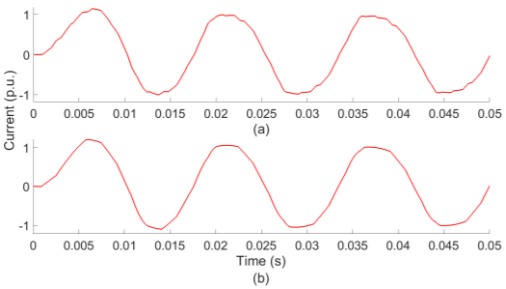


Figure 6.36: Output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

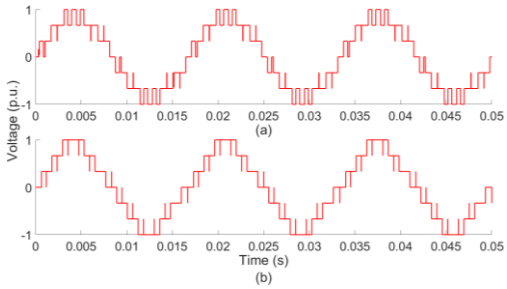


Figure 6.37: Output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

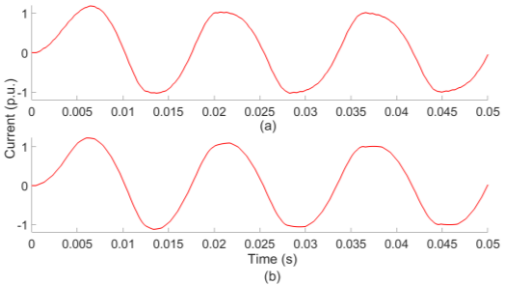


Figure 6.38: Output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

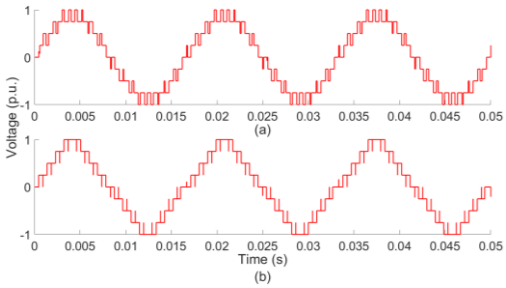


Figure 6.39: Output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

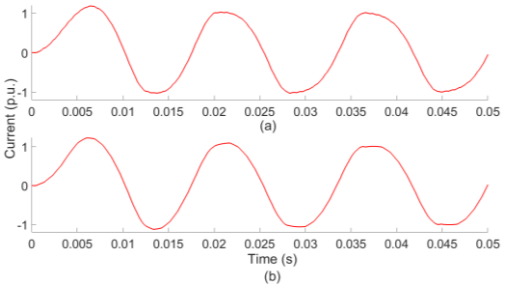


Figure 6.40: Output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

The generated harmonics are the noticeable thing resulting in the voltage and current. Like the other simulation test, modified WPWM has lower amplitude harmonics in the output voltage and current (Figure 6.41 to Figure 6.46). Therefore, lesser energy loss occurs in the unwanted harmonic frequencies. This means that more high-quality signals can be developed in the output. So, the

higher power can be transferred from the source to the load. The voltage and current harmonics comparison is shown in Figure 6.47 and Figure 6.48, respectively. The emphasized area shows the higher amplitude harmonics generated with the PS-PWM scheme.

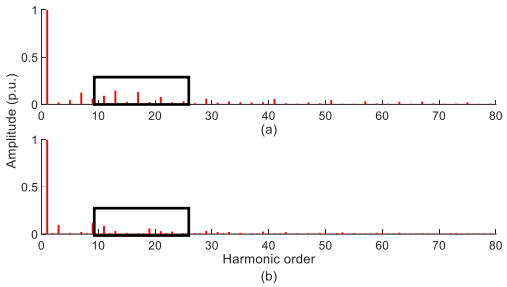


Figure 6.41: Harmonics in the output voltage for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

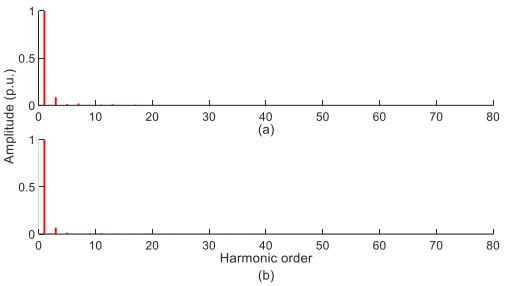


Figure 6.42: Harmonics in the output current for a 5-level CHB-MLI (a) PS-PWM (b) modified-WPWM

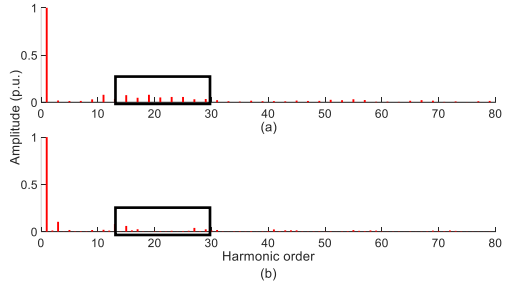


Figure 6.43: Harmonics in the output voltage for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

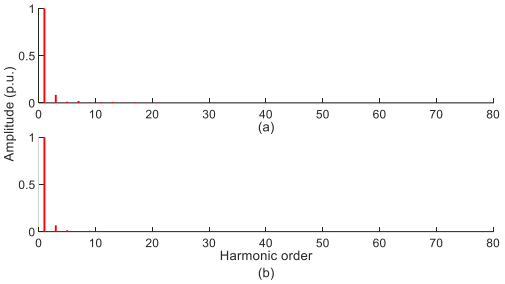


Figure 6.44: Harmonics in the output current for a 7-level CHB-MLI (a) PS-PWM (b) modified-WPWM

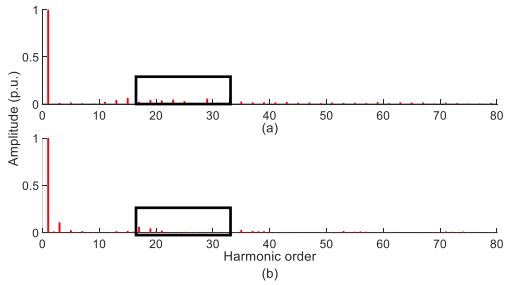


Figure 6.45: Harmonics in the output voltage for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

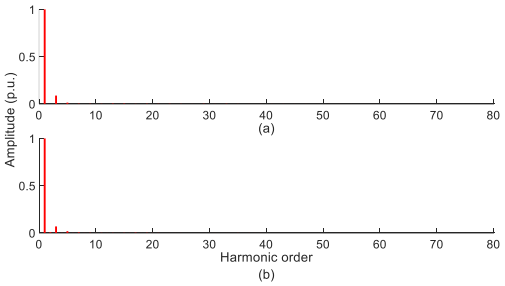


Figure 6.46: Harmonics in the output current for a 9-level CHB-MLI (a) PS-PWM (b) modified-WPWM

Numerical values of voltage and current THD are shown in Tables 5.4 and 5.5, respectively. Both methods' voltage and current THD are compared graphically in Figure 6.47 and Figure 6.48.

Table 6.6.4: Harmonics in the output voltage for the CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM.

	PS-PWM THD (%)	**Modified-WPWM THD (%)**
5-Level	32.22	22.02
7-Level	21.71	17.54
9-Level	18.69	15.87

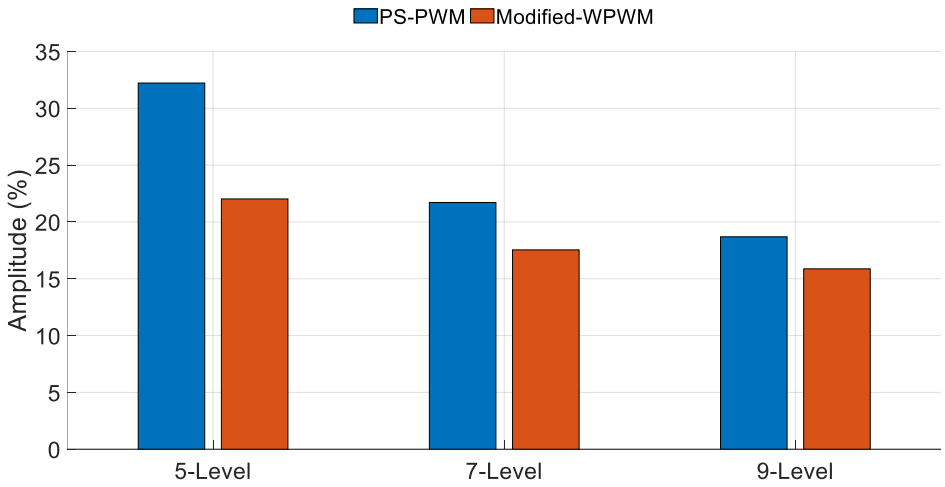


Figure 6.47: The comparison of voltage harmonics for 5, 7, and 9-level CHB-MLI for the PS-PWM and modified-WPWM.

Table 6.6.5: Harmonics in the output current for the CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM.

	PS-PWM THD (%)	**Modified-WPWM THD (%)**
5-Level	13.11	12.00
7-Level	10.90	10.59
9-Level	9.81	9.50

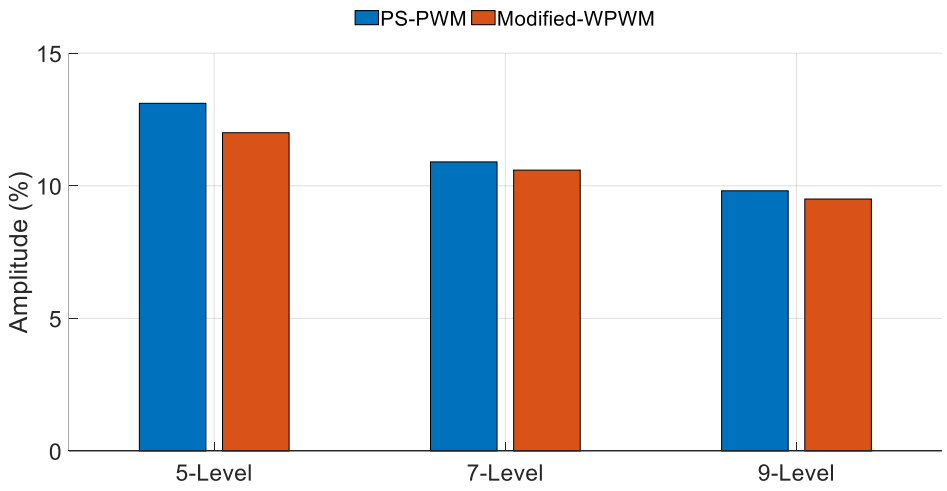


Figure 6.48: The comparison of current harmonics for 5, 7, and 9-level CHB-MLI for the PS-PWM and modified-WPWM.

The test was extended to demonstrate the discharging current of all sources for modified-WPWM and PS-PWM-based systems when supplying to the non-linear load. The results are matching for both techniques (Figure 6.49 to Figure 6.51). All sources have similar discharging percentages.

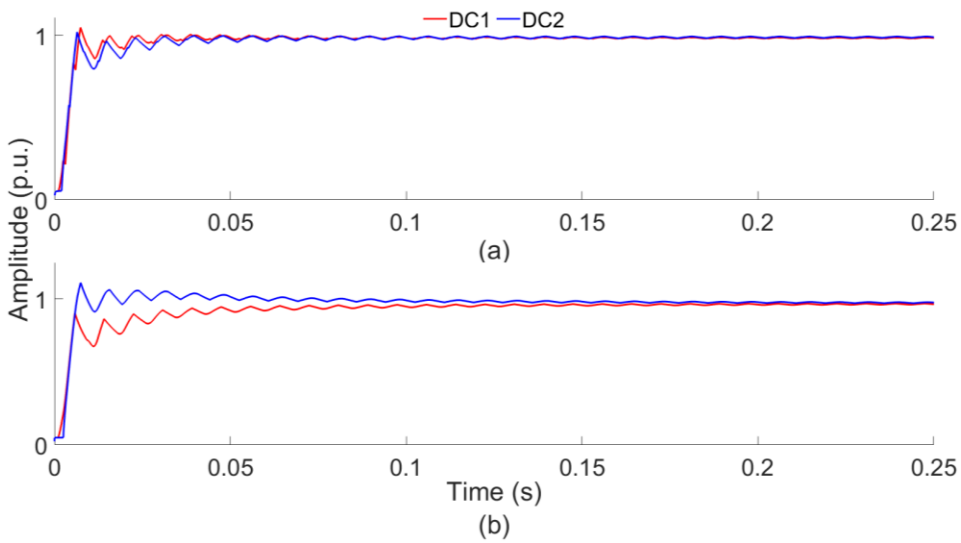


Figure 6.49: RMS value of discharging current of all sources in 5-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

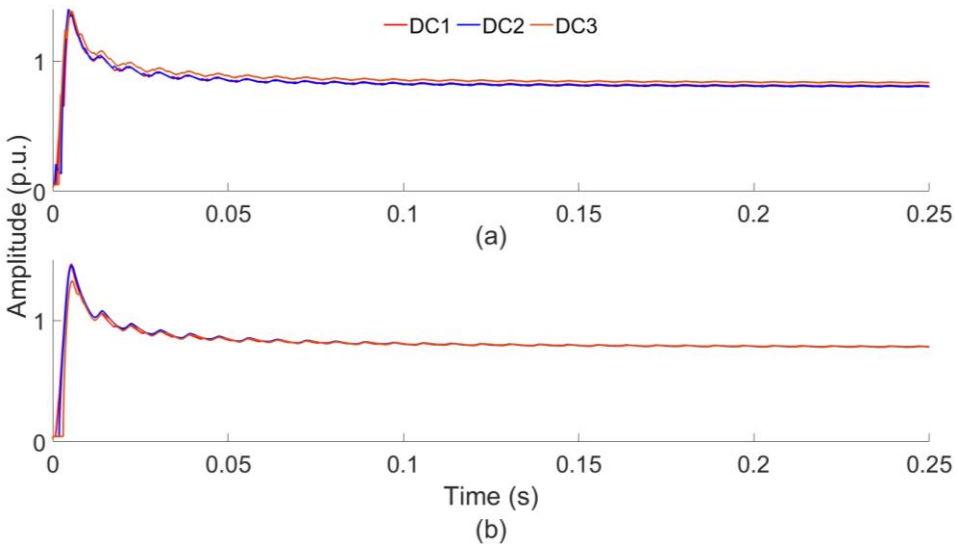


Figure 6.50: RMS value of discharging current of all sources in 7-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

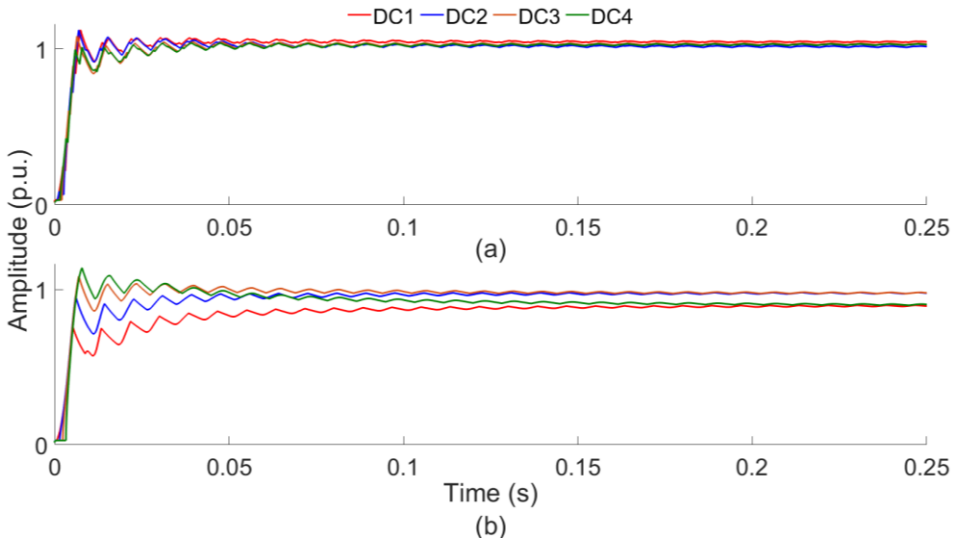


Figure 6.51: RMS value of discharging current of all sources in 9-level CHB-MLI using (a) PS-PWM and (b) modified-WPWM methods.

6.5 Harmonic analysis of modified-WPWM

This section analyzes the proposed strategy's 5th, 7th, 11th, 13th, and 17th harmonics. First, mathematical forms of these harmonics are presented.

Then, these harmonics are displayed graphically to compare with the PS-PWM technique.

6.5.1 Equations for the harmonic calculations

The 5th, 7th, 11th, 13th, and 17th harmonic equations are as follows:

5th harmonic:

$$V_{5^{th}} = b_n \sin(1885t) \quad (6\text{-}10)$$

Where: $b_n = \frac{4V_{dc}}{5\pi}[1 + \sum_{k=1}^{m}(-1)^k * \cos(5\alpha_k)]$

7th harmonic:

$$V_{7^{th}} = b_n \sin(2639t) \quad (6\text{-}11)$$

Where: $b_n = \frac{4V_{dc}}{7\pi}[1 + \sum_{k=1}^{m}(-1)^k * \cos(7\alpha_k)]$

11th harmonic:

$$V_{11^{th}} = b_n \sin(4147) \quad (6\text{-}12)$$

Where: $b_n = \frac{4V_{dc}}{11\pi}[1 + \sum_{k=1}^{m}(-1)^k * \cos(11\alpha_k)]$

13th harmonic:

$$V_{13^{th}} = b_n \sin(4901t) \quad (6\text{-}13)$$

Where: $b_n = \frac{4V_{dc}}{13\pi}[1 + \sum_{k=1}^{m}(-1)^k * \cos(13\alpha_k)]$

17th harmonic:

$$V_{17^{th}} = b_n \sin(6409t) \quad (6\text{-}14)$$

Where: $b_n = \frac{4V_{dc}}{17\pi}[1 + \sum_{k=1}^{m}(-1)^k * \cos(17\alpha_k)]$

where $\alpha1 < \alpha2 < \alpha3 < \cdots < \pi/2$.

6.5.2 Comparison of the harmonics

The PS-PWM and modified-WPWN techniques are diverse; therefore, it is challenging to compare the. PS-PWN technique is highly utilized; consequently, it is selected as a benchmark technique.

6.5.2.1 PS-PWN technique.

Figure 5.52(a) demonstrates the fundamental component and THD(%) and Figure 5.52(b) illustrates individual harmonic's amplitude in the output signal regarding variable modulation index, when PS-PWM technique is applied. The Figure 6.52(a) shows when modulation index is 0.1, the fundamental component is 8.03 and THD% is 250%, which significantly improves when higher value of modulation index is selected. Graph indicates when modulation index equals 1.0, the fundamental component value is 94.20% and % THD is 28.12%. Figure 6.52(b) shows that the 11th and 13th harmonics consume the highest energy among the other harmonics. These harmonics begin from very high and slowly decrease till the modulation index becomes 0.6, though they still have the highest energy peak among the other harmonic signals. when the modulation index is more significant than 0.6, the 7th harmonic start increasing, and modulation index crosses the value 0.9, the 7th and 17th harmonic consume the highest energy among all the harmonics.

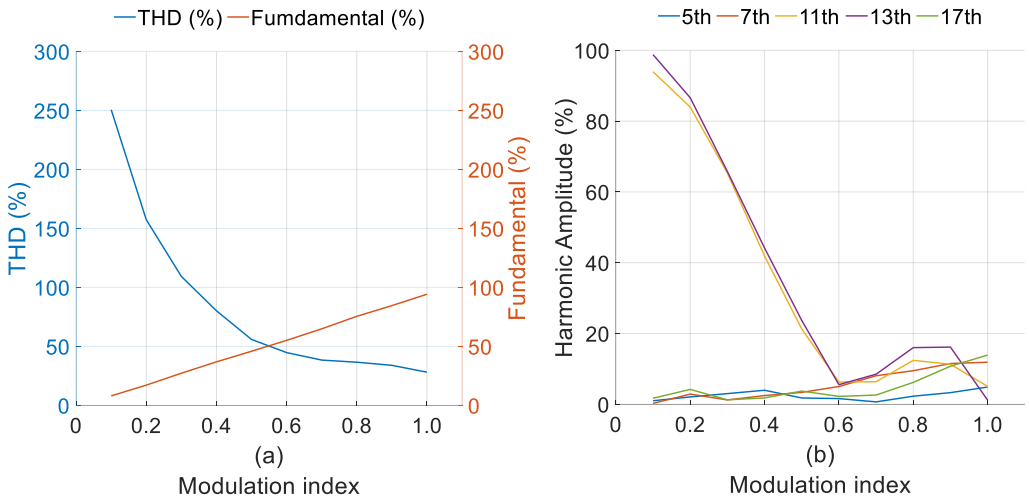


Figure 6.52: PS-PWM Harmonic analysis

6.5.2.2 Modified-WPWM scheme.

This section evaluates the fundamental component, THD, and the individual (5th, 7th, 11th, 13th, and 17th) harmonic amplitude concerning the scaling parameter and control variable for modified-WPWM. Figure 6.53(a) shows the fundamental component with the corresponding THD percentage, and Figure 6.53(b) displays the harmonic amplitude of the specific harmonics (5th, 7th, 11th, 13th, and 17th) generated in the output signal regarding various values of control variable when j=1 (scaling parameter). Similarly, Figure 6.53, Figure 6.54, Figure 6.55, Figure 6.56, Figure 6.57, Figure 6.58, Figure 6.59, Figure 6.60, Figure 6.61, and Figure 6.62 present a graph of fundamental components with corresponding THD percentages and a graph of harmonic amplitude of the specific harmonics regarding various values of control variable when j=2, j=3, j=4, j=5, j=6, j=7, j=8, j=9, and j=10 respectively.

Figure 6.53 presents the output obtained when the selected value of the scaling parameter, j=1. For this applied condition, Figure 6.53(a) illustrates the fundamental component starting from 57.15% and significantly increasing regarding the increase in the control variable's value. Also, the THD percentage is high (56.23%) at the beginning and decreases significantly with the control variable's value. Furthermore, when the control variable's value is 1.0, the fundamental component is 76.71%, and THD is 43.55%. Figure 6.53(b) displays that the 11th harmonic consumes the highest energy among the other harmonics. Harmonic amplitude (%) for the fifth harmonic is almost zero. 17th harmonic accounted for the second highest loss in energy, followed by the 13th and 7th harmonic in decreasing order.

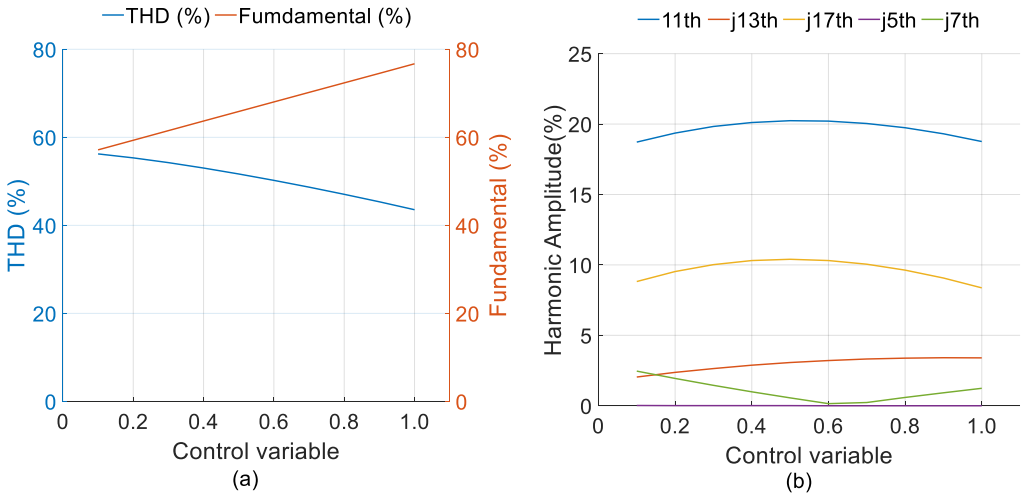


Figure 6.53: Modified-WPWM Harmonic analysis when j=1

Figure 6.54 demonstrates the condition when the value of the scaling parameter, j=2. For this applied condition, the fundamental component starts from 77.76% when the control variable's value is 0.1 and increases to 87.58%

when the control variable's value is 1.0. Also, THD percent noticeably decreases from 42.66% to 33.58% when the control variable's value varies from 0.1 to 1.0, respectively. Figure 6.54(b) shows that the 11th harmonic consumes the highest energy. The harmonic amplitude percentage shows a noticeable decreasing tendency regarding the control variable's value except for some distortion between values 0.3 and 0.4. Other individual harmonics follow an almost similar energy loss trend discussed in condition 1.

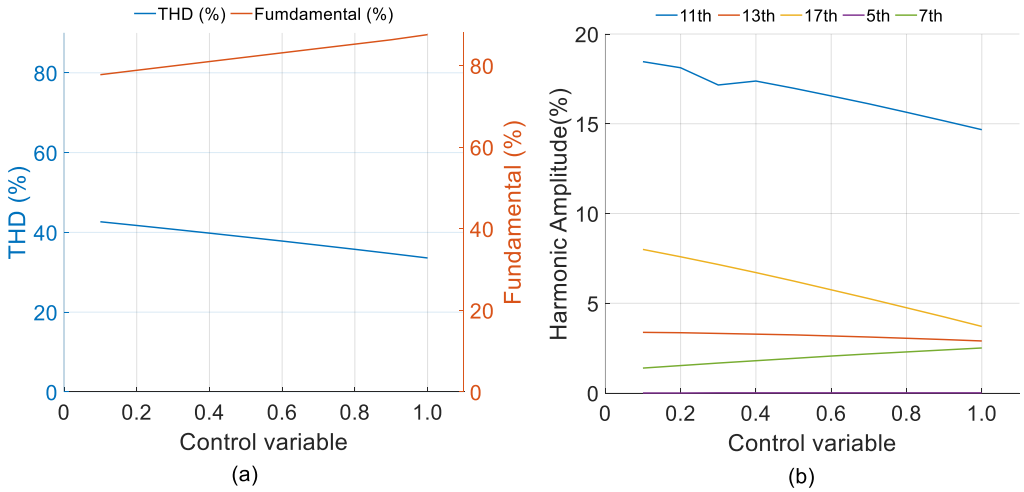


Figure 6.54: Modified-WPWM Harmonic analysis when j=2

Figure 6.55 presents the condition when the value of the scaling parameter, j=3. Here, the fundamental component ranges from 87.92% to 92.68%, and THD (%) varies from 33.02% to 27.65% when control variable varies from 0.1 to 1.0, respectively. Similar to Figure 6.54(b), Figure 6.55(b) also shows a gradual decrease in the harmonic amplitude percentage for the 11th harmonic except for some distortion between values 0.3 and 0.4. However, under this condition, energy loss accounted for 17th harmonic decreases (reaches

almost zero when the control variable value is 0.9), and energy consumption for the seventh harmonic increases significantly compared to conditions 1 & 2.

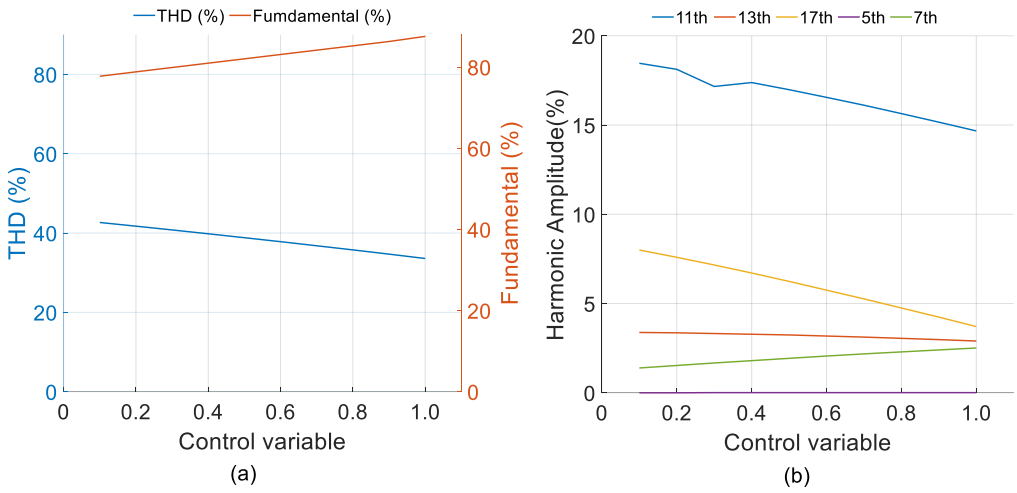


Figure 6.55: Modified-WPWM Harmonic analysis when j=3

Figure 6.56 represents the condition when the scaling parameter j=4 is selected. Here, the fundamental component varies from 92.94% to 95.31%, and THD (%) changes from 27.33% to 24.29% when the control variable goes from 0.1 to 1.0, respectively. Again, the energy consumption is highest in the 11th harmonic. Compared to condition 3, when condition four is applied, the 17th harmonic shows a slow increase in the amplitude percentage. At the same time, the 7th and 13th harmonic energy loss remains constant with changes in control variable value.

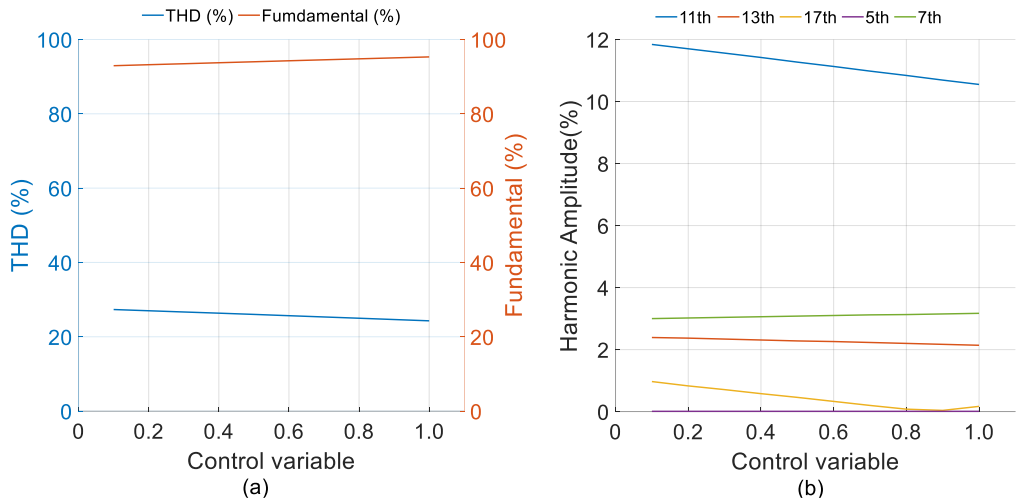


Figure 6.56: Modified-WPWM Harmonic analysis when j=4

Figure 6.57 defines the condition when the scaling parameter j=5 is assigned. The fundamental component increases by 1.18%, and the THD(%) decreases by 1.65%, concerning an increase in the control variable value. As per Figure 6.57(b), the highest energy consumption by the 11th harmonic follows the same decreasing tendency when the control variable value increases from 0.1 to 1.0. However, the change in energy consumption is significantly less (between 10.17% to 9.81%) compared to the above-applied conditions. Here, the amplitude percentage of the 7th and 13th harmonic remains almost constant with different control variable values except for an initial rise in energy consumption for the 13th harmonic (between control variable value of 0.1 and 0.2). The percentage amplitude of the 17th harmonic shows a slight increase with the rise in the control variable value.

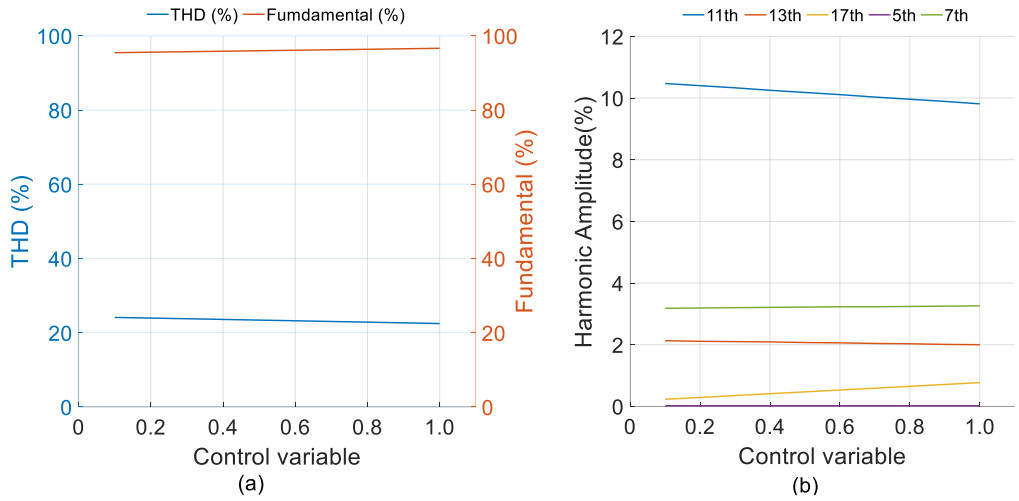


Figure 6.57: Modified-WPWM Harmonic analysis when j=5

Figure 6.58 defines the condition when the scaling parameter j=6. It demonstrated a slight increase in the fundamental component value and a slight decrease in THD (%), with an increase in the control variable's value. As per the trend, amplitude of the 11th harmonic is highest, and it shows a slight decrease with an increased control variable value. However, energy loss accounted for the 7th, 13th, and 17th harmonic remains almost constant over the range of different values of the control variable.

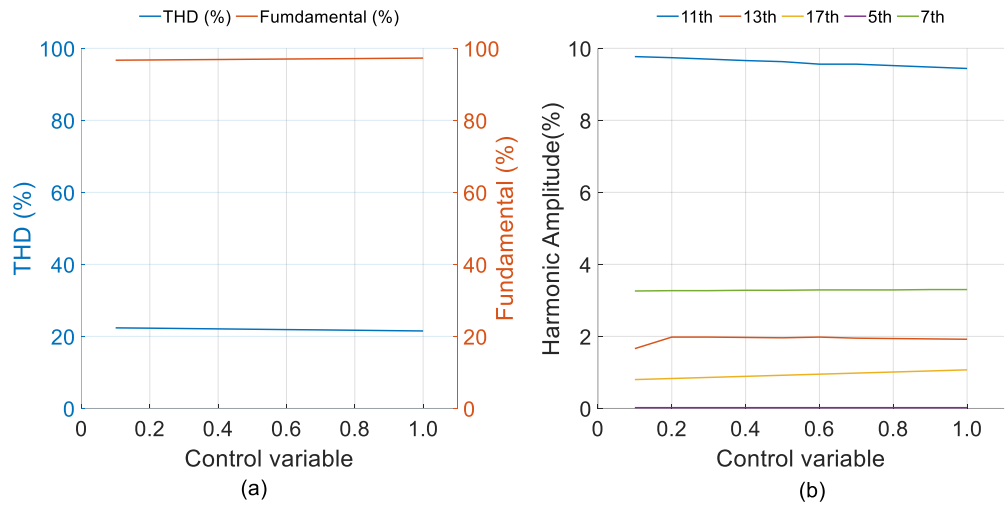


Figure 6.58: Modified-WPWM Harmonic analysis when j=6

As shown in Figure 6.59, Figure 6.60, Figure 6.61, and Figure 6.62, when the value of the scaling parameter rises from 7 to 10, there is a slight increase in the fundamental component and a fine reduction in THD (%). When j= 7, the fundamental component increases from 97.32 % to 97.62 %, and THD (%) decreases from 21.45 % to 21.01 % with increasing the control variable's value from 0.1 to 1.0. Similarly, the fundamental component shows improvement from 97.63 to 97.78 (THD 20.98 % to 20.76 %), 97.78 to 97.86 (THD 20.75 to 20.64), and 97.87 to 97.90 (THD 20.62 % to 20.57%) over the selected range of control variable values when j=8, j=9, and j=10, respectively. Also, all applied conditions have no significant effect on the trend of specific harmonic amplitude (%) when the scaling parameter value is between 7 to 10.

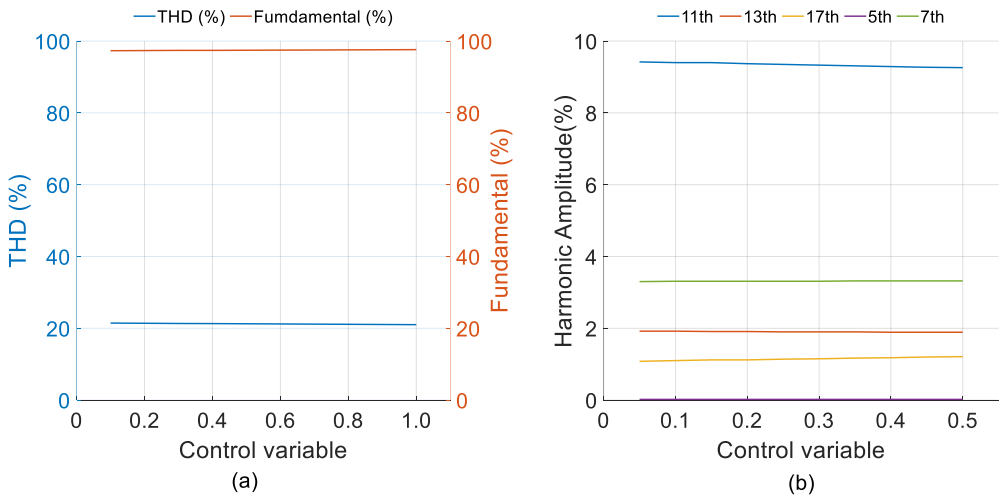


Figure 6.59: Modified-WPWM Harmonic analysis when j=7

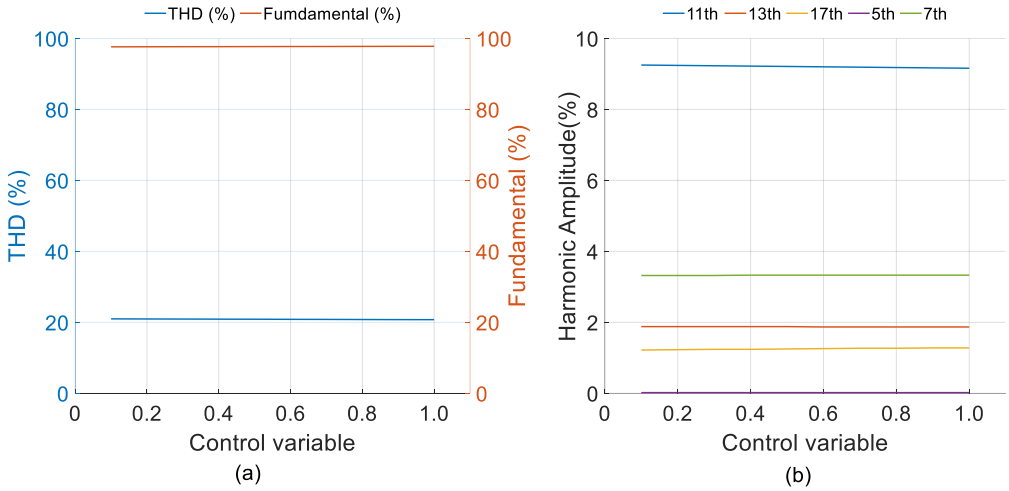


Figure 6.60: Modified-WPWM Harmonic analysis when j=8

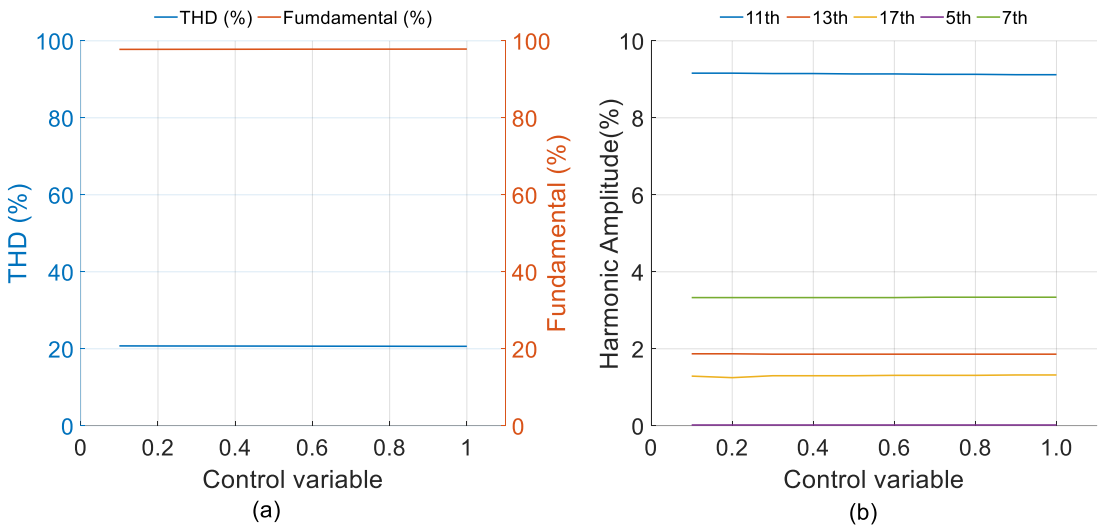


Figure 6.61: Modified-WPWM Harmonic analysis when j=9

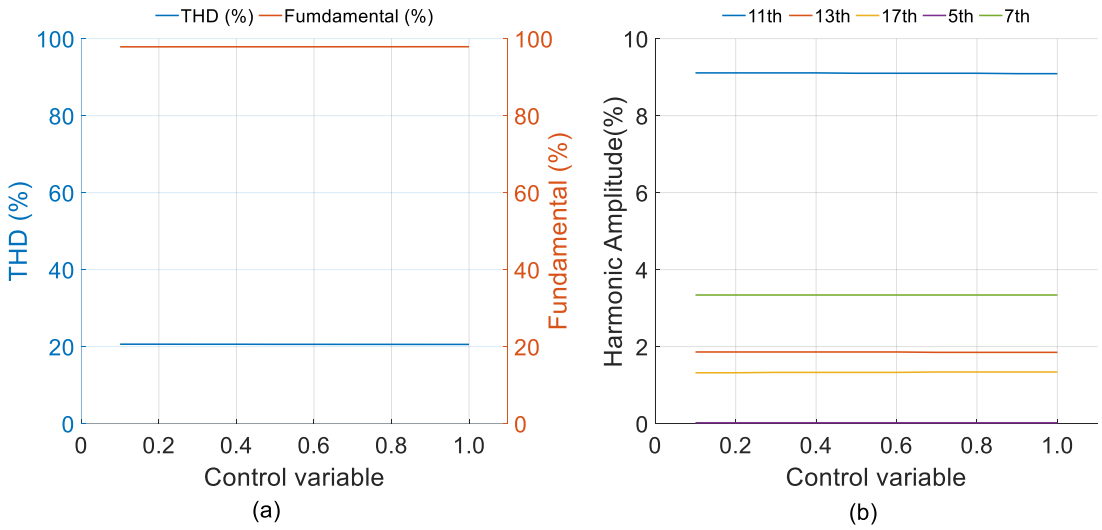


Figure 6.62: Modified-WPWM Harmonic analysis when j=10

6.6 Simulation and results of 3-phase modified-WPWM

The previous section shows the simulation study of a modified-WPWM technique for a single-phase CHB-MLI. In the previous study, the proposed method was simulated for the different levels of CHB-MLI and tested with a variety of loads.

In this section, the modified-WPWM technique is simulated with the 3-phase CHB-MLI as the 3-phase system delivers more power than the single-phase system. For this study, 3-phase 5-level CHB-MLI is considered to supply resistive, resistive/inductive, and non-linear loads.

6.6.1 Simulation study with resistive load

The MATLAB Simulink is used to simulate a modified-WPWM technique for a 3-phase 5-level CHB-MLI. The six H-bridge power cells are connected to the 100 V isolated DC sources. This converter is suppling to the Y-connected resistive load. This simulation study is performed to explore the open-loop steady-state performance of the 3-phase modified-WPWM technique for CHB-MLI when supplying a linear load. The results of the proposed method are compared with the PS-PWM technique for validation. The 3-phase line to line voltages ($V_{ab}(t), V_{bc}(t), V_{ca}(t)$) and currents ($I_a(t), I_b(t), I_c(t)$) are measured for the resistive load, which is shown as per unit (p.u.) in Figure 6.63 and Figure 6.64.

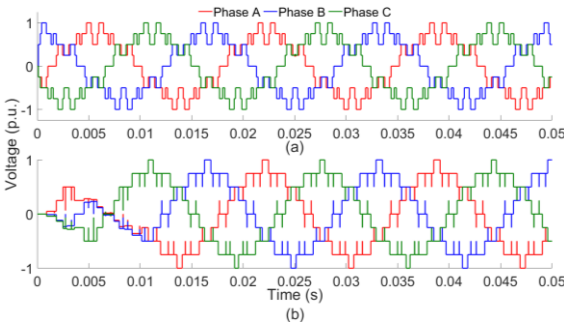


Figure 6.63: Line to line voltage for a 3-phase CHB-MLI with R load (a) PS-PWM (b) modified-WPWM

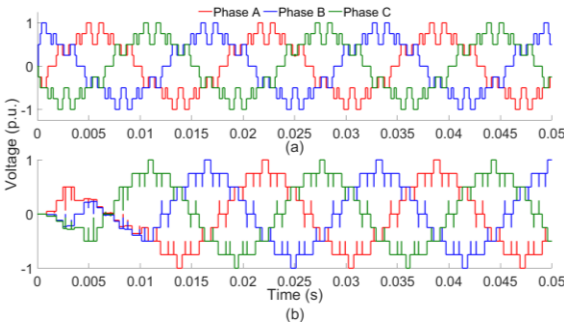


Figure 6.64: Line current for a 3-phase CHB-MLI with R load (a) PS-PWM (b) modified-WPWM

Figure 6.65 and Figure 6.66 show the harmonic spectrum of line to line voltage and line current for the PS-PWM and modified-WPWM techniques for the 5-level CHB-MLI. The comparison of voltage and current THD for both modulation techniques is shown in Figure 6.67. The proposed method produces lower THD as compare with the PS-PWM technique. Hence, the modified-WPWM improves the quality of the output signal, which indicates the reduction of energy loss in the harmonics.

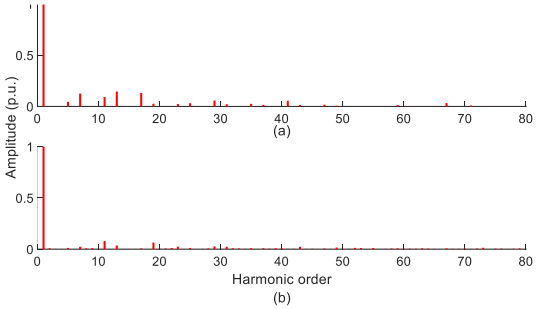


Figure 6.65: Harmonics in the line-to-line voltage for a 3-phase CHB-MLI with R load (a) PS-PWM (b) modified-WPWM

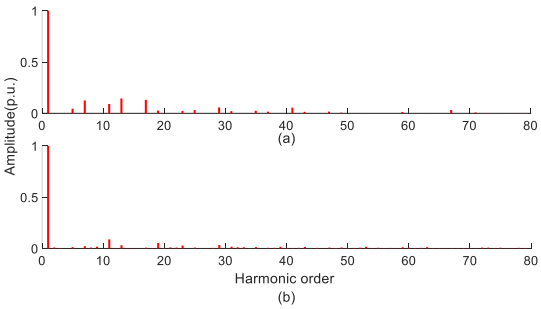


Figure 6.66: Harmonics in the line current for a 3-phase CHB-MLI with R load (a) PS-PWM (b) modified-WPWM

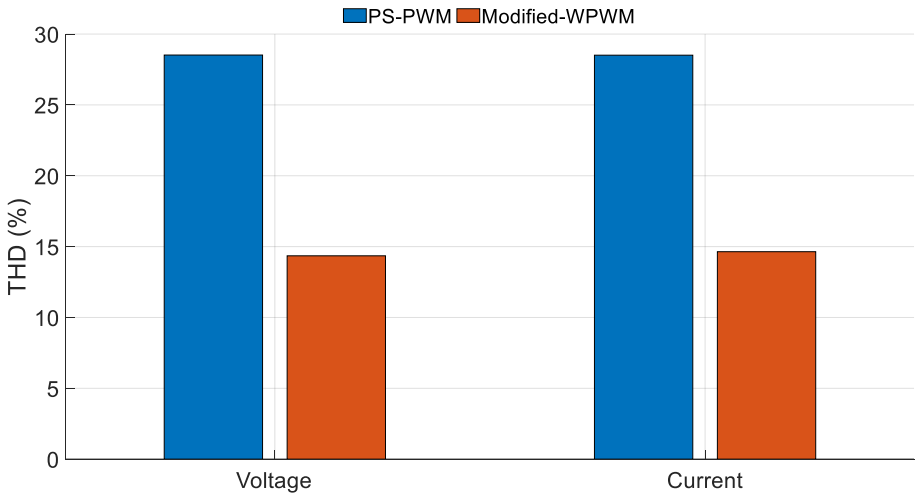


Figure 6.67: The comparison of voltage and current harmonics for the R load

The source balancing capability of the proposed method is also tested in Simulink by measuring the RMS current of each input DC source. The result of the proposed method compared with the results of the PS-PWM technique for validation is shown in Figure 6.68. The results show that the source balancing method can be avoided, that reducing the converter's complexity.

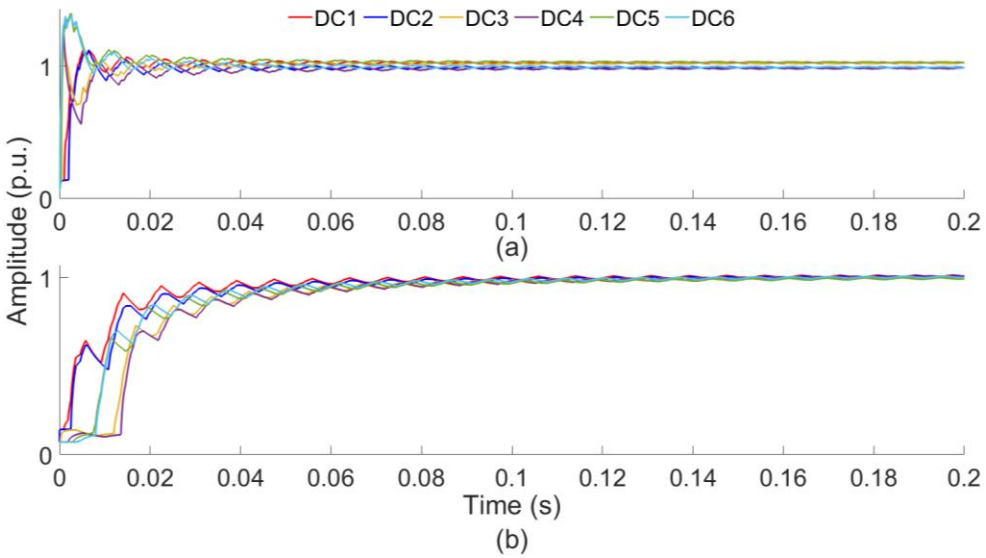


Figure 6.68: RMS value of discharging current of all sources in 3-phase CHB-MLI with R load (a) PS-PWM and (b) modified-WPWM methods

6.6.2 Simulation study with R-L load

The simulation study of the modified-WPWM technique for CHB-MLI is carried out by connecting an R-L load of an impedance of (8+j1.15) kΩ towards the converter's output. This study was performed to evaluate the steady-state performance in the open-loop condition when supplying to the R-L load. The measured line to line voltages (($V_{ab}(t), V_{bc}(t), V_{ca}(t)$) and currents ($I_a(t), I_b(t), I_c(t)$) are shown in Figure 6.69 and Figure 6.70 respectively.

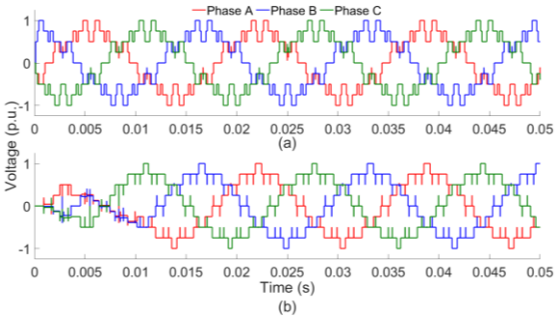


Figure 6.69: Line to line voltage for a 3-phase CHB-MLI with R-L load (a) PS-PWM (b) modified-WPWM

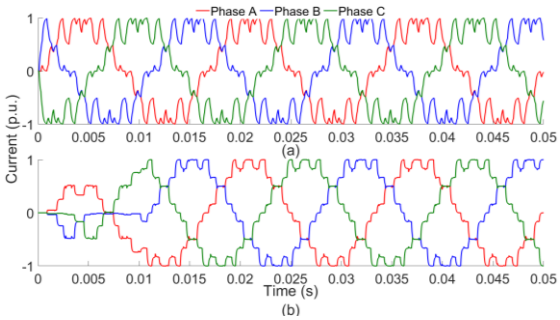


Figure 6.70: Line current for a 3-phase CHB-MLI with R-L load (a) PS-PWM (b) modified-WPWM

The harmonics also measured in the line to line voltage and line current using FFT built-in function in Simulink. The harmonic spectrum of output voltage and current for PS-PWM and modified-WPWM techniques are shown in Figure 6.71 and Figure 6.72. Also, the comparison of harmonics generated by the PS-PWM method and modified-WPWM method is shown in Figure 6.73. The harmonics generated by the modified-WPWM technique have lower amplitude, leading to lower voltage and current THDs in the output signal. Therefore, the proposed method can reduce the filtering process. Here the size and cost of the converter can be reduced.

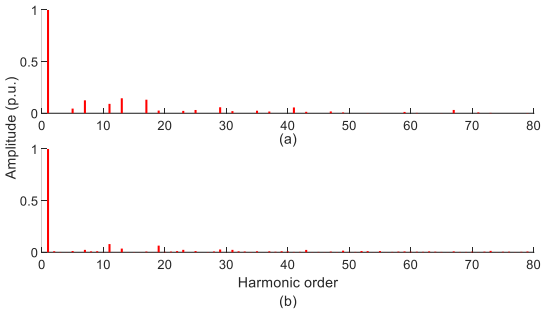


Figure 6.71: Harmonics in the line-to-line voltage for a 3-phase CHB-MLI with R-L load (a) PS-PWM (b) modified-WPWM

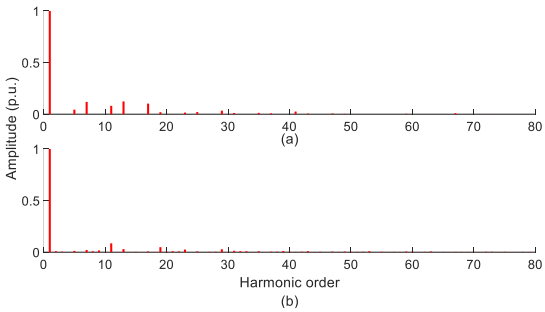


Figure 6.72: Harmonics in the line current for a 3-phase CHB-MLI with R-L load (a) PS-PWM (b) modified-WPWM

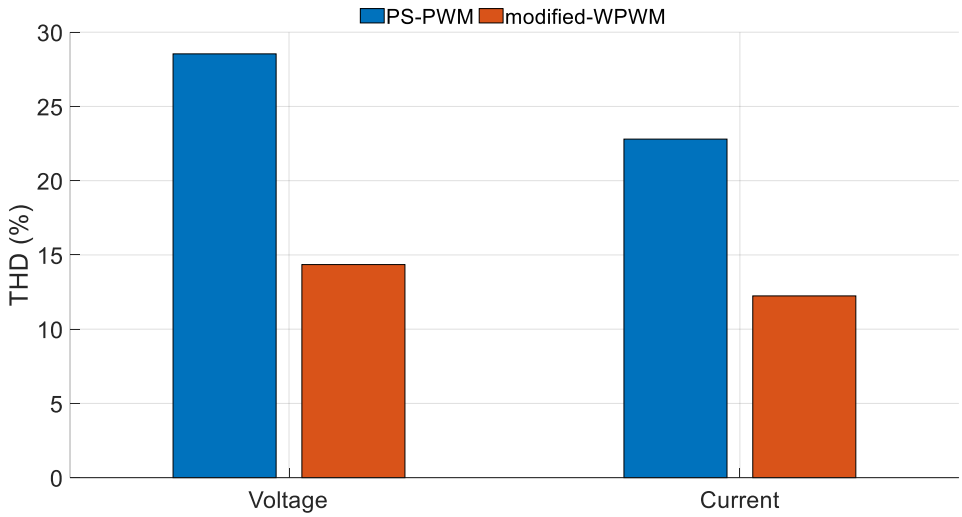


Figure 6.73: The comparison of voltage and current harmonics for the R-L load

The source balancing capability of the proposed method is also tested in Simulink when the converter is supplying to the inductive load. In this test, the supply current of each source is measured as RMS current. The proposed method's results are compared with the PS-PWM technique's results for validation is shown in Figure 6.74. The results show that the source balancing

method can be prevented. Therefore, the converter's control system complexity can be reduced.

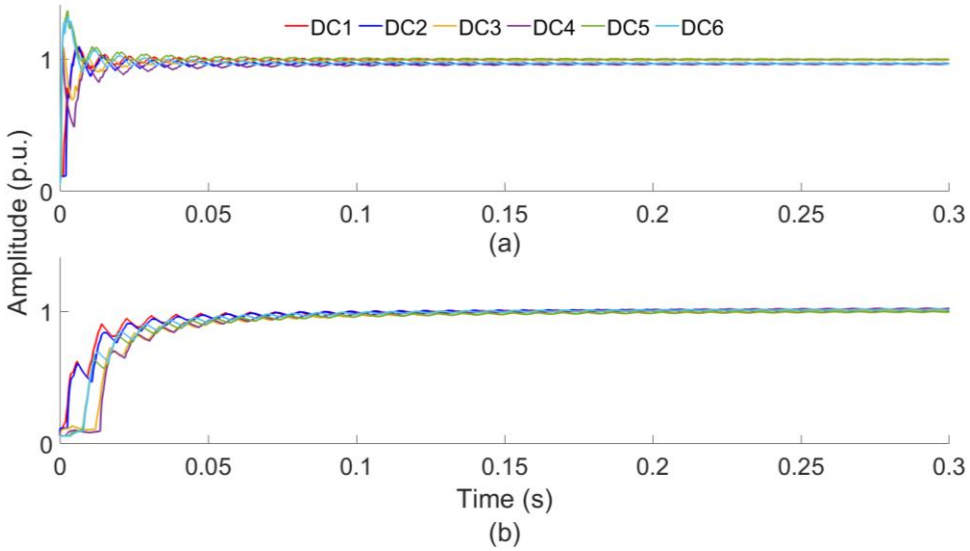


Figure 6.74: RMS value of discharging current of all sources in 3-phase CHB-MLI with R-L load (a) PS-PWM and (b) modified-WPWM methods

6.6.3 Simulation study with non-linear load (a diode rectifier)

This test is performed to examine the functioning of the converter in steady-state operation with the non-linear load. The converter switches are controlled using modified-WPWM, and a 3-phase rectifier circuit is connected to 10 kΩ load. A similar system is made, which is controlled with the PS-PWM technique. Both systems' output results are compared to validate the performance of the modified-WPWM technique. The line to line voltages ($(V_{ab}(t), V_{bc}(t), V_{ca}(t))$ and currents $(I_a(t), I_b(t), I_c(t))$ are shown in Figure 6.75 and Figure 6.76.

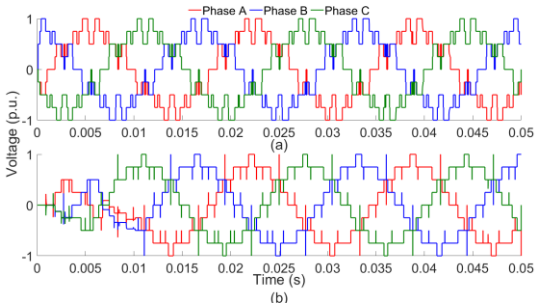


Figure 6.75: Line to line voltage for a 3-phase CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM

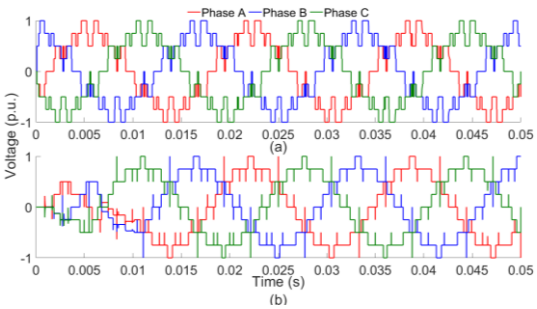


Figure 6.76: Line current for a 3-phase CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM

As a testing process, harmonics in the line to live voltage and line currents are measured using the FFT function in Simulink. Figure 6.77 and Figure 6.78 show the harmonic spectrum of output voltage and current for PS-PWM and modified-WPWM techniques. Also, the comparison of harmonics generated by the PS-PWM method and modified-WPWM method is shown in Figure 6.79. The harmonics generated by the modified-WPWM technique have smaller peaks as compared to the PS-PWM system.

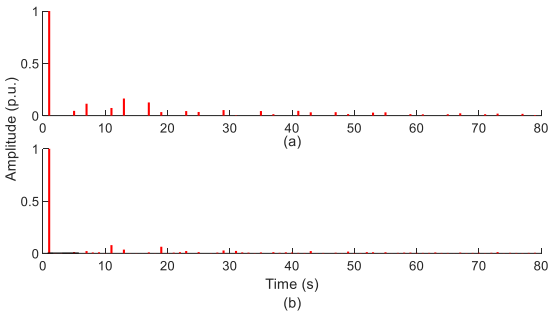


Figure 6.77: Harmonics in the line-to-line voltage for a 3-phase CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM

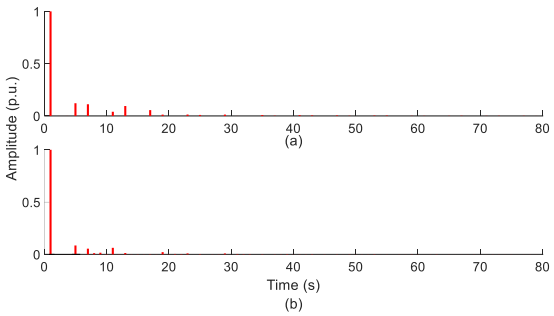


Figure 6.78: Harmonics in the line current for a 3-phase CHB-MLI with non-linear load (a) PS-PWM (b) modified-WPWM

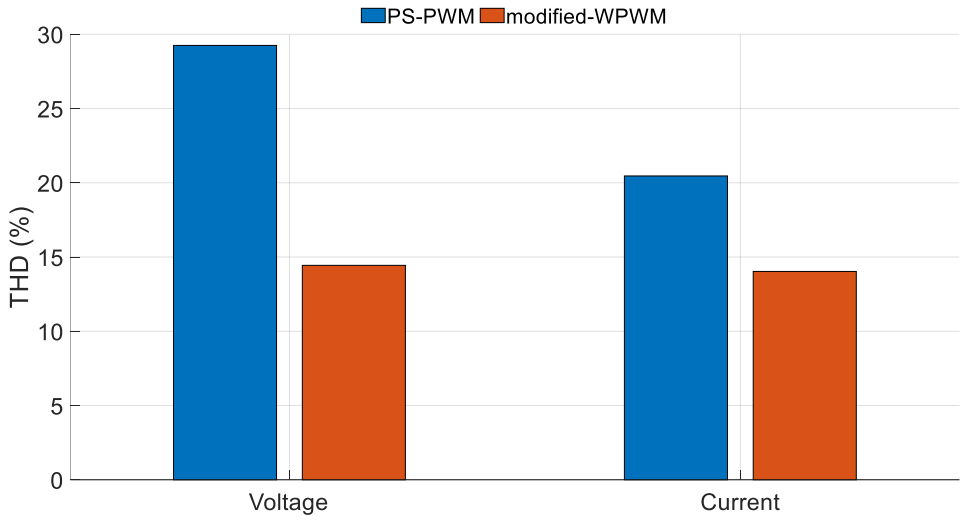


Figure 6.79: The comparison of voltage and current harmonics for the non-linear load

The source current is also measured to test the balancing capability of the proposed method. In this test, the supply current of each source is measured as RMS current. The proposed method's results are compared with the PS-PWM technique's results for validation is shown in Figure 6.80. The results show that

the source balancing method can be prevented. Therefore, the converter's control system complexity can be reduced.

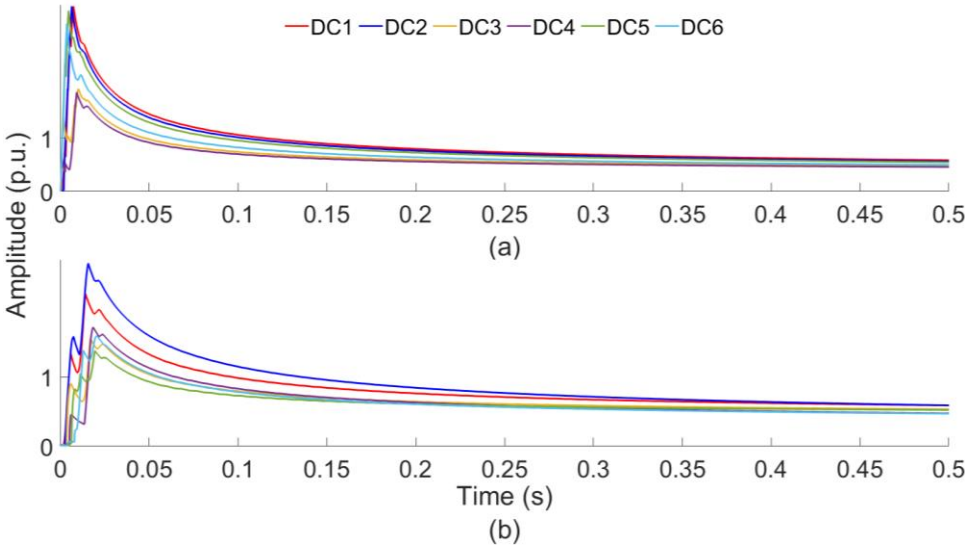


Figure 6.80: RMS value of discharging current of all sources in 3-phase CHB-MLI with non-linear load (a) PS-PWM and (b) modified-WPWM methods.

6.7 Summary

This chapter explained the implementation steps of the modified-WPWM technique. The modified-WPWM method was tested in MATLAB-Simulink with 1-phase and 3-phase 5-, 7-, and 9-level CHB-MLI. The output signal of each CHB-MLI configuration was analyzed with resistive, inductive, and non-linear loads. The analysis was carried out by comparing the measured fundamental component and THD in the output signal with a signal generated with a PS-PWM technique. Also, 5^{th}, , 7^{th} , 11^{th} , 13^{th} , and 17^{th} harmonics were analyzed. Furthermore, the load balancing capability of the proposed modulation technique was studied as well.

Chapter 7. PSPICE Simulation and Real Model

7.1 Introduction

The Modified-WPWM method was evaluated in the previous chapter using the MATLAB-Simulink model. The output of the proposed method was compared with the PS-PWM technique's results.

The proposed method is validated in this chapter using PSPICE simulation and actual hardware implementation. First, the proposed modulation technique and PS-PWM technique are applied to the PSPICE model of a 5-level CHB-MLI. This simulation study is the second step to validating the results of the proposed technique before evaluating it with actual hardware.

After that, the proposed method is evaluated with a single phase 5-level CHB-MLI hardware.

7.2 PSPICE model of PS-PWM technique

This model has four carriers (triangular) signals (Cr1 - Cr4), as required for the 5-level CHB-MLI. These carrier signals are 90-degree out of phase with each other. The sources V2, V3, V6, and V7, are the source of carrier signals, as shown in Figure 7.1. In this figure, fs is a carrier frequency. The initial peak is 0 V, peak during the ON period is 1 V. The pulse's rising and falling time is shown as T_{rise} and T_{fall}, respectively. The values of T_{rise} and T_{fall} are 0.5/fs second, and the pulse period (T_{period}) is 1/fs second.

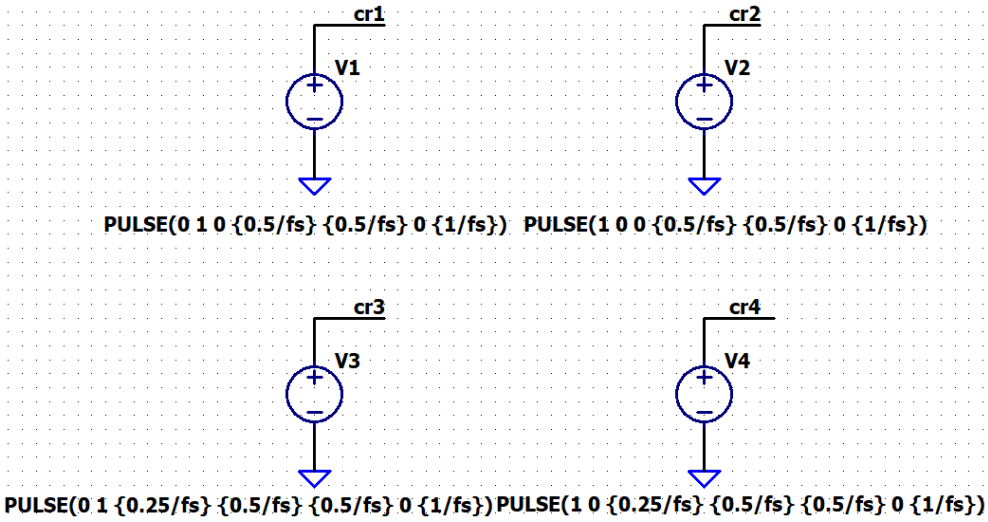


Figure 7.1: Carrier signal sources

The required sinusoidal reference signal is generated, as shown in Figure 7.2. The amplitude and DF offset of the signal are 0.5 V. the frequency of the signal is 60 Hz, and the signal starts at 270-degree.

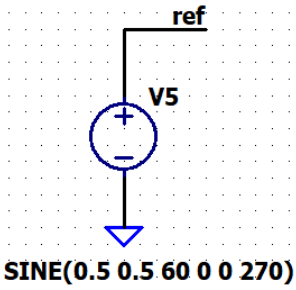


Figure 7.2: Sinusoidal signal generator

The carrier and reference signals are compared using behavioral voltage sources, as shown in Figure 7.3. When the amplitude of the reference signal is higher than the amplitude of the carrier signal, it generates an ON switching pulse of 1.5 V; otherwise, it stays in the OFF condition at 0 V.

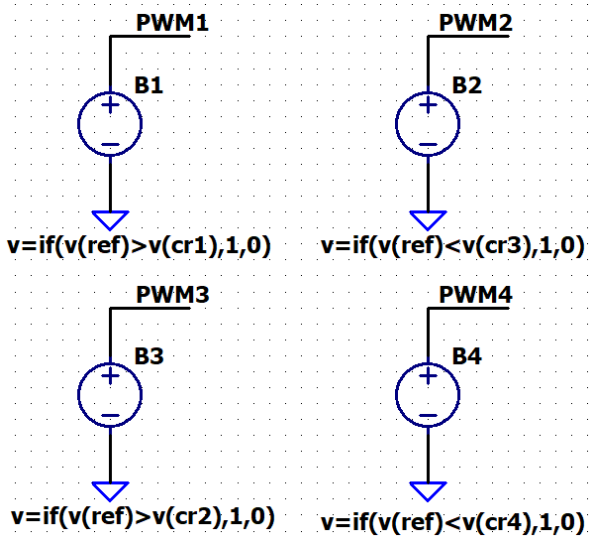


Figure 7.3: Signal comparators

The four carrier signals generated eight switching pulses. The four switching pulses are generated with the comparator, and the other four are complimentary and applied to the four gate drivers, LT1160.

7.3 PSPICE model of modified-WPWM technique

This model is simplified by using the pre-calculated values for the td1 and td2 to increase the simulation speed. These pre-calculated values are compared with a 60 Hz sawtooth signal using behavioral voltage sources as a comparator block.

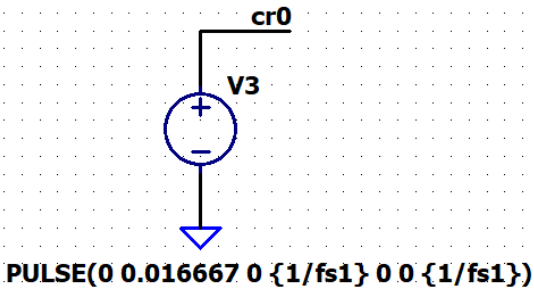


Figure 7.4: Counter block for the one cycle of 60 Hz signal

The sawtooth signal has a fundamental frequency, similar to the reference signal used in the PS-PWM technique. The peak voltage of this signal is 0.016667 V. The rise time (T_{rise}) and fall time (T_{fall}) are 1/fs s and 0 s, respectively. The T_{period} is 1/fs s. The value of fs is 60 Hz.

Like the PS-PWM technique, four switching pulses are generated with the comparator block, and the other four are opposite signals. All eight pulses are connected to the four gate driver circuits.

7.4 Testing of the gate pulse with LT1160 Gate driver

A single LT1160 can be used to control the half-bridge converter. It is integrated with two drive channels with separate inputs PWM1 and PWM2 in a half-bridge circuit for the top and bottom switches, respectively. Similarlly, it is integrated with two separate outputs, Tgate and Bgate for the top and bottom switches. This gate driver uses the principle of the bootstrap technique, which is helpful in a high-voltage gate driver. In this concept, when the bottom switch is turned ON and the top switch is turned OFF, the bootstrap capacitor (C1) charges through the diode D1, as shown in Figure 7.5. Also, when the bottom switch is turned OFF and the top switch is turned ON, the bootstrap capacitor discharges some of the reserved voltage to the top switch through pin seven and pin six of the gate driver. The datasheet for this gate driver is shown in the appendix.

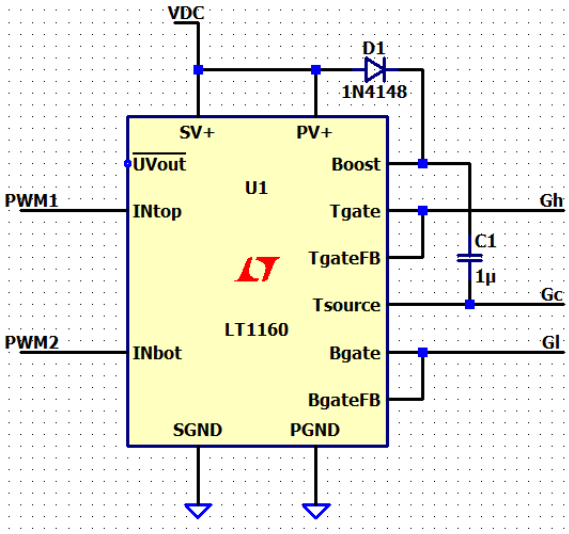


Figure 7.5: Gate driver IC

The selection/sizing of the bootstrap capacitor is crucial because it drives the top switch in the leg. Therefore, the capacitor charging and discharging is verified, since PS-PWM and modified-WPWM have variable width pulses. The charging and discharging of the bootstrap capacitor are shown in the Figure 7.6 and Figure 7.7 for the PS-PWM and modified-WPWM respectively. In both figures, red signal shown capacitor voltage, blue is a switching pulse for the top switch and purple signal represents the gate signal for the lower switch. The △V shows the rate of voltage flactuation in the capacitor charge during ON/OFF of the top switch. In the PS-PWM the voltage flactuates in between 11.55 V to 11.15 V and in the modified-WPWM 11.55 V to 11.20 V.

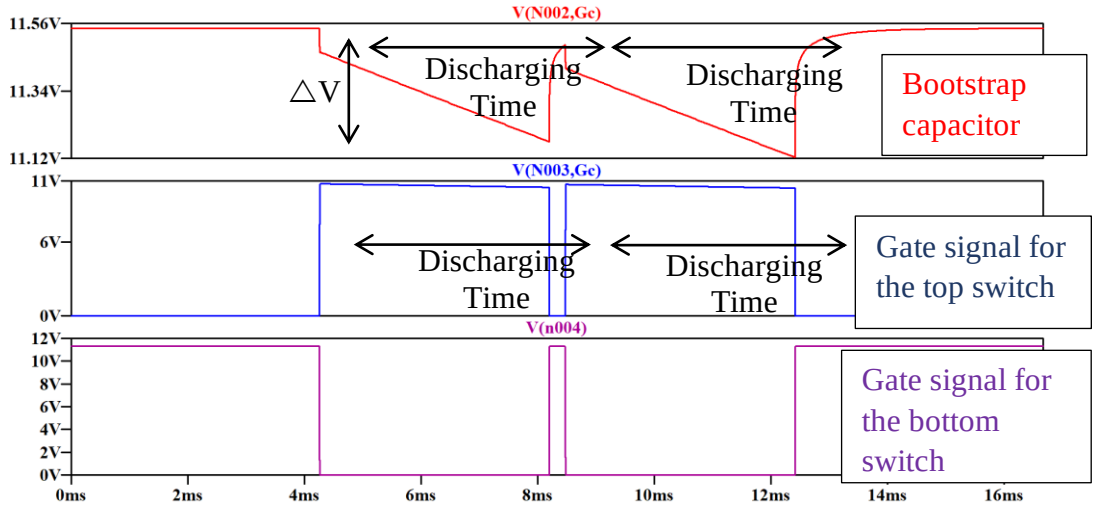


Figure 7.6: Boot-strap capacitor charging and dis-charging waveforms

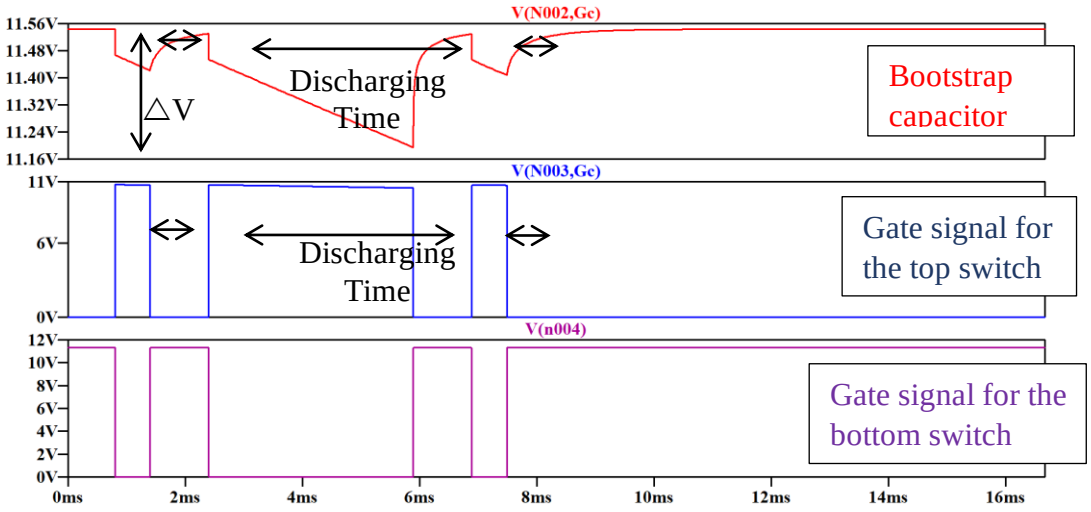


Figure 7.7: Boot-strap capacitor charging and dis-charging waveforms.

7.5 PSPICE Simulation results of the modified-WPWM methods

The PS-PWM method is used to operate CHB-MLI. As shown in Figure 7.8, this method can generate precise 5-levels and symmetry in both positive and negative half cycles. The peak-to-peak output voltage is measured at approximately 28 V.

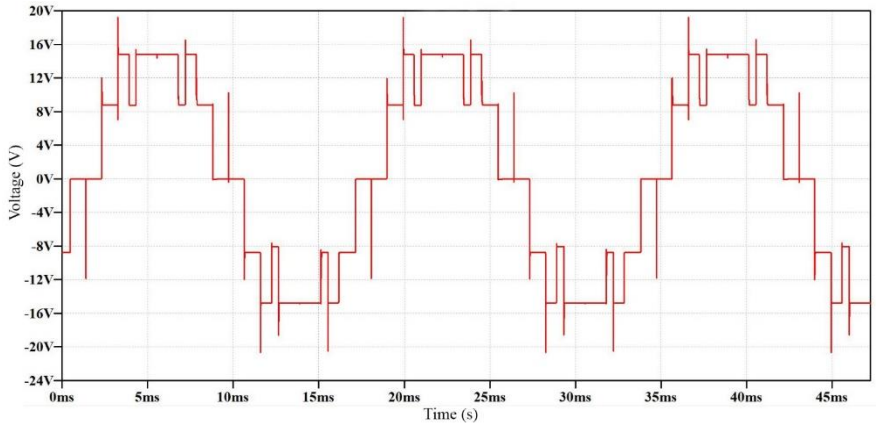


Figure 7.8: Voltage output of 5-level CHB-MLI using PS-PWM

The output voltage in Figure 7.9 was achieved using the modified-WPWM method for the 5-level CHB-MLI. Like the PS-PWM method, this technique can generate precise 5-levels and symmetry in both positive and negative half cycles. The peak-to-peak output voltage is measured at approximately 28 V.

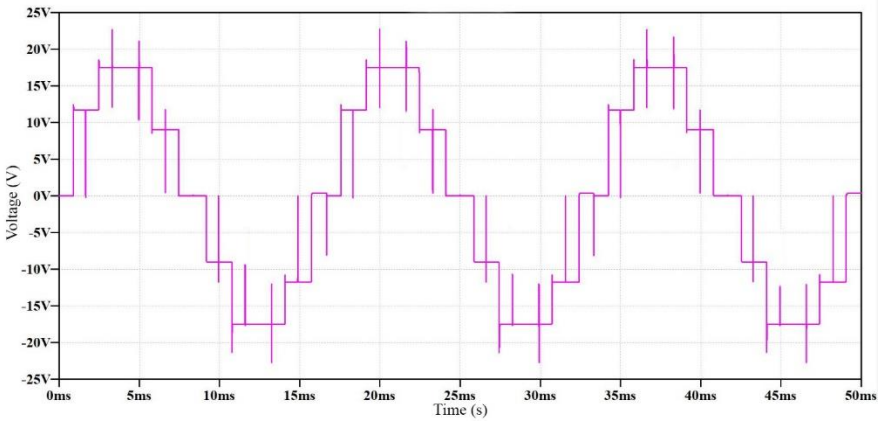


Figure 7.9: Voltage output of 5-level CHB-MLI using modified-WPWM.

Figure 7.10(a) demonstrates the fundamental component, and THD(%) and Figure 7.10(b) illustrate individual harmonic amplitude in the output signal regarding variable modulation index when the PS-PWM technique is applied. Figure 7.10(a) shows that when the modulation index is 0.1, the fundamental

component is 8.03, and THD% is 250%, which significantly improves when a higher value of the modulation index is selected. The graph indicates that when the modulation index equals 1.0, the fundamental component value is 94.20%, and % THD is 28.12%. Figure 7.10(b) shows that the 11th and 13th harmonics consume the highest energy among the other harmonics. These harmonics begin from very high and slowly decrease till the modulation index becomes 0.6, though they still have the highest energy peak among the other harmonic signals. When the modulation index is more significant than 0.6, the 7th harmonic start increasing, and the modulation index crosses the value of 0.9. The 7th and 17th harmonics consume the highest energy among all the harmonics.

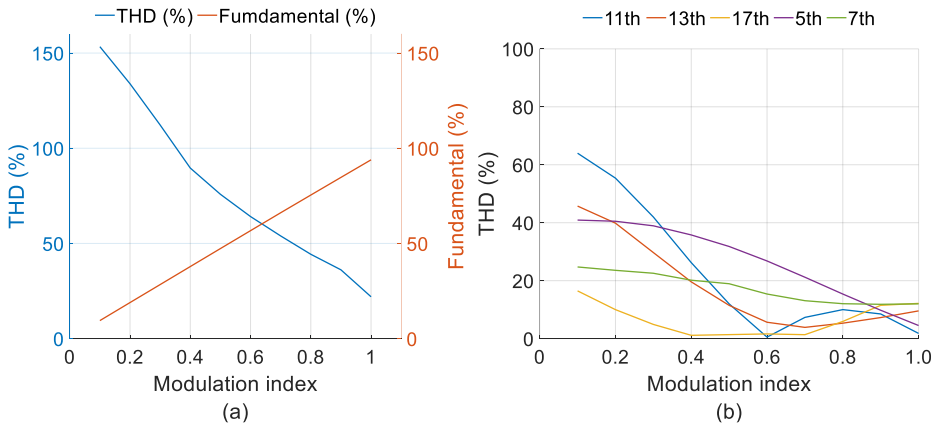


Figure 7.10: (a) fundamental component and THD(%) (b) anplitude of lower order harmonics

Figure 7.11(a) demonstrates the fundamental component, and THD (%) and Figure 7.11(b) illustrate individual harmonic amplitude in the output signal regarding variable scaling parameter value when the modified-WPWM technique is applied. Figure 7.11(a) shows that when the value of the scaling parameter is 1, the fundamental component is 40%, and THD% is 55.43%, which significantly

improves when a higher value of the scaling parameter is selected. The graph indicates that when the scaling parameter value is 10, the fundamental component value is 98.30%, and % THD is 17.25%. Figure 7.11(b) shows that the 11th and 17th harmonics consume the highest energy among the other harmonics. These harmonics begin from very high and slowly decrease, though they still have the highest energy peak among the other harmonic signals.

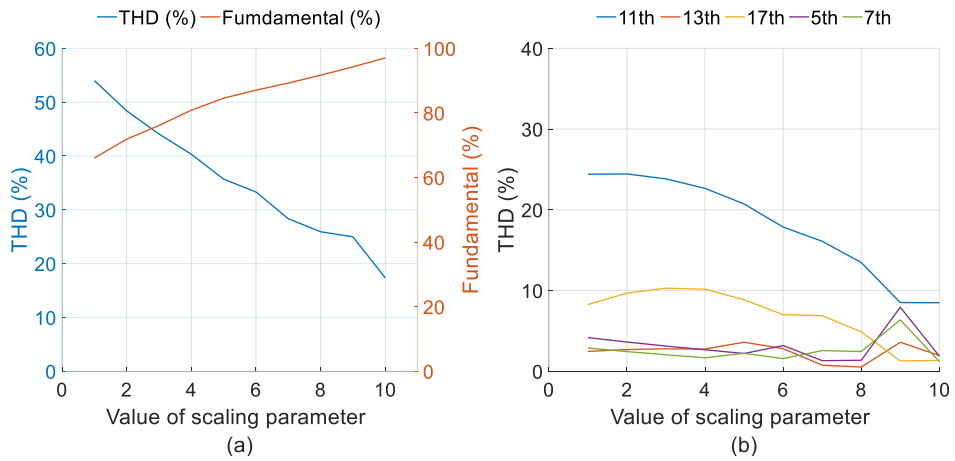


Figure 7.11: (a) fundamental component and THD(%) (b) anplitude of lower order harmonics

7.6 Experimental setup and results

In the previous sections, the Modified-WPWM method has been verified with the PSPICE model of 5-level CHB-MLI using LTSpice software. In this section, the experimental setup of 5-level CHB-MLI is used to test the modified-WPWM method, and the results are verified by comparing them with the PS-PWM method.

7.6.1 Experimental setup of 5-level CHB-MLI

The hardware setup shown in Figure 7.12, that consists of a transformer bank, AC/DC converter, H-bridge driver circuit, H-bridge power module, load, and digital controller.

The transformer bank consists of four 120 V/12 V step-down transformers to supply 12 V AC to the four rectifier circuits. The rectifier circuit converts the 12 V AC supply to the 12 V DC supply. These four isolated DC supplies are connected to the two power modules, and the other two are supplied to the driver circuit. The driver circuit consists of two main components, the PC817 optocoupler, and IRS2004 driver IC. The PC817 is a four-pin IC isolates the digital controller from the power circuit. The IRS2004 can drive a half-bridge converter unit and can be used with 200 V DC. Also, it provides 520 ns of dead time between upper and lower switches. More details are provided in the appendix.

A Texas Instruments F28069 microcontroller is a digital controller that generates switching pulses for all the switches used in power modules. For the PS-PWM technique, pre-calculated values of 60 Hz sinusoidal signal are stored in a tabular form. The carrier signals are generated digitally; those are compared with stored values to generate switching pulses. The modified WPWM is implemented using a similar algorithm shown in Figure 6.1.

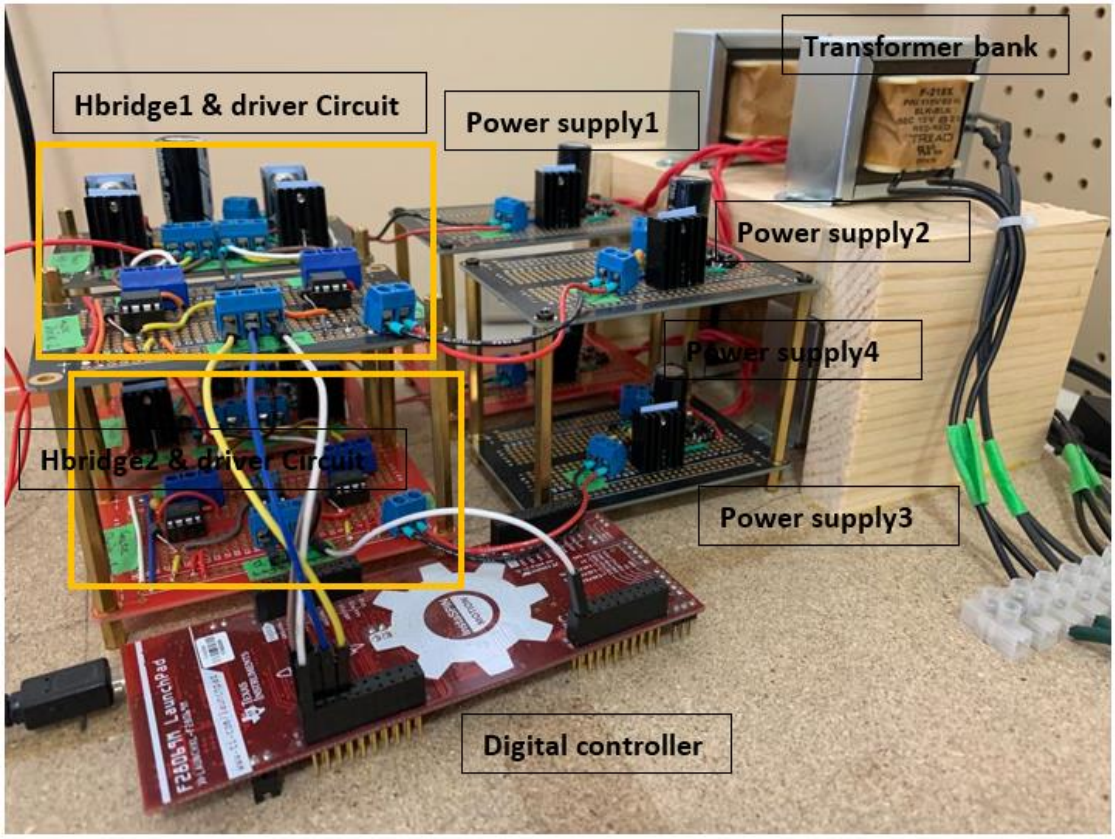


Figure 7.12: Experimental setup of 5-level CHB-MLI

7.6.2 Output voltage and harmonic spectrum of PS-PWM technique

This section shows the experimental results achieved for the 5-level 1-phase CHB-MLI when it is controlled using PS-PWM techniques. The 5-level CHB-MLI consists of two h-bridge power cells with equal DC sources. The 8 kΩ resistive load is connected at the output terminal. The switching frequency of each switch of the converter is 180 Hz, and the fundamental frequency is 60 Hz. The voltage THD is calculated manually using THD equation.

7.6.2.1 Case 1: m = 0.1

For the case, m = 0.1, output voltage and voltage harmonics are shown in Figure 7.13 and Figure 7.14 respectively. In this case, the converter can

generate three output voltage levels; the pick-to-pick voltage is measured at 12 V. Also, the THD of this converter is calculated as 194.63%.

The harmonic spectrum shows that the 11th and 13th harmonics have significantly high values**,** 106.6% of the fundamental component for both harmonics. In an experimental setup, some even number of harmonics are also observed.

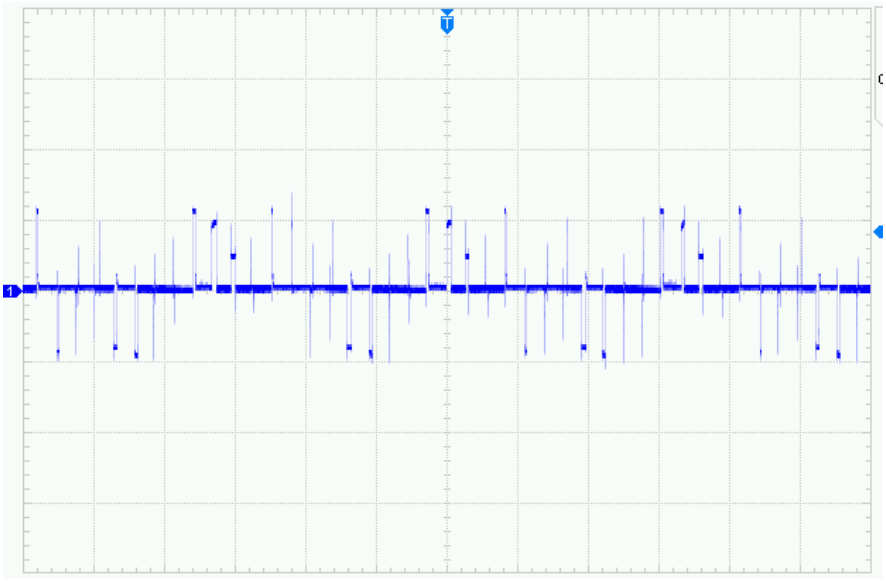


Figure 7.13: Output voltage m = 0.1

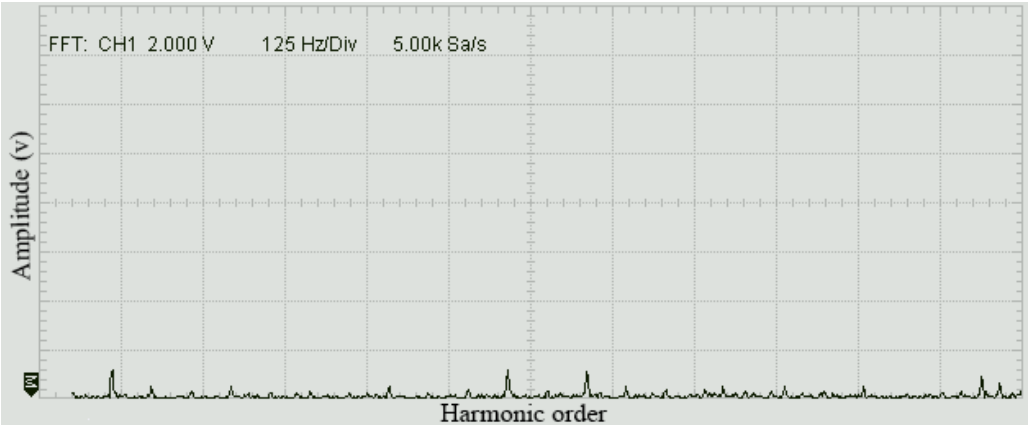


Figure 7.14: Harmonic spectrum when m = 0.1

7.6.2.2 Case 2: m = 0.2

For the case, m = 0.2, output voltage and voltage harmonics are shown in Figure 7.15 and Figure 7.16, respectively. Like case 1, in this case also, the converter can generate three levels in the output voltage; however, the peak-to-peak voltage is measured at 14 V. The THD of this converter is calculated as 187.01%.

Here, the harmonic spectrum shows that the 11th and 13th harmonics have a high value as compared to other individual harmonics, 95.56% of the fundamental component for both the harmonics. Also, in the experimental setup, small levels of some even harmonics are observed.

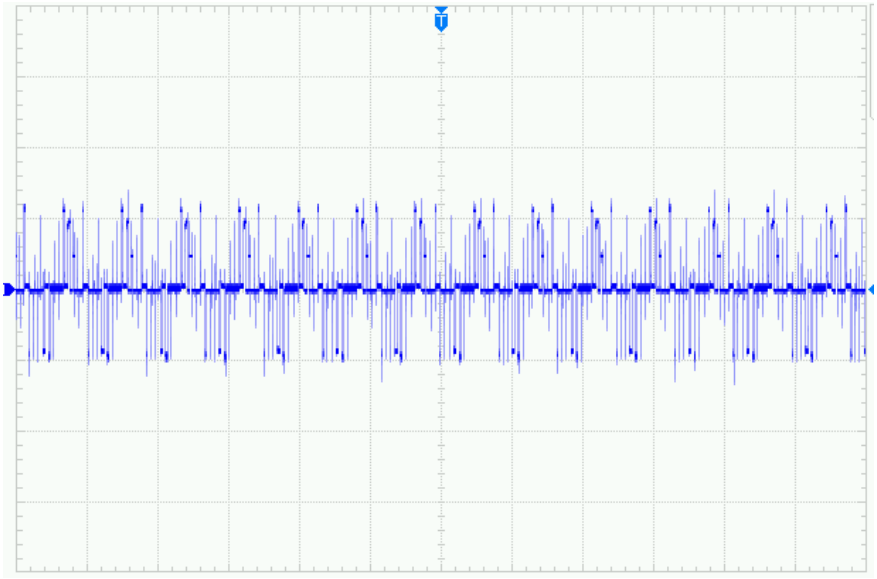


Figure 7.15: Output voltage m = 0.2

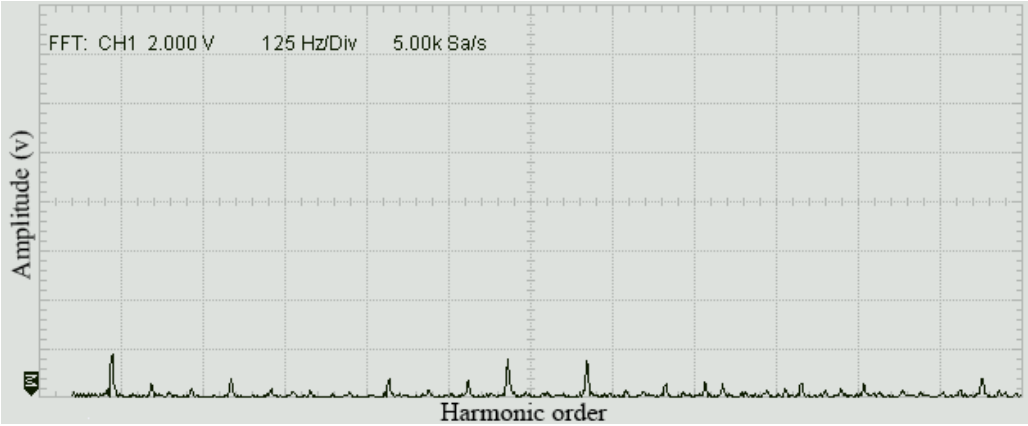


Figure 7.16: Harmonic spectrum when m = 0.2

7.6.2.3 Case 3: m = 0.3

For the case, m = 0.3, output voltage and voltage harmonics are shown in Figure 7.17 and Figure 7.18, respectively. In this case, the converter can generate three levels in the output voltage, the same as in the previous cases, and the pick-to-pick voltage is measured at 14 V. Also, the THD of this converter is calculated as 147.71%.

The harmonic spectrum shows that the 11th and 13th harmonics have significantly high value (71.47%) among other individual harmonics. In the experimental setup, some even harmonics are also observed.

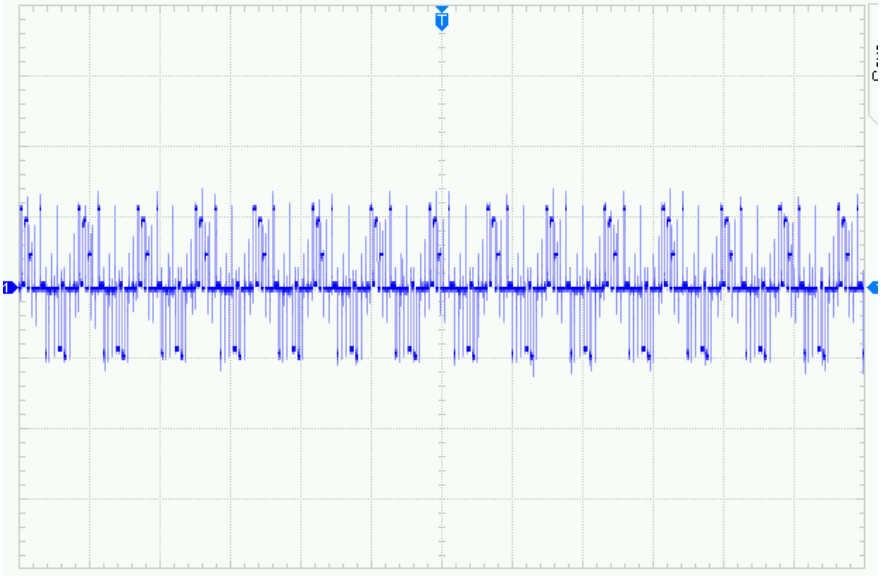


Figure 7.17: Output voltage m = 0.3

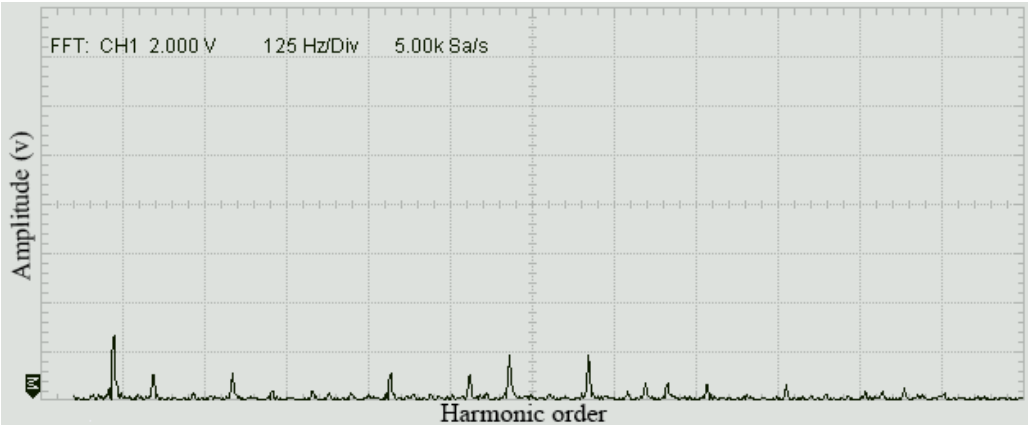


Figure 7.18: Harmonic spectrum when m = 0.3

7.6.2.4 Case 4: m = 0.4

For this case, m = 0.4, Figure 7.19 and Figure 7.20 show output voltage and voltage harmonics, respectively. Here, the converter can generate three levels in the output voltage. The peak-to-peak voltage is measured at 14 V. The THD of this converter output is calculated as 127.92%.

Like previous cases, here the harmonic spectrum shows that the 11th and 13th harmonics display a content of, 53.41% and 51.14%, respectively, of the fundamental component. It also contains some small levels of even harmonics.

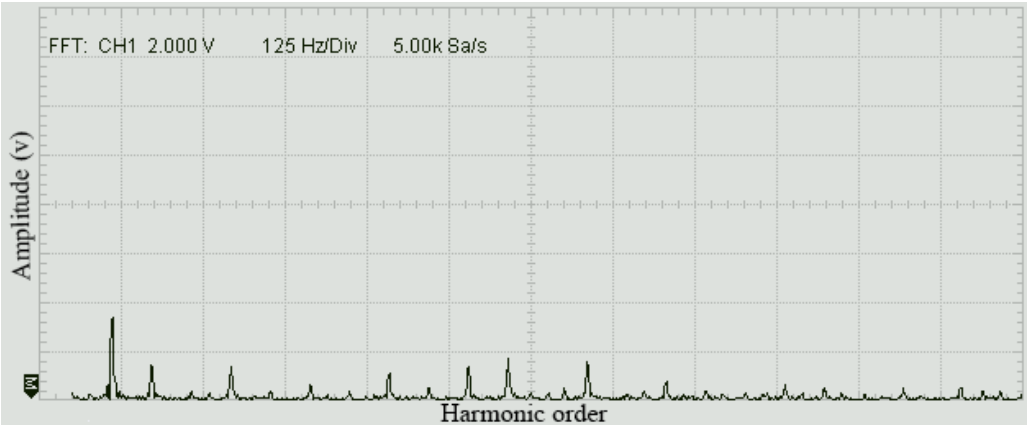


Figure 7.19: Output voltage m = 0.4

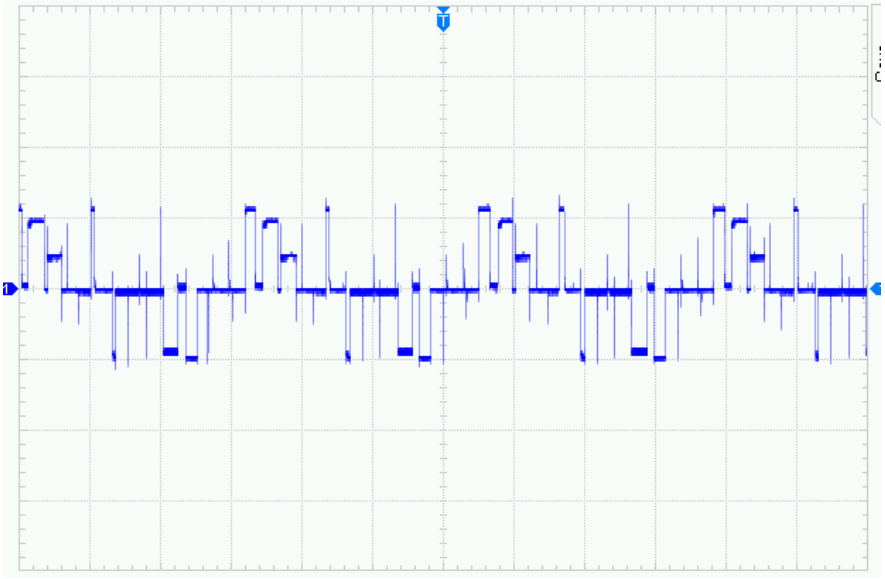


Figure 7.20: Harmonic spectrum when m = 0.4

7.6.2.5 Case 5: m = 0.5

For the case, m = 0.5, output voltage and voltage harmonics are shown in Figure 7.21 and Figure 7.22, respectively. In this case, the converter can generate five output voltage levels; the peak-to-peak voltage is measured at 22 V. The THD of this converter is calculated as 100.58%.

Harmonic spectra of this experimental setup show that the second harmonic has the highest content (44.64 % of the fundamental component) among all individual harmonics. Compared to previous cases, the 11th and 13th harmonics display lower content; however, it is still significantly high among other odd-numbered harmonics in this case (25.89%, and 20.54%, respectively, of the fundamental component). Other even-numbered harmonics were also observed to display a noticeable content of the fundamental component in the experimental setup.

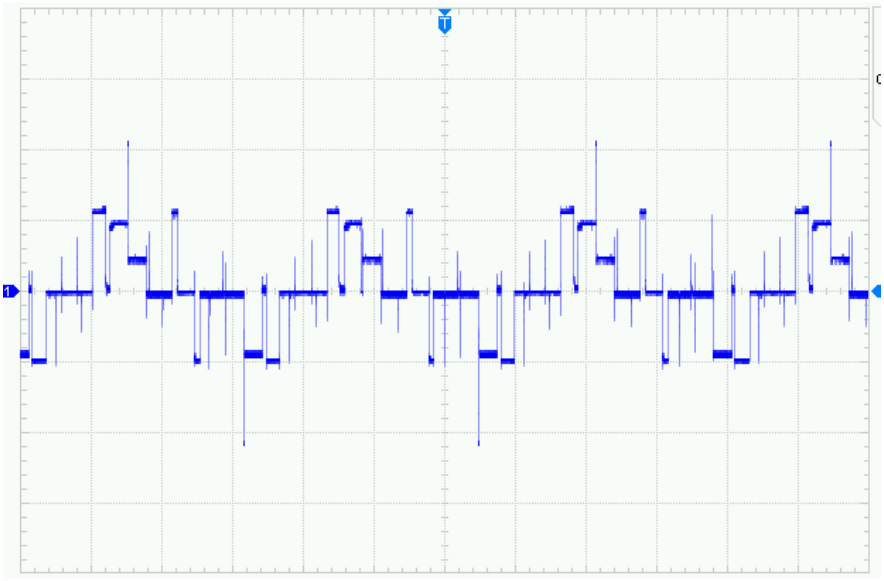


Figure 7.21: Output voltage m = 0.5

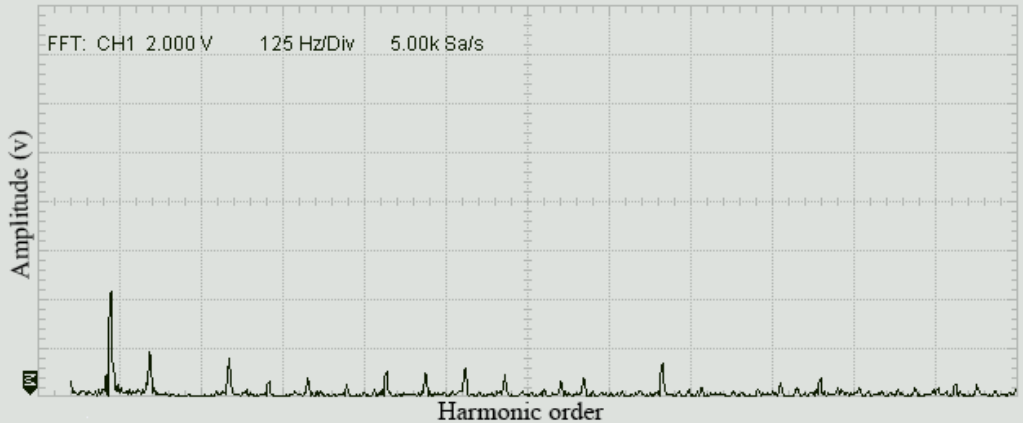


Figure 7.22: Harmonic spectrum when m = 0.5

7.6.2.6 Case 6: m = 0.6

For the case, m = 0.6, output voltage and voltage harmonics are shown in Figure 7.23 and Figure 7.24, respectively. In this case, the converter can generate five output voltage levels; the peak-to-peak voltage is measured at 22 V. Also, the THD of this converter is calculated as 84.21%.

Like case 5, harmonic spectra of this experimental setup show second harmonic has the highest content (38.81 % of the fundamental component) among all individual harmonics. Other even-numbered harmonics were also observed to display noticeable content level of the fundamental component in the experimental setup. The harmonic spectrum shows that among all odd-numbered harmonics, the 5th and 7th harmonics have the high value, 19.40%, and 20.29%, respectively, of the fundamental component.

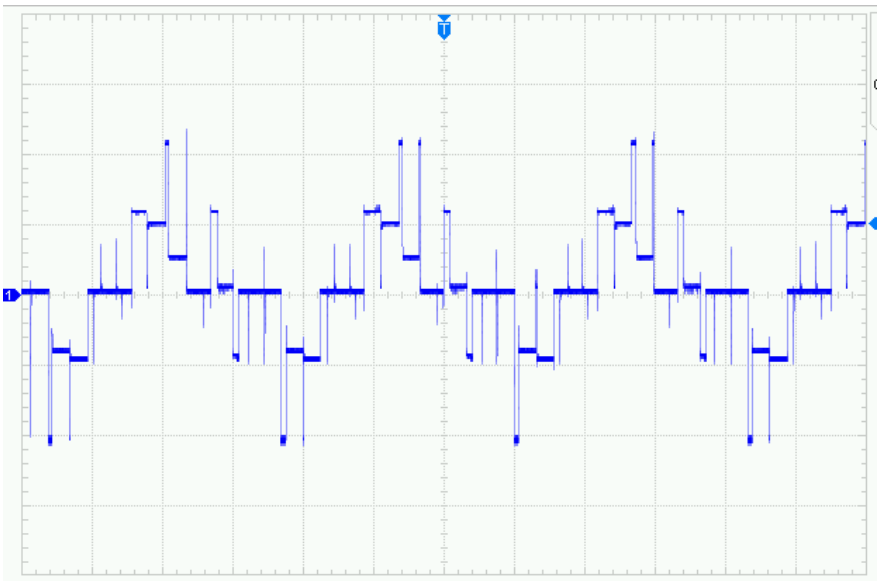


Figure 7.23: Output voltage m = 0.6

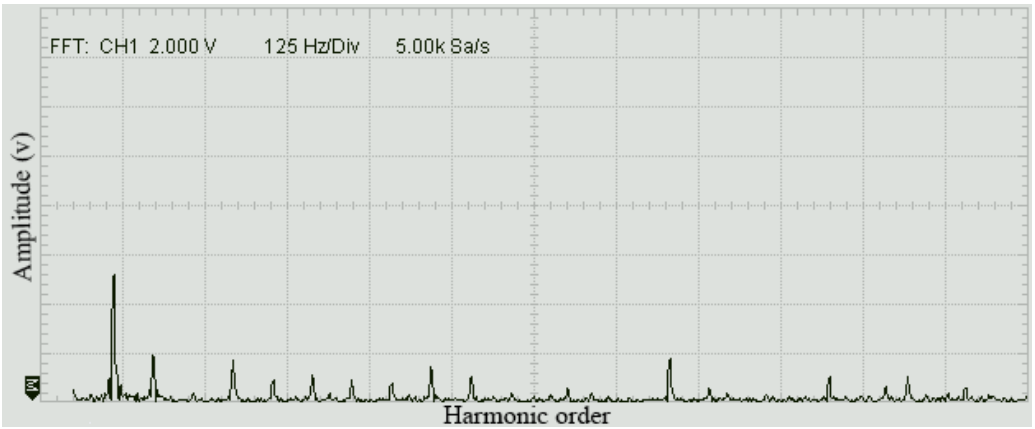


Figure 7.24: Harmonic spectrum when m = 0.6

7.6.2.7 Case 7: m = 0.7

For the case, m = 0.7, output voltage and voltage harmonics are shown in Figure 7.25 and Figure 7.26, respectively. In this case, the converter can generate five levels in the output voltage; therefore (and), the peak-to-peak voltage is measured at 22 V. Also, the THD of this converter is calculated as 72.57%.

Like cases 5 & 6, harmonic spectra of this experimental setup show that the second harmonic displays the highest content (28.13 % of the fundamental component) among all individual harmonics. Other even-numbered harmonics also have noticeable content of the fundamental component in the experimental setup. Compared to other cases, in this case, the harmonic spectrum shows that among odd-numbered harmonics, the 13th and 17th harmonics have a high value, 22.40%, and 19.79%, respectively, of the fundamental component.

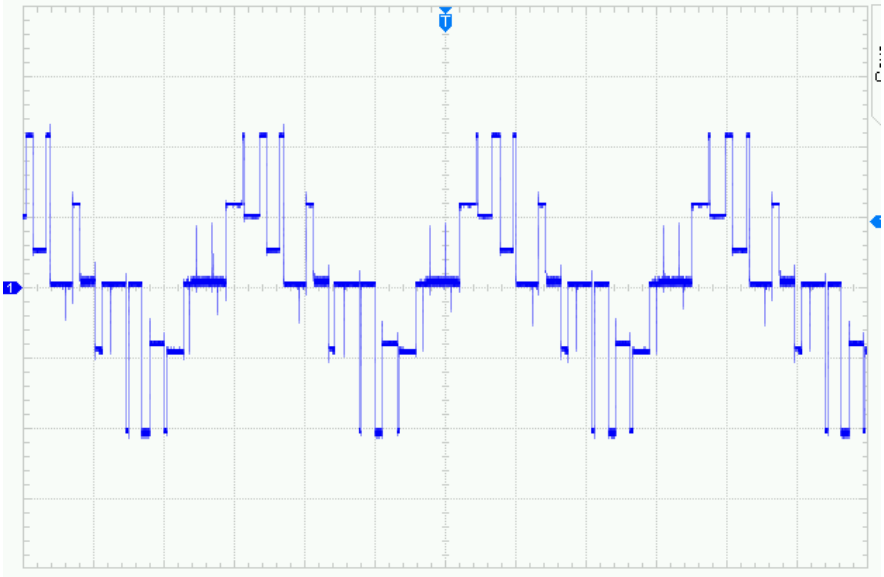


Figure 7.25: Output voltage m = 0.7

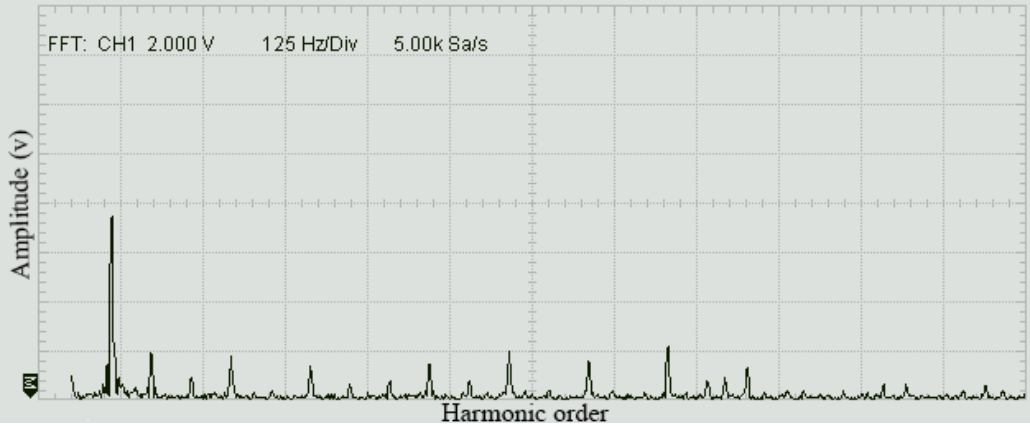


Figure 7.26: Harmonic spectrum when m = 0.7

7.6.2.8 Case 8: m = 0.8

For the case, m = 0.8, output voltage and Figure 7.27 and Figure 7.28, respectively. In this case, the converter can generate five levels in the output voltage, and the peak-to-peak voltage is measured at 24 V. Also, the THD of this converter is calculated as 70.40%.

The harmonic spectrum shows that the 11th and 13th harmonics have the highest value, 31.53% and 24.32%, respectively, of the fundamental component. In an experimental setup, some even harmonics are also observed.

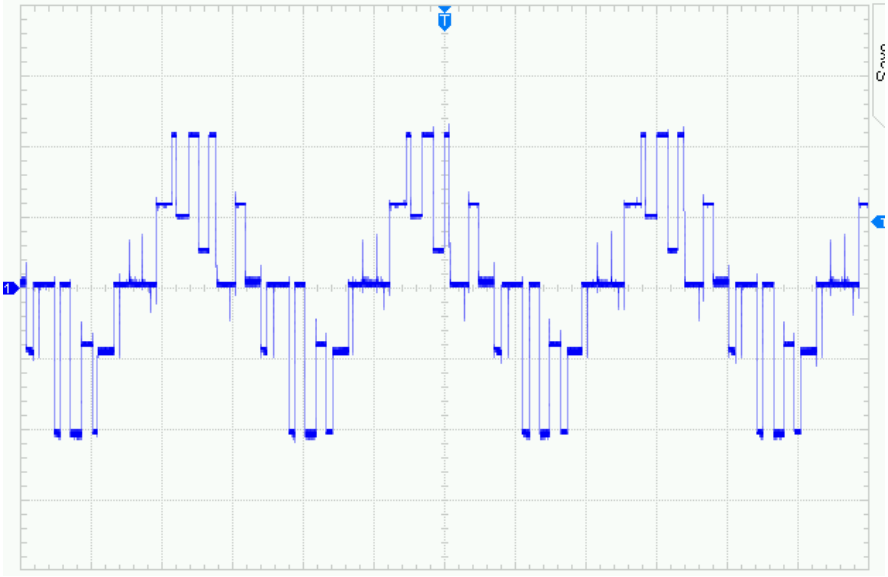


Figure 7.27: Output voltage m = 0.8

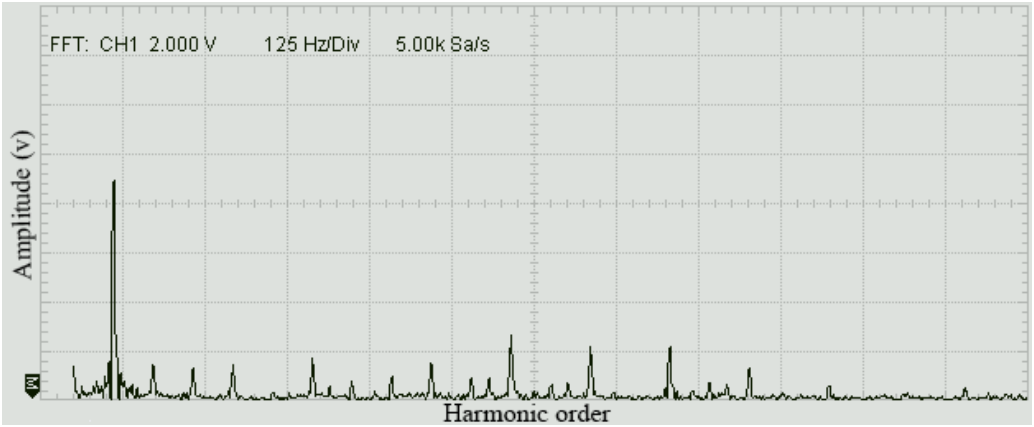


Figure 7.28: Harmonic spectrum when m = 0.8

7.6.2.9 Case 9: m = 0.9

For the case, m = 0.9, output voltage and voltage harmonics are shown in Figure 7.29 and Figure 7.30, respectively. In this case, the converter can generate five levels in the output voltage; therefore, the pick-to-pick voltage is measured at 24 V. Also, the THD of this converter is calculated as 63.21%.

The harmonic spectrum shows that the 11th and 13th harmonics have the highest value, 33.94%, and 22.64%, respectively, of the fundamental component. In an experimental setup, some even harmonics are also observed.

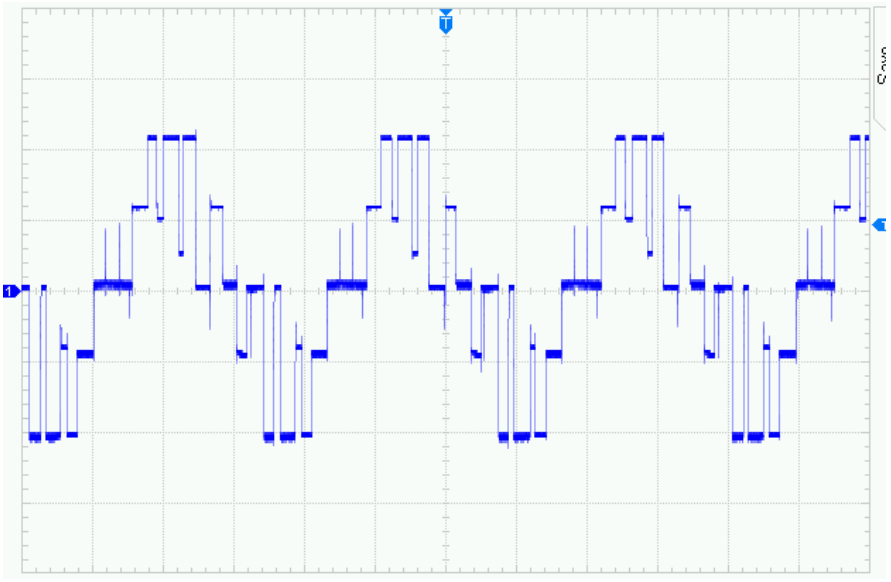


Figure 7.29: Output voltage m = 0.9

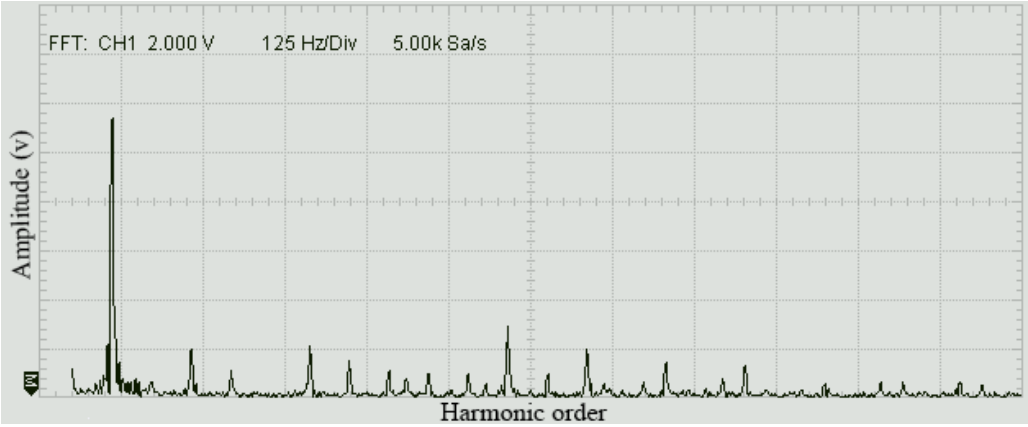


Figure 7.30: Harmonic spectrum when m = 0.9

7.6.2.10 Case 10: m = 1.0

For the case, m = 1.0, Figures 31 and 32 show output voltage and voltage harmonics, respectively. In this case, the converter generates five levels in the output voltage; therefore (and), the peak-to-peak voltage is measured at 24 V. The THD of this converter is calculated as 53.11%.

The harmonic spectrum shows that among all individual harmonics, the 11th and 13th harmonics display more content, 26.02% and 17.89% of the fundamental component. The experimental setup also shows the generation of some even harmonics.

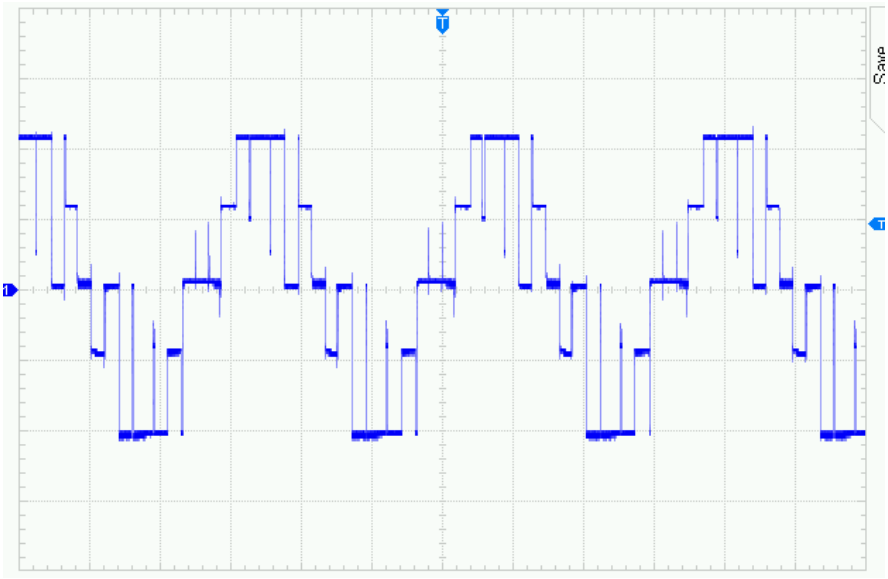


Figure 7.31: Output voltage m = 1.0

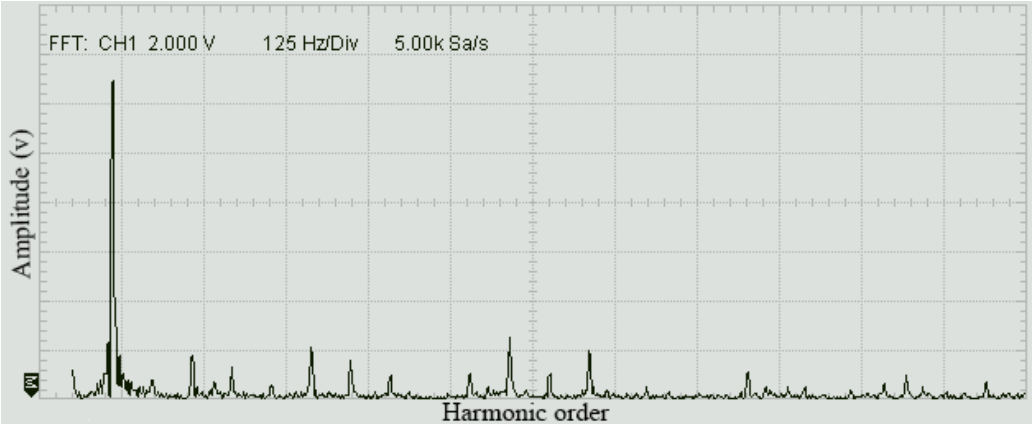


Figure 7.32: Harmonic spectrum when m = 1.0

7.6.3 Output voltage and harmonic spectrum of modified-WPWM technique

This section shows the experimental results achieved for the 5-level single phase CHB-MLI when controlled using modified-WPWM techniques. The same experimental setup is used to analyze the result of the proposed method. Like the previous section, the switching frequency of each switch of the converter is 180 Hz, and the fundamental frequency is 60 Hz. The voltage THD is calculated manually.

7.6.3.1 Case 1: j = 1

For the case, j= 1, output voltage and voltage harmonics are shown in Figure 7.33 and Figure 7.34, respectively. In this case, the converter can generate five complete levels in the output voltage; therefore, the pick-to-pick voltage is measured at 24 V. Also, the THD of this converter is calculated as 87.73%.

The harmonic spectrum shows that the 11th and 13th harmonics have the highest value, 70.33%, and 14.29%, respectively, of the fundamental component. In an experimental setup, there are only odd harmonics observed.

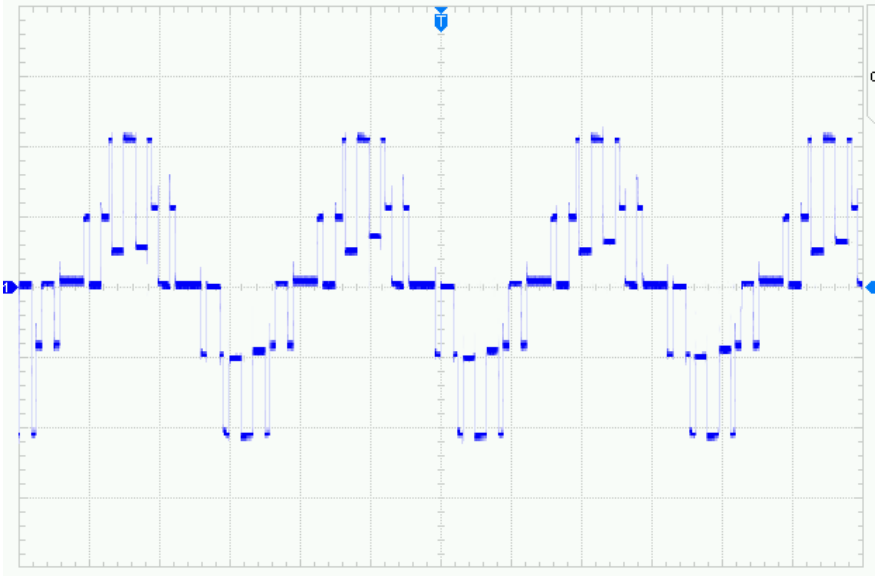


Figure 7.33: Output voltage when j=1

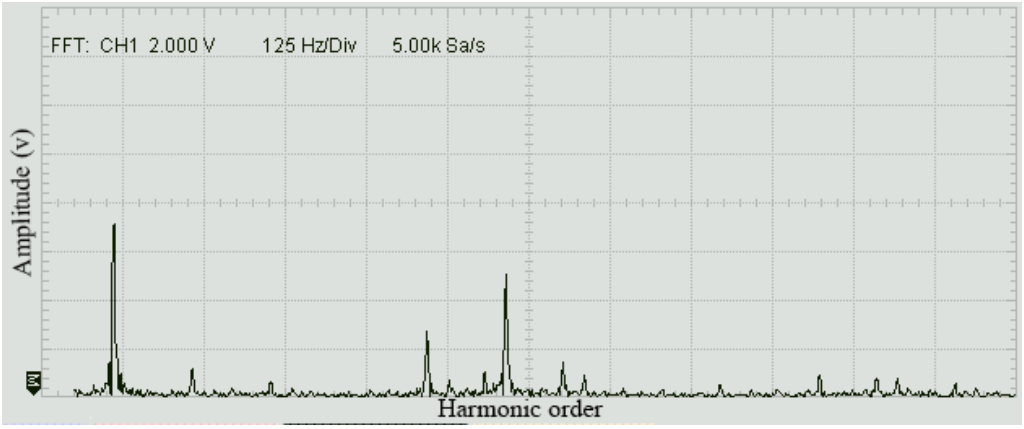


Figure 7.34: Harmonic spectrum when j = 1

7.6.3.2 Case 1: j = 2

For the case, j= 2, output voltage and voltage harmonics are shown in Figure 7.35 and Figure 7.36, respectively. In this case, the converter can generate five complete levels in the output voltage; therefore, the peak-to-peak voltage is measured at 24 V. Also, the THD of this converter is calculated as 77.03%.

The harmonic spectrum shows that the 11th and 13th harmonics have the highest value, 61.50% and 12.50%, respectively, of the fundamental component. In the experimental setup, there are only odd harmonics observed.

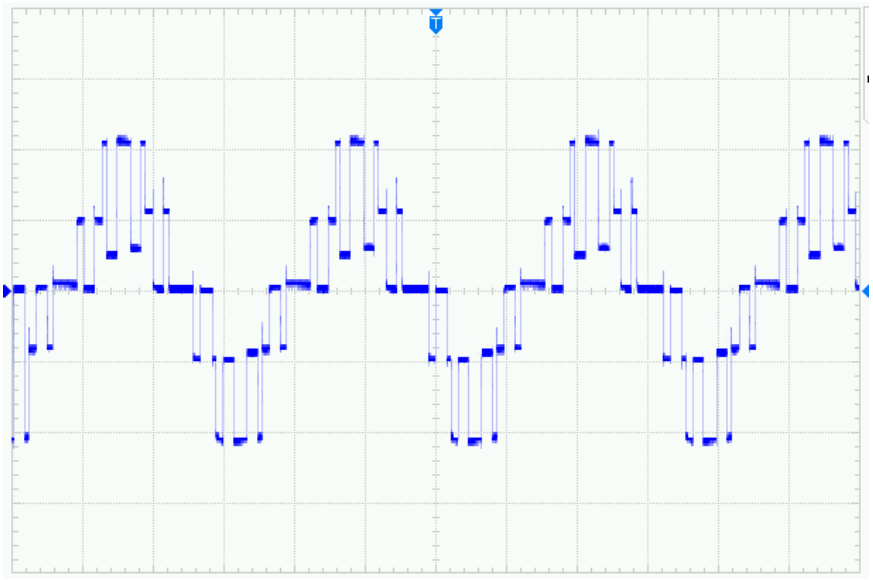


Figure 7.35: Output voltage when j=2

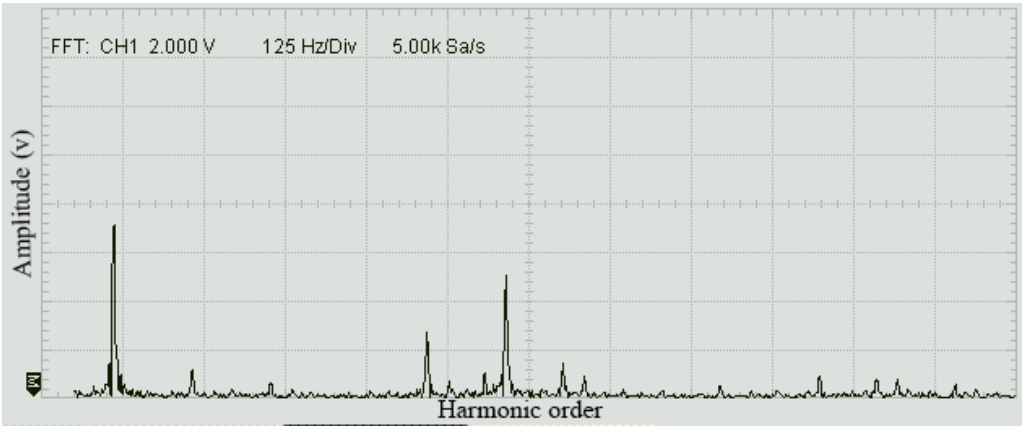


Figure 7.36: Harmonic spectrum when j = 2

7.6.3.3 Case 1: j = 3

For the case, j= 3, Figure 7.37 and Figure 7.38 show output voltage and voltage harmonics, respectively. Like previous cases, the converter generates five complete levels in the output voltage**,** and the peak-to-peak voltage is measured at 24 V. Also, the THD of this converter is calculated as 60.89%.

Here, the harmonic spectrum shows that, compared to all individual harmonics, the 11th and 19th harmonics consume more energy, 54.67% and 23.56% of the fundamental component. Also, in the experimental setup, only odd harmonics are observed**.**

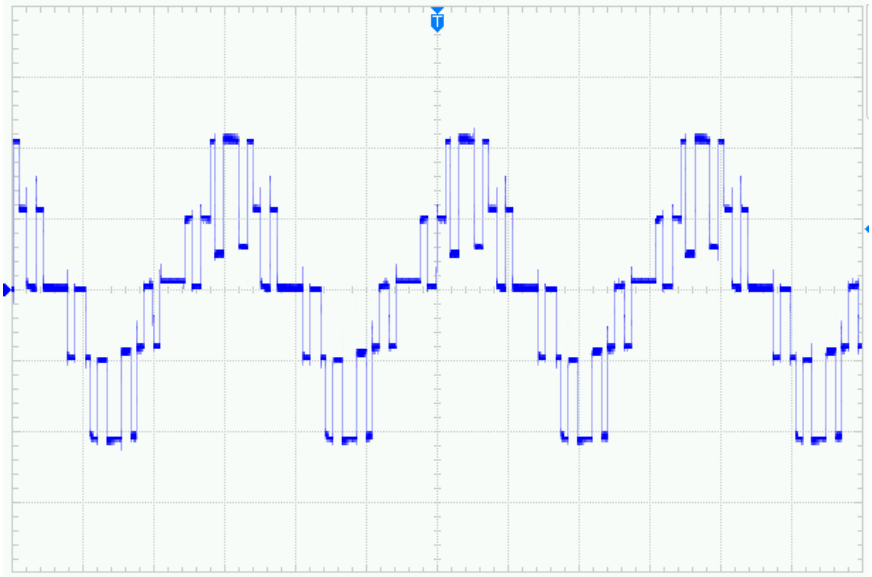


Figure 7.37: Output voltage when j=3

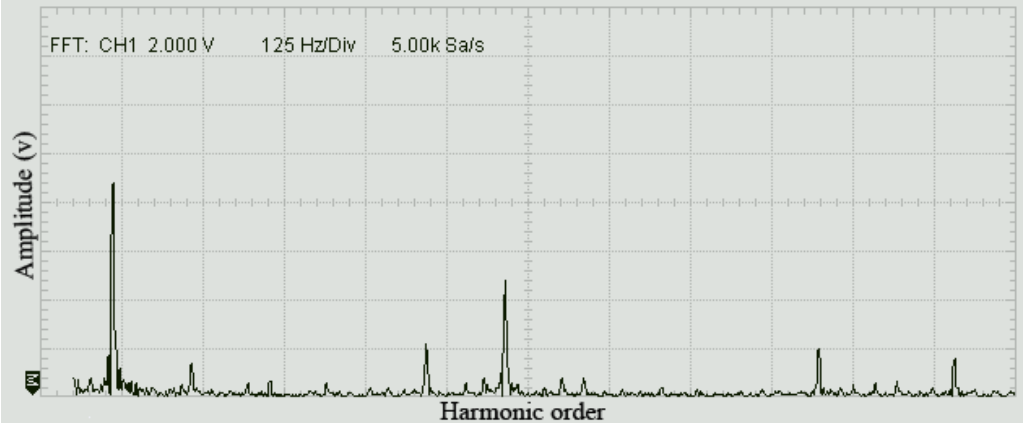


Figure 7.38: Harmonic spectrum when j = 3

7.6.3.4 Case 1: j = 4

For the case, j= 4, output voltage and voltage harmonics are shown in Figure 7.39 and Figure 7.40, respectively. In this case, the converter can generate five complete levels in the output voltage; therefore, the pick-to-pick voltage is measured at 24 V. Also, the THD of this converter is calculated as 60.89%.

Like case 3, the harmonic spectrum shows that among all harmonics, the 11th and 19th harmonics have a high value, 48.13%, and 24.48%, respectively, of the fundamental component. Also, the spectrum shows only odd harmonics.

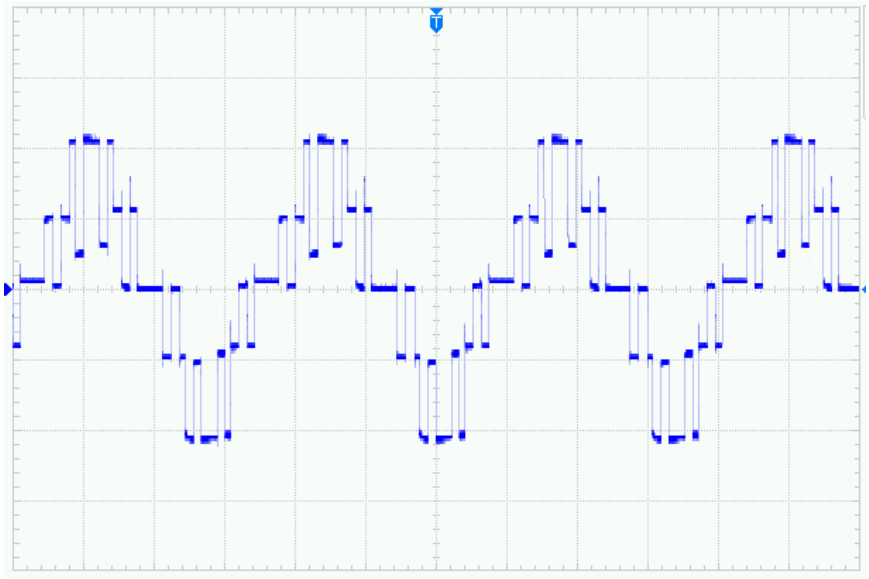


Figure 7.39: Output voltage when j=4

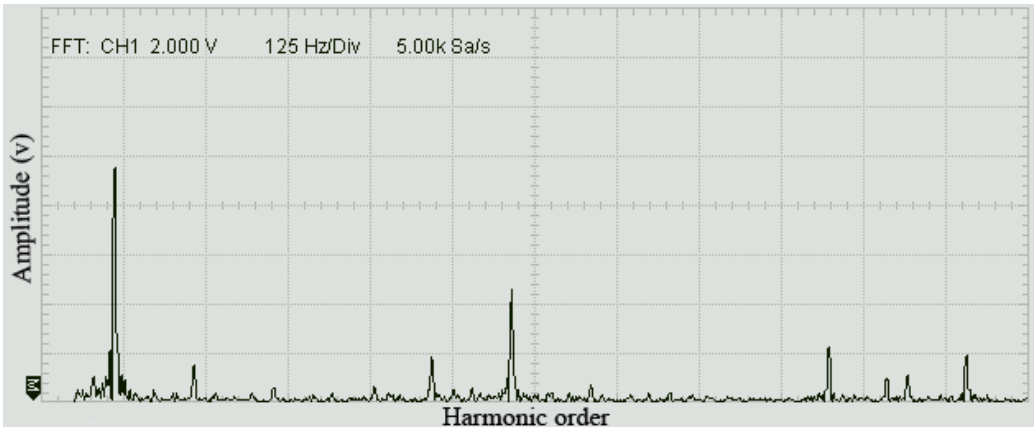


Figure 7.40: Harmonic spectrum when j = 4

7.6.3.5 Case 1: j = 5

For the case, j= 5, output voltage and voltage harmonics are shown in Figure 7.41 and Figure 7.42, respectively. In this case, the converter can generate five complete levels in the output voltage, and the peak-to-peak voltage is measured at 24 V. Also, the THD of this converter is calculated as 49.91%.

The harmonic spectrum shows that the 11th and 19th harmonics have the highest value, 37.08% and 23.60%, respectively, of the fundamental component. In the experimental setup, there are only odd harmonics observed.

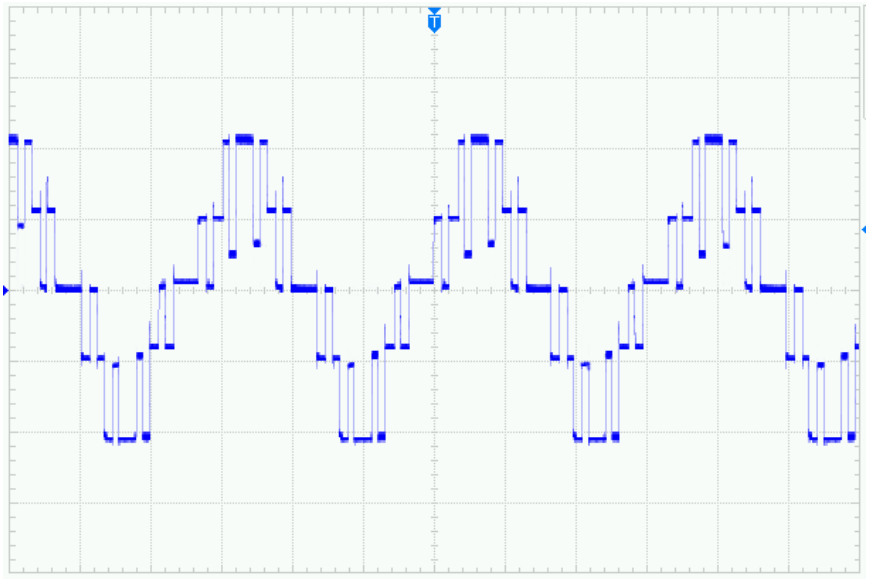


Figure 7.41: Output voltage when j=5

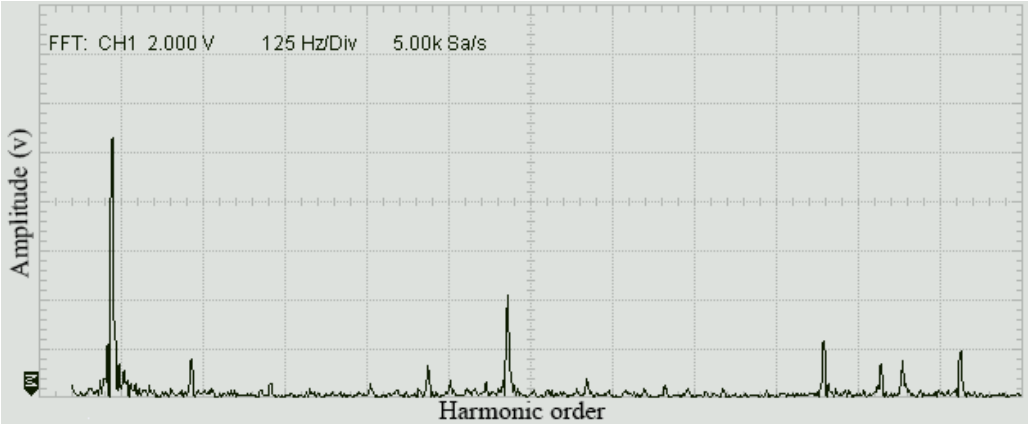


Figure 7.42: Harmonic spectrum when j = 5

7.6.3.6 Case 1: j = 6

For the case, j= 6, output voltage and voltage harmonics are shown in Figure 7.43 and Figure 7.44, respectively. In this case, the converter can generate five complete levels in the output voltage; therefore, the pick-to-pick voltage is measured at 24 V. Also, the THD of this converter is calculated as 42.87%.

The harmonic spectrum shows that the 11th and 19th harmonics have the highest value, 32.86% and 20.36%, respectively, of the fundamental component. In the experimental setup, there are only odd harmonics observed.

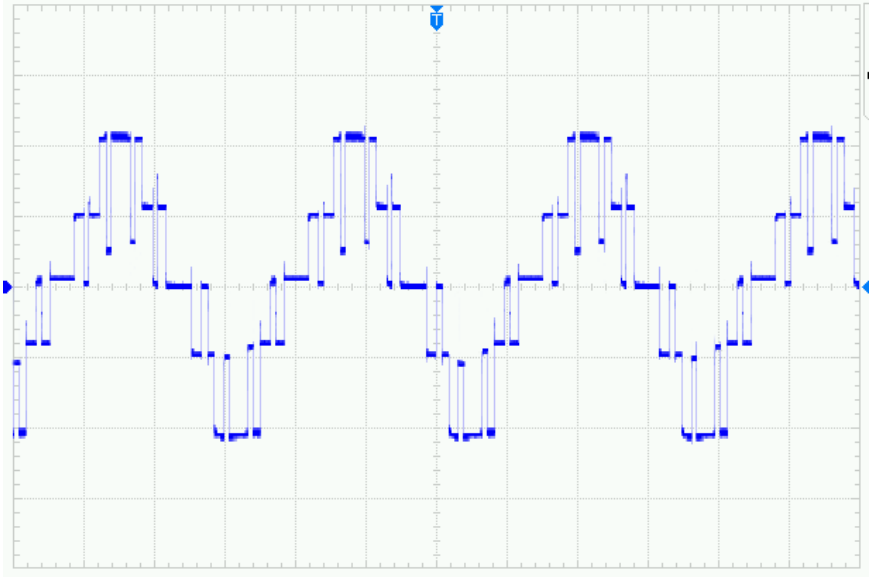


Figure 7.43: Output voltage when j=6

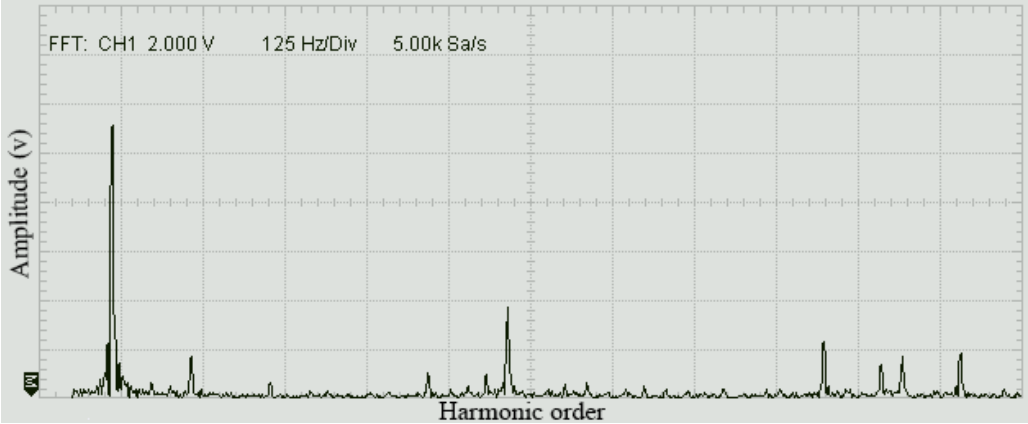


Figure 7.44: Harmonic spectrum when j = 6

7.6.3.7 Case 1: j = 7

For the case, j= 7, output voltage and voltage harmonics are shown in Figure 7.45 and Figure 7.46, respectively. In this case, the converter can generate five complete levels in the output voltage; therefore, the pick-to-pick voltage is measured at 24 V. Also, the THD of this converter is calculated as 37.02%.

Similar to previous cases, the harmonic spectrum shows that the 11th and 19th harmonics have the highest value compared to other individual harmonics, 27.42%, and 18.06%, respectively, of the fundamental component. Also, the experimental setup generated only odd-numbered harmonics.

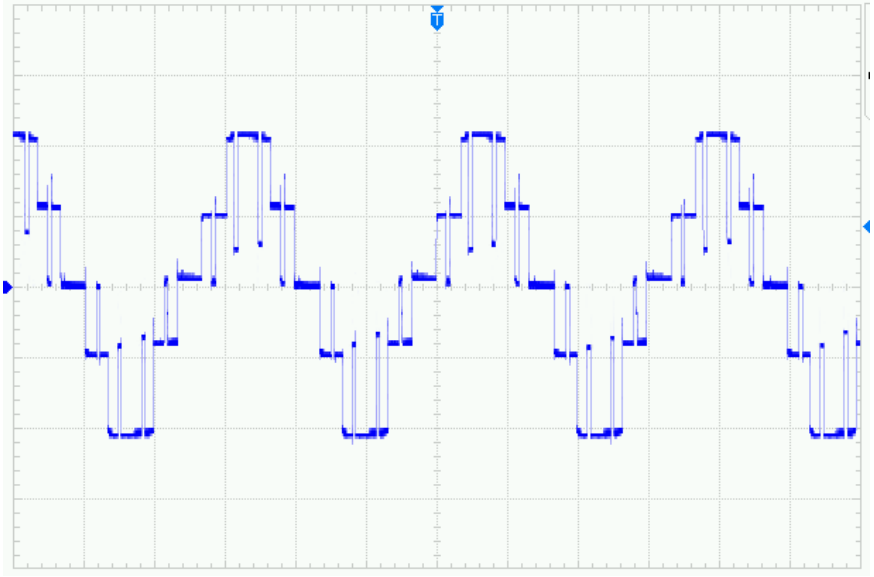


Figure 7.45: Output voltage when j=7

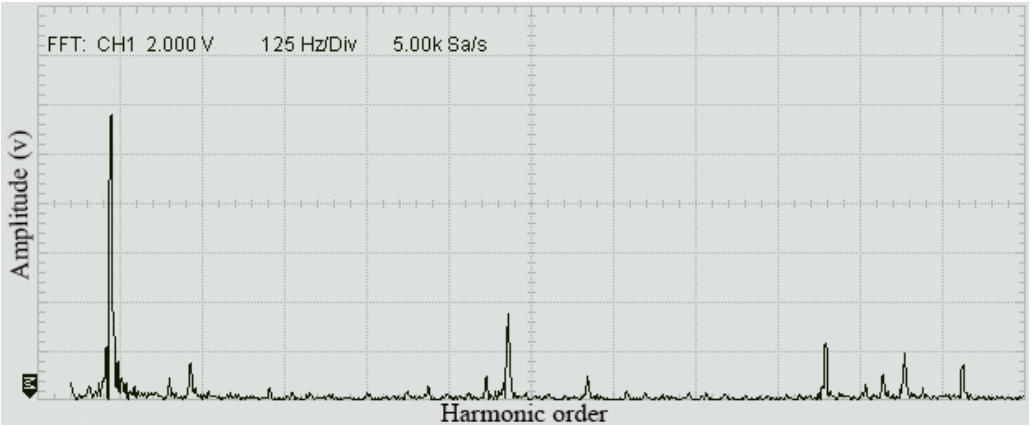


Figure 7.46: Harmonic spectrum when j = 7

7.6.3.8 Case 1: j = 8

For the case, j= 8, output voltage and voltage harmonics are shown in Figure 7.47 and Figure 7.48, respectively. Like previous cases, the converter generates five complete levels in the output voltage, and the peak-to-peak voltage is measured at 24 V. The THD of this converter is calculated as 33.31%.

The harmonic spectrum shows that the 11th and 19th harmonics have the highest value, 23.61%, and 17.38%, respectively, of the fundamental component. Also, the experimental setup generated only odd-numbered harmonics.

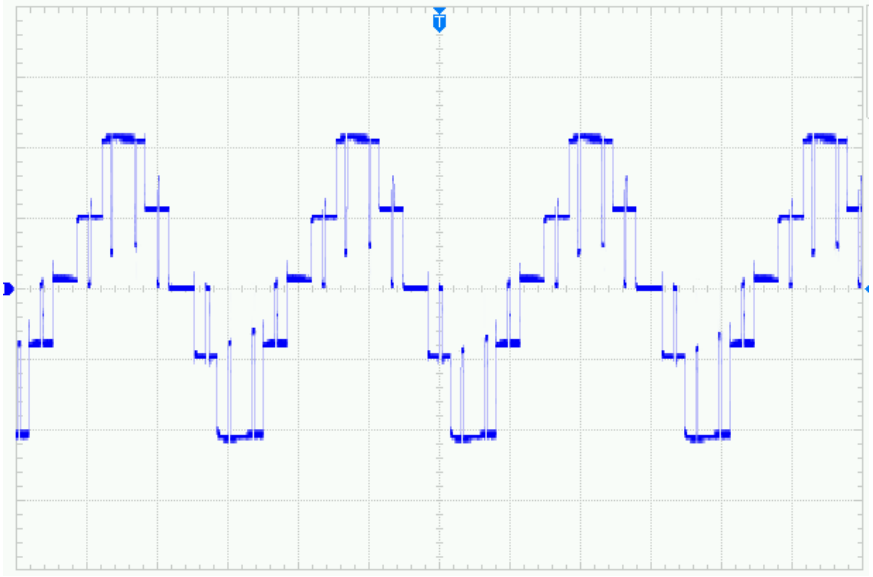


Figure 7.47: Output voltage when j=8

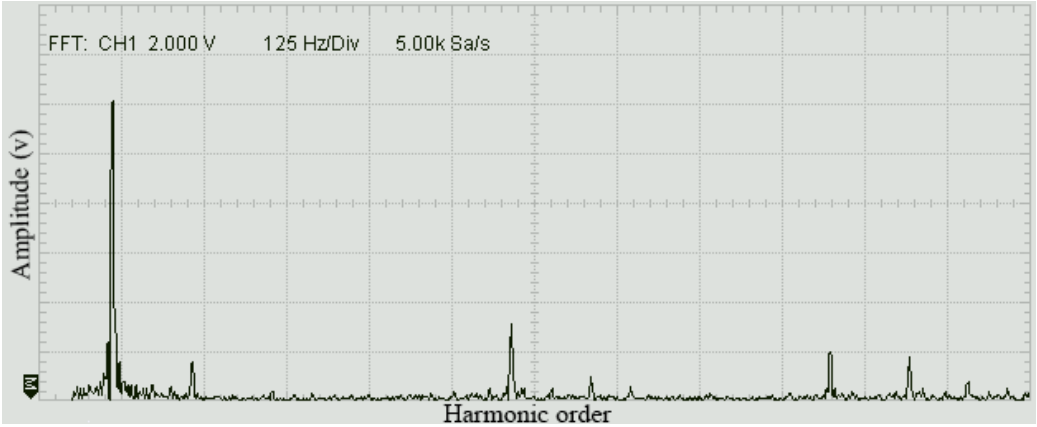


Figure 7.48: Harmonic spectrum when j = 8

7.6.3.9 Case 1: j = 9

For the case, j= 9, output voltage and voltage harmonics are shown in Figure 7.49 and Figure 7.50, respectively. In this case, the converter generates five complete levels in the output voltage; the peak-to-peak voltage is measured at 24 V. The THD of this converter is calculated as 31.16%.

The harmonic spectrum shows that among all individual harmonics, the 11th and 19th harmonics have significantly high values, 20.31% and 16.56%, respectively, of the fundamental component. The experimental setup generates only odd-numbered harmonics. No even-numbered harmonics were observed.

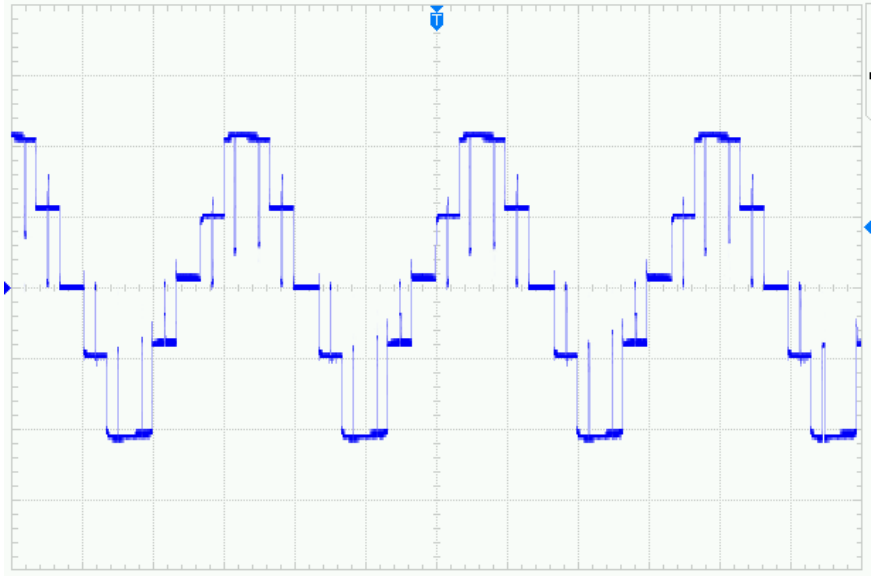


Figure 7.49: Output voltage when j=9

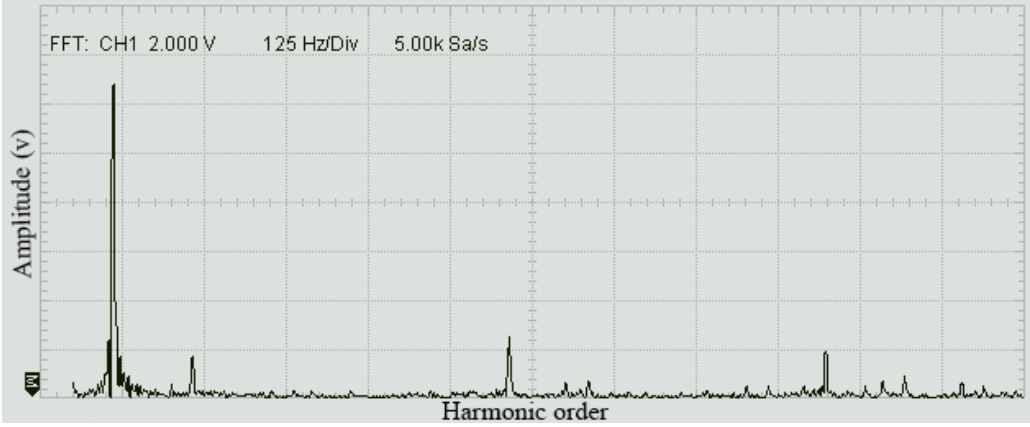


Figure 7.50: Harmonic spectrum when j = 9

7.6.3.10 Case 1: j = 10

For the case, j= 10, output voltage and voltage harmonics are shown in Figure 7.51 and Figure 7.52, respectively. Here, the converter generates five complete output voltage levels; the peak-to-peak voltage is measured at 24 V. The THD of this converter is calculated as 26.07%, which is the lowest of all previous cases.

Like previous cases, the harmonic spectrum shows that among all individual harmonics, the 11th and 19th harmonics consume significantly high energy, 14.33% and 13.43%, respectively, of the fundamental component. Also, the experimental setup generates only odd-numbered harmonics, and no even-numbered harmonics are observed.

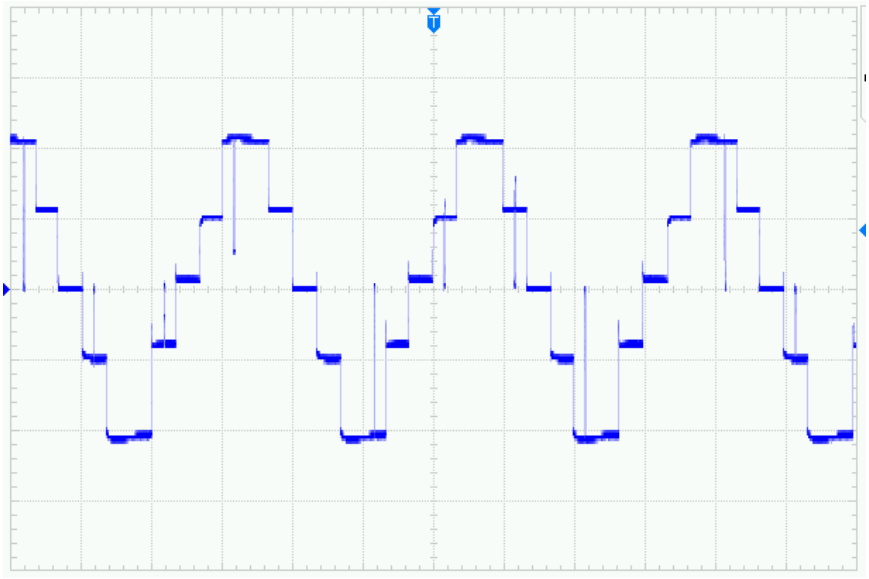


Figure 7.51: Output voltage when j = 10

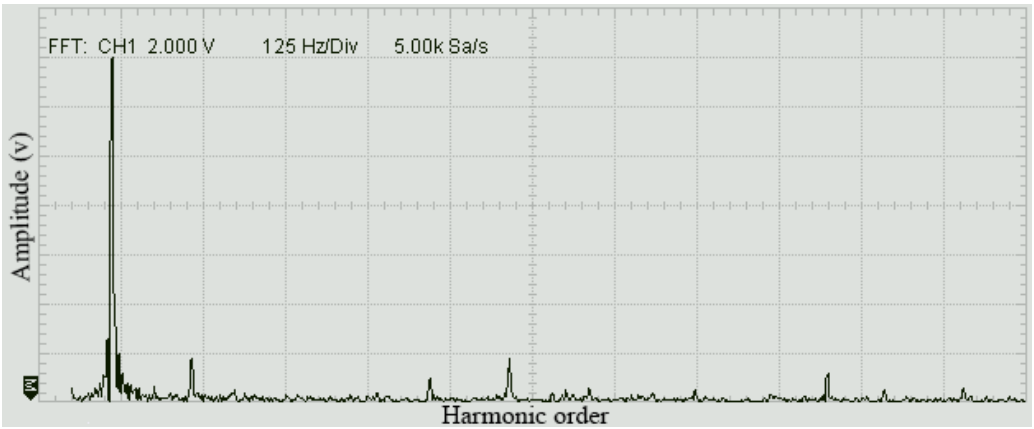


Figure 7.52: Harmonic spectrum when j = 10

7.7 Summary:

This chapter explained the PSPICE model of a 5-level CHB-MLI which is used to simulate the modified-WPWM technique. In this study charging and dis-charging of boot-strap capacitor has been analysed with the waveforms. Moreover, output waveform and lower order harmonics have been compared with the output of SPWM based CHB-MLI.

Furthermore, real hardware of a 5-level CHB-MLI has been explained and test results of output waveforms and harmonic sprectum have been presented in this chapter.

Chapter 8. Conclusion

8.1 Conclusion

This research aims to enhance the efficiency of PE converters with newly developed modified wavelet-based PWM technique. PE converters suffer from higher losses due to the presence of harmonics and switching actions that reduce the system's efficiency. Previous researchers have tried to improve the PE converter's efficiency by modifying its topology and redesigning the modulation (control) techniques. Changing the converter's topology may reduce a small number of harmonics, but increases the system's complexity, which is often not cost-effective. Some researchers have tried designing various modulation techniques that lower the losses in the PE converter. This thesis shows a new mathematical, wavelet-based modulation technique, called modified-WPWM, for the CHB-MLI converter that can be employed in medium/high voltage applications, operating at low frequency.

Mathematical equations of the proposed modified-WPWM technique have been derived. The solution of these equations gives the ON and OFF switching pulses of the PE switches. To evaluate the operation of this method, a 1-phase Simulink model has been made for the 5-, 7-, and 9-levels CHB-MLI operated at 180 Hz frequency. The proposed method widens the control pulses, allowing the PE switches to conduct longer and that enhances the fundamental component. The method has been validated by measuring the fundamental component and total harmonic distortion (THD) with the Simulink model.

This validation is extended with the PSPICE model of the CHB-MLI using LTSpice software which is more realistic and accurate model that includes the rise/fall times, switching delays, etc... of physical components.

Furthermore, a scaled-down physical model has also been implemented on the Texas Instruments F28069 microcontroller board for a 1-phase 5-level CHB-MLI converter. Test results for the fundamental component and THD have been measured. In all cases, the switching frequency is kept at 180 Hz which reduces the switching loss by 94.6% based on the calculation as compared to the previously implemented WPWM method. Similarly, other method also reduces the switching loss since the switching loss is a function of load current and the switching frequency. However, the result show that the novel proposed method reduces the harmonics efficiently at low switching frequency as compared to the traditional MC-PWM method.

8.2 Contribution

The analysis of the 1-phase model of the modified-WPWM technique has been presented. The benchmark in this dissertation is the most used carrier-based phase-shifted pulse-width modulation (PS-PWM). The performance comparison of the PS-PWM and proposed method has been carried out under the same switching stress.

Modified-WPWM technique shows an 8.94% increase in the fundamental component than the traditional PS-PWM strategy. This growth in the fundamental component represents a more efficient utilization of the DC source.

In the results, it is observed that the proposed method improves the THD performance by 50.9% of the system. Also, the amplitudes of the low-order harmonics 5th, 7th, 11th, 13th, and 17^{th} are reduced by 0%, 50.17%, 44.93%, 73.28% and 100% respectively. That means lower energy loss in the unwanted frequency signal and improved system efficiency. Moreover, the filter size can be reduced, lowering the overall system cost.

The proposed method produced switching pulses using mathematical equations. The pair of analysis and scaling functions are assigned to each H-bridge; hence the operator must only assign a new equation to the added H-bridge. It is not as complicated as the MC-PWM method in which carrier signals need to rearrange. Therefore, it is easily scalable to N number of levels. Also, the proposed method provides the closed form solution of the equations, meaning it does not require higher computational power and it can be implemented on inexpensive digital controller.

The previously applied WPWM method displaced switching pulses vertically, means they provide different conduction time for each H-bridge module. In contrast, the proposed modified-WPWM method displaced switching pulses horizontally to provide equal conduction time for all H-bridge modules. The equal conduction time distributed the load current equally in all sources to balance it without additional controller. In addition, conduction loss has been distributed equally among all switches. Therefore, equal rating switching is utilized in all H-bridge cells.

8.3 Limitations of the work conducted

This analysis of the modified-WPWM method neglected the impact of the filter circuit design. These filters are targeted to remove the harmonics from the output signal. Including the impact of the filter model with respect to its size and cost would be more practical to assess the full impact of the proposed approach.

In addition, the simplified model system used here helped to deliver precise, theoretical results and eliminate the impact of any external factors.

Also, the DC source applied in the analysis is derived using an AC-DC converter instead of an actual battery storage system.

8.4 Future research

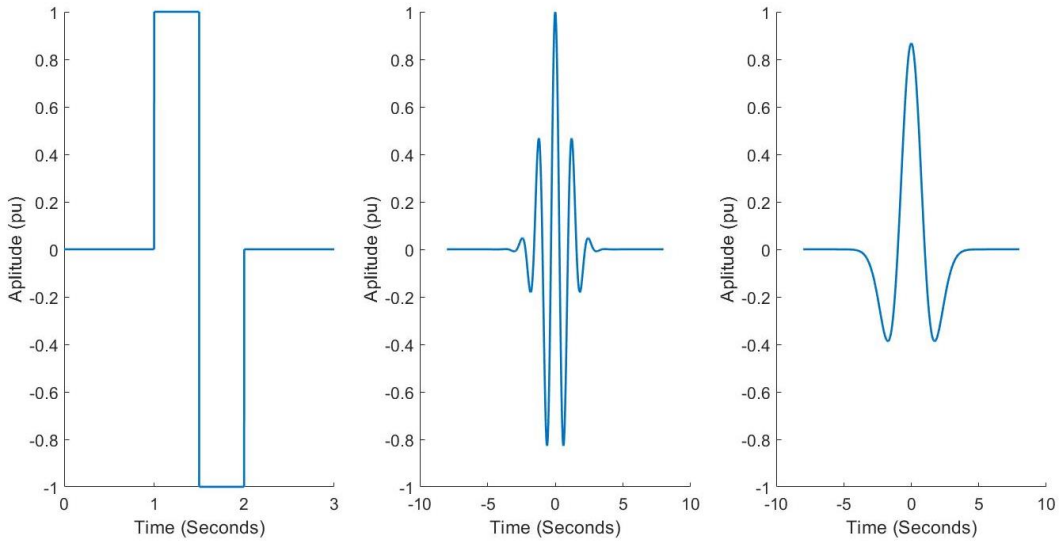
The modified WPWM can be evaluated for the higher-levels of multi-level converters, resulting in outputs with less harmonic content, which may not require the use of output filters.

Also, each switching frequency generates corresponding harmonic signals. Finding the modified-WPWM optimal switching frequency is another potential research area.

The comparison in this work is founded on principal measurements, like fundamental components and THD. It is advised to analyze the modified-WPWM designs employing other factors such as power, distortion, and lowest order harmonics etc...

Appendix A. Basic concept of a wavelet

Wavelet basis functions have been applied in numerous fields such as signal and image processing, sampling theory, turbulence, differential equations, statistics, quality control, computer graphics, economics and finance, medicine, neural networks, geophysics, astrophysics, quantum mechanics, neuroscience, and chemistry. In 1982, Jean Morlet, et al [142] first introduced the idea of wavelets as a family of functions that are constructed by using translation and dilation of a single function called the mother wavelet. Since then, Wavelet basis functions have been used for processing and representing non-periodic and non-stationary signals. There are distinct types of wavelets used for signal analysis such as Haar wavelet (Figure A 1 (a)), Morlet wavelet (Figure A.1 (b)) and Mexican hat wavelet (Figure A.1 (c)), etc. The choice of a wavelet function depends on the type of application.



(a) (b) (c)

Figure A.1: Types of Wavelet functions (a) Haar wavelet; (b) Morlet wavelet; (c) Mexican hat wavelet

Compared to wavelet and wavelet transformation, Fourier transform analysis does not contain the local information of the signal under study. Hence, it is not adequate for analyzing non-periodic signals in joint time and frequency domains [142], [143]. Wavelet functions, on the other hand, are a special kind of function that represent the oscillatory behavior of an arbitrary non-periodic and non-stationary signals signal (i.e., signals that last for a brief period and then fade out). Such a feature is based on their ability to parameterize signals using sets of basic functions that are localized in time and frequency. Each type of wavelet functions uses a single function in conjunction with its dilations and translations, to generate a set of orthonormal basis functions to represent the signal under study.

As mentioned before, wavelet basis functions (and their related transforms) have been used as effective and efficient tools for representing and processing signals with non-periodic and non-stationary natures. Such signals are common under large signal disturbances in power systems, machines drive, and power electronic converters. The notion of applying a wavelet function on a signal involves decomposing the signal using sets of analysis basis functions and reconstructing signals using sets of synthesis basis functions. Thus, the signal can be represented as an N-dimensional approximation case. This kind of representation is used to interpret the sampling theorem in the framework of the wavelet-based multiresolution analysis (MRA).

Mathematically, the aim of constructing MRA is to represent a function (f) as a limit of successive approximations, each of which is a finer version of the function (f). These successive approximations correspond to different levels of resolutions. Thus, MRA is a formulation approach to constructing orthogonal wavelet bases using a definite set of rules and procedures. The basic principle of the MRA deals with the decomposition of the whole function space into individual subspaces $\mathrm{V_n} \subset \mathrm{V_{n+1}}$ so that space $\mathrm{V_{n+1}}$ consists of all rescaled functions in V_n. This means decomposition of each function into components of different scales so that an individual component of the original function (f) occurs in each subspace.

An MRA of $\mathrm{L}^2(\mathbb{R})$ is a sequence $\{\mathrm{V_n}: \mathrm{n} \in \mathbb{Z}\}$ of closed subspace $\mathrm{L}^2(\mathbb{R})$ satisfying the following properties:

$\mathrm{V_n} \subset \mathrm{V_{n+1}}$ for all $\mathrm{n} \in \mathbb{Z}$ (A-1)

$\mathrm{U_{n\in\mathbb{Z}}V_n}$ is dense in $\mathrm{L}^2(\mathbb{R})$ (A-2)

$\mathrm{U_{n\in\mathbb{Z}}^{n\in\mathbb{Z}}V_n} = \{0\}$ (A-3)

$\mathrm{f(t)} \in \mathrm{V_n}$ if and only if $\mathrm{f(2t)} \in \mathrm{V_{n+1}}$ for all $\mathrm{n} \in \mathbb{Z}$

There is a function ϕ in $\mathrm{V_0}$ such that the system $\{\phi(\mathrm{t-n}): \mathrm{n} \in \mathbb{Z}\}$ forms an orthogonal basis for $\mathrm{V_0}$.

The function ϕ whose existence is declared in (v) is called the father wavelet or scaling function $\phi(\mathrm{t})$ of the given MRA. This scaling function $\phi(\mathrm{t})$ when dilated to scale j as $\phi_{\mathrm{j}}(\mathrm{t})$ is orthogonal to its translations at that scale j. The

generated basis functions at scale j spans a space V_j that provides an approximation to the signal in that space, which can be defined as:

$$V_j(\varphi) = clos_{L^2} < \{\phi_{j,k}(t)\} > ; \quad \text{(A-4)}$$

Where,

$$\phi_{j,k}(t) = \phi_1(2^j t - k) ; \quad \text{(A-5)}$$

j = 0, 1, 2 3, …, $k \in \mathbb{Z}$

The collection of the spanned spaces $\{V_j\}$ allows the construction of a dyadic type MRA. Since scaling basis functions $\{\phi_{j,k}\}$ are generated through shifting and dilating the scaling function φ(t), the spanned scaling spaces are nested such that:

$$\ldots V_{j-1} \subset V_j \subset V_{j+1} \subset V_{n+2} \quad \text{(A-6)}$$

Although the generated basis functions $\{\phi_{j,k}\}$ at a certain scale j are orthogonal, they are not complete with respect to $L^2(\mathbb{R})$. A more complete set $\{\phi_{j-1,k}\}$ is also orthogonal but it is twice as dense. The difference between the successive spaces V_j and V_{j-1} yields a difference space spanned by another set of basis functions that are known as the wavelet basis functions. That is, for each space V_j, there exists an orthogonal complement space W_j, which is spanned by the set $\{\Psi_{j,k}\}$ and can be defined as:

$$W_j(\varphi) = clos_{L^2} < \{\Psi_{j,k}(t)\} > ; \quad \text{(A-7)}$$

Where, j = 1, 1, 2 3, …, $k \in \mathbb{Z}$

And

$$\Psi_{j,k}(t) = \Psi_1\left(2^j t - k\right); \quad \text{(A-8)}$$

Where, j = 0, 1, 2 3, …, $k \in \mathbb{Z}$

In general, a spanned space V_j in an MRA can be constructed using both spaces V_{j+1} and W_{j+1} as:

$$V_j = V_{j+1} \oplus W_{j+1} \quad \text{(A-9)}$$

There are four major types of wavelet basis functions used in different signal and image processing applications:

1. Orthogonal wavelet basis functions
2. Semi-orthogonal wavelet basis functions
3. Bi-orthogonal wavelet basis functions
4. Shifted-orthogonal wavelet basis function.

These types of wavelet basis functions are capable of spanning spaces, such as, V_j and W_j. A collection of these spaces allows the construction of MRAs. However, these constructed MRAs are the dyadic type that can support uniform ideal sampling processes.

Appendix B. Numerical value of measured individual harmonics

Table 10.1: Amplitude of the harmonics and fundamental components for the modified-WPWM 5-level CHB-MLC

J	60 Hz	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th	18th	19th	20th
1	7.28	0.00	1.32	0.00	0.92	0.00	0.00	0.00	2.84	0.00	5.12	0.00	1.04	0.00	0.00	0.00	0.00	0.00	1.00	0.00
		0.00	18.13	0.00	12.64	0.00	0.00	0.00	39.01	0.00	70.33	0.00	14.29	0.00	0.00	0.00	0.00	0.00	13.74	0.00
2	8.00	0.00	1.40	0.00	0.80	0.00	0.00	0.00	2.76	0.00	4.92	0.00	1.00	0.00	0.00	0.00	0.00	0.00	1.60	0.00
		0.00	17.50	0.00	10.00	0.00	0.00	0.00	34.50	0.00	61.50	0.00	12.50	0.00	0.00	0.00	0.00	0.00	20.00	0.00
3	9.00	0.00	1.56	0.00	0.80	0.00	0.00	0.00	2.32	0.00	4.92	0.00	0.92	0.00	0.00	0.00	0.00	0.00	2.12	0.00
		0.00	17.33	0.00	8.89	0.00	0.00	0.00	25.78	0.00	54.67	0.00	10.22	0.00	0.00	0.00	0.00	0.00	23.56	0.00
4	9.64	0.00	1.64	0.00	0.72	0.00	0.00	0.00	1.92	0.00	4.64	0.00	0.68	0.00	0.00	0.00	0.00	0.00	2.36	0.00
		0.00	17.01	0.00	7.47	0.00	0.00	0.00	19.92	0.00	48.13	0.00	7.05	0.00	0.00	0.00	0.00	0.00	24.48	0.00
5	10.68	0.00	1.68	0.00	0.68	0.00	0.00	0.00	1.40	0.00	3.96	0.00	0.88	0.00	0.60	0.00	0.00	0.00	2.52	0.00
		0.00	15.73	0.00	6.37	0.00	0.00	0.00	13.11	0.00	37.08	0.00	8.24	0.00	5.62	0.00	0.00	0.00	23.60	0.00
6	11.20	0.00	1.72	0.00	0.72	0.00	0.00	0.00	0.88	0.00	3.68	0.00	0.24	0.00	0.00	0.00	0.00	0.00	2.28	0.00
		0.00	15.36	0.00	6.43	0.00	0.00	0.00	7.86	0.00	32.86	0.00	2.14	0.00	0.00	0.00	0.00	0.00	20.36	0.00
7	11.96	0.00	1.52	0.00	0.80	0.00	0.00	0.00	0.68	0.00	3.28	0.00	0.24	0.00	0.00	0.00	0.84	0.00	2.16	0.00
		0.00	12.71	0.00	6.69	0.00	0.00	0.00	5.69	0.00	27.42	0.00	2.01	0.00	0.00	0.00	7.02	0.00	18.06	0.00
8	12.20	0.00	1.60	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.88	0.00	1.08	0.00	0.00	0.00	0.00	0.00	2.12	0.00
		0.00	13.11	0.00	0.00	0.00	0.00	0.00	0.00	0.00	23.61	0.00	8.85	0.00	0.00	0.00	0.00	0.00	17.38	0.00
9	12.80	0.00	1.88	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.60	0.00	0.84	0.00	0.00	0.00	0.64	0.00	2.12	0.00
		0.00	14.69	0.00	0.00	0.00	0.00	0.00	0.00	0.00	20.31	0.00	6.56	0.00	0.00	0.00	5.00	0.00	16.56	0.00
10.0	13.40	0.00	1.76	0.00	0.00	0.00	0.76	0.54	0.84	0.00	1.92	0.00	0.64	0.00	0.00	0.44	0.00	0.00	1.80	0.00
		0.00	13.13	0.00	0.00	0.00	5.67	4.03	6.27	0.00	14.33	0.00	4.78	0.00	0.00	3.28	0.00	0.00	13.43	0.00

Table 10.2: Amplitude of the harmonics and fundamental components for a PS-PWM

m	60 Hz	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th	18th	19th	20th
0.1	1.32	0.64	0.52	0.64	0.32	0.00	0.28	0.60	0.22	0.00	1.40	0.00	1.40	0.64	0.32	0.64	0.20	0.20	0.00	0.00
		48.48	39.39	48.48	24.24	0.00	21.21	45.45	16.67	0.00	106.06	0.00	106.06	48.48	24.24	48.48	15.15	15.15	0.00	0.00
0.2	1.80	0.68	0.52	0.96	0.44	0.00	0.32	0.84	0.60	1.00	1.72	0.00	1.72	0.40	0.72	0.80	0.20	0.20	0.00	0.00
		37.78	28.89	53.33	24.44	0.00	17.78	46.67	33.33	55.56	95.56	0.00	95.56	22.22	40.00	44.44	11.11	11.11	0.00	0.00
0.3	2.80	1.24	0.44	1.32	0.60	0.48	0.00	1.36	0.00	1.16	2.00	0.00	2.00	0.56	0.84	0.50	0.00	0.76	0.00	0.00
		44.29	15.71	47.14	21.43	17.14	0.00	48.57	0.00	41.43	71.43	0.00	71.43	20.00	30.00	17.86	0.00	27.14	0.00	0.00
0.4	3.52	1.60	0.60	1.56	0.52	0.84	0.56	1.32	0.72	1.60	1.88	0.40	1.80	0.00	0.96	0.00	0.00	0.80	0.56	0.00
		45.45	17.05	44.32	14.77	23.86	15.91	37.50	20.45	45.45	53.41	11.36	51.14	0.00	27.27	0.00	0.00	22.73	15.91	0.00
0.5	4.48	2.00	0.00	1.80	0.84	0.96	0.80	1.24	1.16	1.36	1.16	0.00	0.92	0.00	1.56	0.00	0.00	0.72	0.96	0.00
		44.64	0.00	40.18	18.75	21.43	17.86	27.68	25.89	30.36	25.89	0.00	20.54	0.00	34.82	0.00	0.00	16.07	21.43	0.00
0.6	5.36	2.08	0.56	1.96	1.04	1.24	1.12	0.88	1.60	1.20	0.64	0.00	0.20	0.00	0.90	0.00	0.00	0.00	1.16	0.80
		38.81	10.45	36.57	19.40	23.13	20.90	16.42	29.85	22.39	11.94	0.00	3.73	0.00	16.79	0.00	0.00	0.00	21.64	14.93
0.7	7.68	2.16	1.08	2.08	0.00	1.52	0.84	0.92	1.68	0.92	1.16	0.00	1.72	0.00	2.40	1.00	1.52	0.00	0.00	0.00
		28.13	14.06	27.08	0.00	19.79	10.94	11.98	21.88	11.98	15.10	0.00	22.40	0.00	31.25	13.02	19.79	0.00	0.00	0.00
0.8	8.88	1.92	1.32	1.88	0.00	1.84	0.00	1.00	1.72	0.00	2.80	0.80	2.16	0.00	2.28	0.84	1.52	0.84	0.84	0.00
		21.62	14.86	21.17	0.00	20.72	0.00	11.26	19.37	0.00	31.53	9.01	24.32	0.00	25.68	9.46	17.12	9.46	9.46	0.00
0.9	10.60	1.32	1.72	1.64	0.00	1.96	1.24	1.28	1.68	1.32	3.28	1.20	2.40	0.00	2.12	0.00	1.68	0.00	0.80	0.00
		12.45	16.23	15.47	0.00	18.49	11.70	12.08	15.85	12.45	30.94	11.32	22.64	0.00	20.00	0.00	15.85	0.00	7.55	0.00
1.0	12.30	1.32	2.20	1.40	0.00	2.40	1.40	1.12	1.20	0.80	3.20	1.32	2.20	0.00	1.60	0.00	1.64	0.00	1.00	0.00
		10.73	17.89	11.38	0.00	19.51	11.38	9.11	9.76	6.50	26.02	10.73	17.89	0.00	13.01	0.00	13.33	0.00	8.13	0.00

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