THE UNIVERSITY OF ONTARIO INSTITUTE OF TECHNOLOGY
FACULTY OF ENGINEERING AND APPLIED SCIENCE

RELIABILITY EVALUATION OF THE TWO BUS INTERFACE CONTROLLERS IN THE DARLINGTON SIMULATOR

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ABSTRACT

The Darlington simulator is now two decades old and, in common with any nuclear simulator of a similar age, suffers the problem of parts aging and obsolescence. In the past, replacement parts were available from the original vendor, Canadian Aviation Electronics. This is no longer an option, as the vendor has shown no interest in continuing to supply spare parts. Over the years, the Simulator Services Department has undertaken several projects. These projects were carried out aiming at different goals: (i) solving the problem with spare parts scarcity, (ii) modifying the simulator to adapt it to increased usage requirements, or (iii) upgrading the simulator to improve its reliability. One such project is the re-design of the Bus Interface Controller used in the I/O system of the simulator. The Bus Interface Controller is probably the most important piece of hardware in the whole I/O system. As such, it is important that reliability evaluation of the new design be carried out.

Reliability has become increasingly important in the design of engineering systems. The key factor driving this is the demand of the customers [6]. The Darlington simulator usage time has always been consistently high, sometimes reaching the level of continuous use during some periods of the past years. The increase usage requirement creates a demand for higher availability, while the allocated maintenance time has been cut back substantially. The only way to meet this demand is to have better designs, where reliability consideration and evaluation are incorporated into the design cycle. Following this design methodology, during the early design cycle of the new Ethernet Bus Interface Controller, an analysis was done to evaluate its reliability. This report presents the details of the analysis and compares the reliability of the new design with the existing one.

LIST OF ABBREVIATION

BIC	: Bus Interface Controller
BOM	: Bill of Materials
CAE	: Canadian Aviation Electronics
COTS	: Commercial Off-The-Shelf
DACBUS	: Data Acquisition and Control bus. Proprietary bus system developed by CAE
DSA	: DACBUS-SCS Adapter
DCC	: Digital Control Computer
eBIC	: Ethernet Bus Interface Controller
FIFO	: First In First Out
I/O	: Input Output
IOB	: Input Output Buffer
MCP	: Main Control Panel
MCPI	: Main Control Panel Interface
MCR	: Main Control Room
MIPS	: Millions of Instructions Per Seconds
MTBF	: Mean Time Between Failure
MTTF	: Mean Time To Failure
MTTR	: Mean Time To Repair
OS	: Operating System
PCI	: Peripheral Component Interconnect
RAM	: Random Access Memory
SCS	: Simulation Computer System
SIMH	: Computer History Simulation System. It can be deployed to simulate a variety of computer systems, including PDP, VAX, IBM, etc…
VHSIC	: Very-High-Speed Integrated Circuit
VLSI	: Very-Large-Scale Integration
VME	: VERSAmodule Eurocard. Bus system developed by Motorola

CHAPTER 1: INTRODUCTION

1.1 BACKGROUND

Ontario Power Generation (OPG) currently has three generating stations in its nuclear fleet: Pickering A, B, and Darlington nuclear power plant (NPP) Each has a corresponding fullscope replica simulator, where licensed shift personnel are trained, certified and re-qualified, as required by law. Among the three simulators, the Darlington simulator is the newest one, originally built by Canadian Aviation Electronics (CAE) in the late 1980s. It was placed in service in 1989 and has been maintained by the simulator service department. The computer equipment and electronics with which the simulator was built are typical of the mid 1980's. For instance, the Encore Seahawk 32/2040 was used as simulation computer, while Ramtek 9400 was used as the display system. Over the years, as the simulator aged, reliability and parts obsolescence have become increasingly problematic. A number of projects have, therefore, been carried out to resolve these issues. A few important projects in recent years are the upgrade of the simulator computer system (SCS), the emulation of the PDP11-70 station digital control computer (DCC), with the SIMH emulator, and the redesign of the I/O system. A simplified post-upgrade block diagram of the simulator is depicted in figure 1. As shown, the simulator consists of the main control panel (MCP), the main control panel interface (MCPI), and the simulation computer system (SCS). The SCS is an Alpha ES40 server running Tru64 Unix OS hosting the simulation software, which runs in real time. The MCPI comprises of a set of fan-out and I/O cabinets through which the simulation software controls the panel devices. The MCP is a set of panels mimicking the real control panels at the station. In addition, the simulation software employs a display sub-system to display various kinds of graphical data, such as trend, alarms summary, etc. The display system includes a set of standard PCs running Exceed, acting as local X

servers for the simulation software. Finally, the PDP 11/70 digital control computer (DCC) is emulated in the simulator using the SIMH emulator.

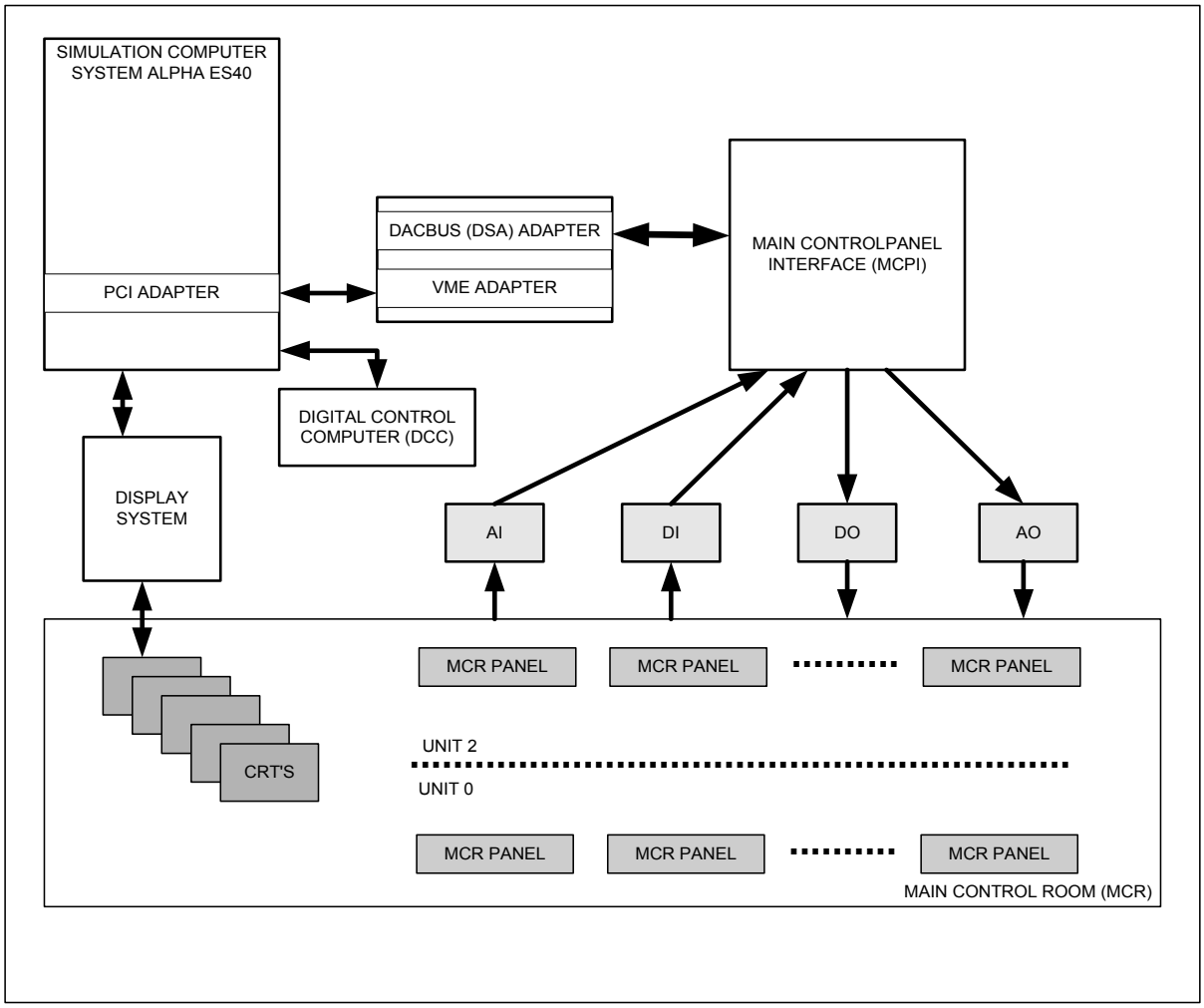

Figure 1: Simplified Simulator Block Diagram

Of all the sub-systems of the simulator, the MCPI is most relevant to this project. A detailed block diagram of the existing MCPI is presented in figure 2. As shown, the MCPI consists of several I/O cabinets connected to two fan-out chassis. The SCS communicates to the MCPI fan-out chassis through the PCI-VME adapters and the DSA (DACBUS – SCS Adapter) boards. The data transfer between the fan-out chassis and

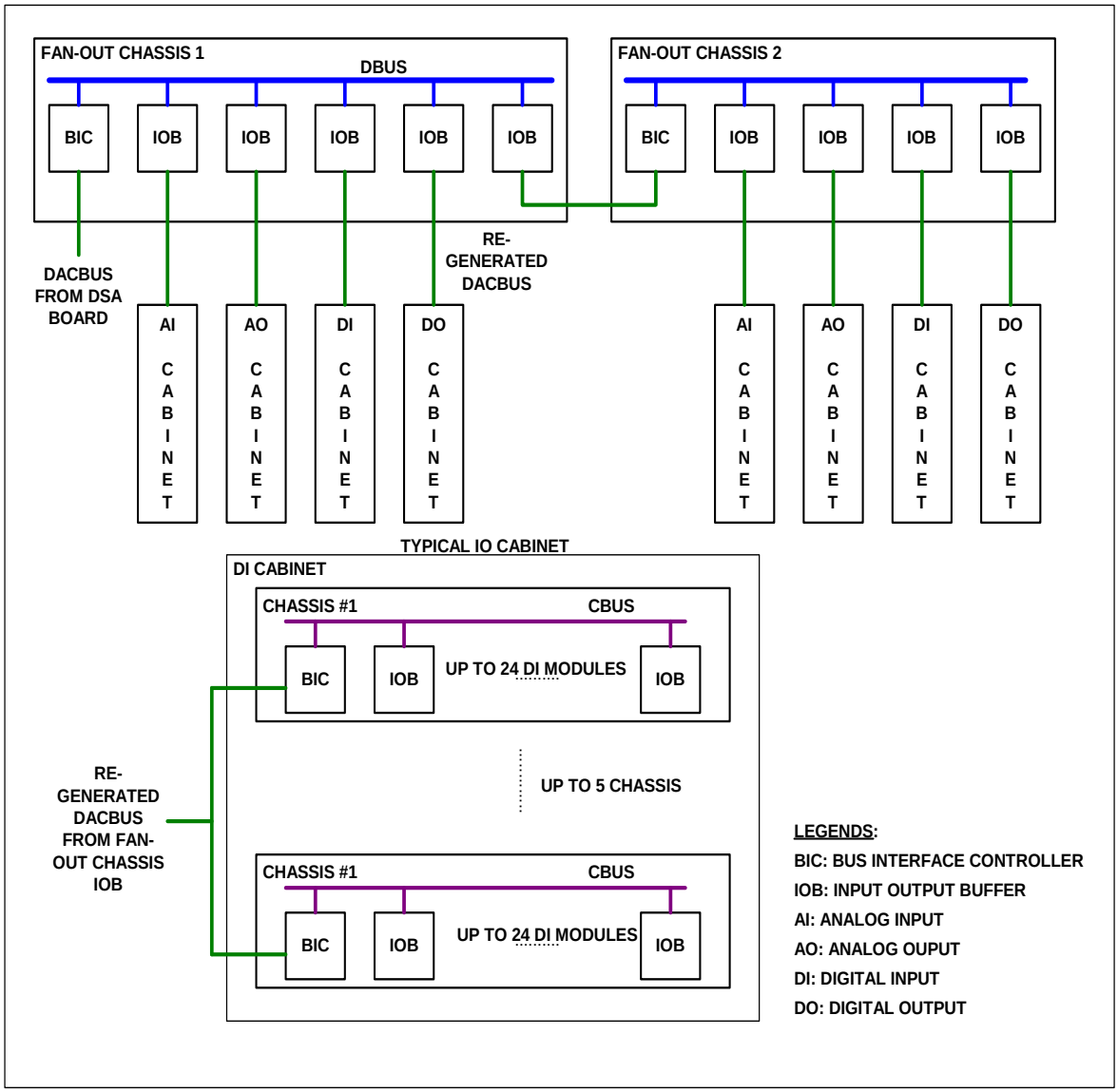

Figure 2: Main Control Panel Interface (MCPI)

the I/O cabinets is handled by a number of BIC and IOB cards. This architecture suffers one major shortcoming regarding to the maintainability and, more importantly, the availability of the whole system: all communication to the MCPI system relies on the first BIC in the chain. It represents the weakest link, whose failure would render the whole I/O system unavailable. In a similar fashion, if any particular IOB card fails, the whole I/O cabinet associated with that IOB will stop functioning. In other words, this

architecture represents a single point of failure system. The system would have to be redesigned, either partially or entirely, if reliability and maintainability are to be improved. An investigation was launched to look into feasible design approaches to address the shortcoming of the existing I/O system and it was decided that a new BIC (called eBIC) be designed. Its mission is to replace the existing BIC and eliminate all intermediate hardware components between the SCS and the MCPI. In doing so, the hardware configuration is greatly simplified, resulting in higher system robustness and hence higher reliability. The new MCPI hardware configuration is depicted in figure 3.

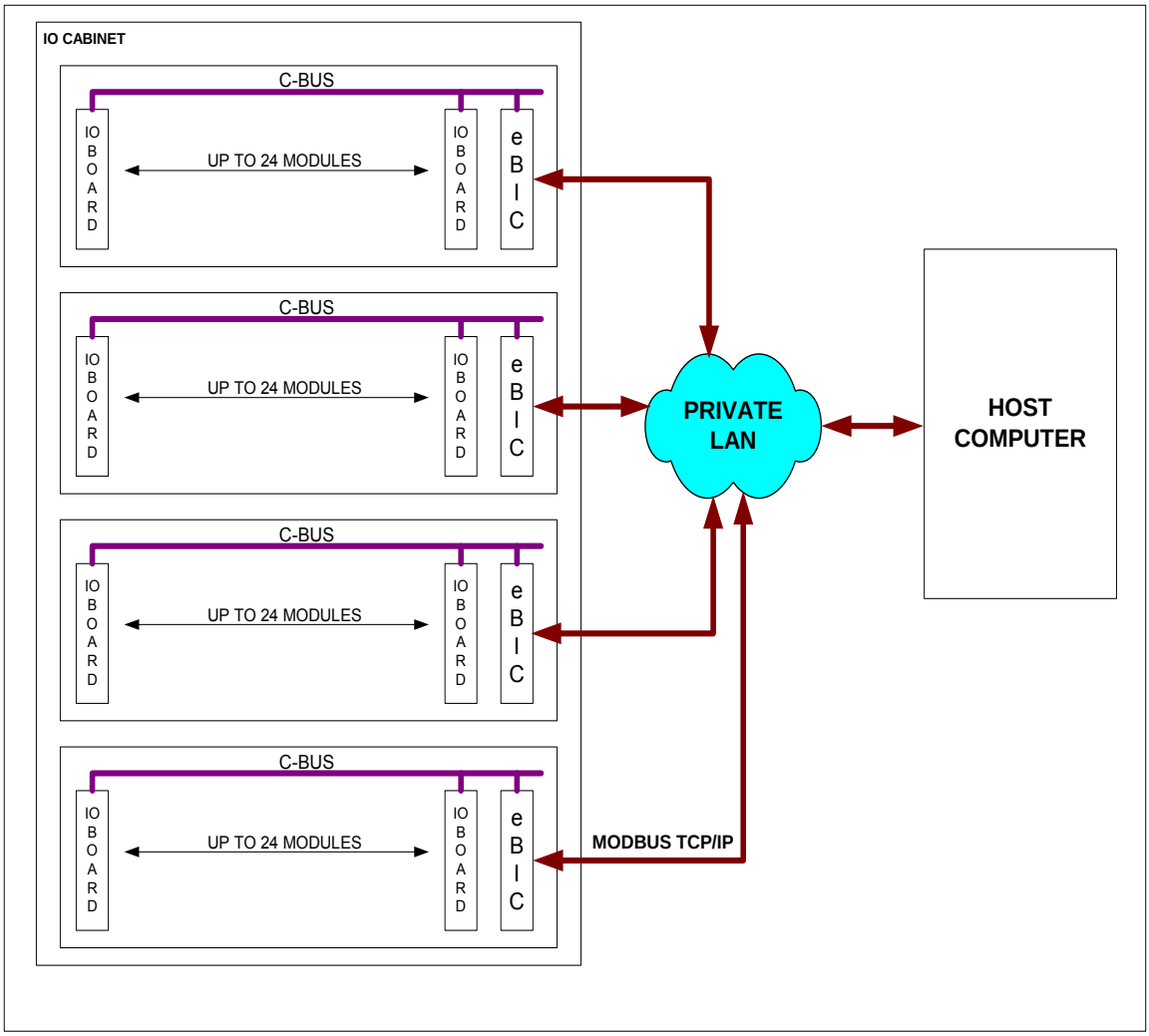

Figure 3: New eBIC Design

The new configuration possesses many advantages, among them those most critical are as follows:

1. Each I/O chassis is individually connected to the SCS via Ethernet.
2. The whole VME chassis is eliminated.
3. The two fan-out chassis are entirely eliminated.
4. All intermediate circuit boards, such as the PCI-VME adapters, the DSA board, and the IOB are eliminated.

1.2 OBJECTIVES

As described, the scope of the change to the I/O system is rather significant, and the success of the new design depends largely on the reliability of the newly designed eBIC. As such, it becomes inevitable that the reliability of the new eBIC must be evaluated. This M. Eng project proposes that such a reliability prediction analysis be performed on not only the newly designed board, but also on all the boards that it is supposed to replace. The reliability of the new and existing systems will be compared against one another, and recommendation on further improvement, if any, on the new design, will be drawn based on the results of the analysis.

1.3 SCOPE OF THE PROJECT

The reliability prediction analysis will cover the following components:

(i) Existing architecture:

- The Bus Interface Controller.
- The Input Output Buffer.
- The DSA board.

(ii) New architecture:

- The Ethernet Bus Interface Controller.

As for the other two circuit boards belonged to the existing architecture, namely the PCI-VME adapters, the reliability prediction reports obtained from the manufacturer will be used, as the BOM and schematic are not provided to buyers, as normally the case with commercial off-the-shelf products.

Other hardware components belonged to the old system, such as the VME chassis and the fan-out chassis will not be evaluated, due to the lack of data.

1.4 REPORT ORGANIZATION

This report consists of the following chapters:

Chapter 1 provides the background of the project, its scope and motivation.

Chapter 2 outlines the theoretical background needed in carrying out the project.

Chapter 3 presents the reliability prediction analysis of the I/O interface architectures involved.

Chapter 4 summarizes the result of the project work and makes recommendation as to future works.

CHAPTER 2: FUNDAMENTALS OF RELIABILITY THEORY

2.1 KEY CONCEPTS IN RELIABILITY ENGINEERING

Since the objective of the project is to perform reliability prediction on the two above-mentioned I/O architectures, this section will only present the reliability concepts applicable to the prediction methods, rather than the modeling aspect of reliability. In the following, definition of reliability, key concepts and prediction methods will be presented.

2.1.1 Definition

Reliability is defined as the ability of a system or component to perform its required functions under stated conditions for a period of time [1].

The reliability function is expressed as:

$$R(t) = 1 - F(t) \tag{2.1}$$

F(t) is the cumulative distribution function, or the unreliability function. It is defined as:

$$F(t) = \int_{-\infty}^{t} f(t)dt \tag{2.2}$$

Where $f(t)$ is the probability density function, representing the failure probability of the random variable [2].

If the failure rate is constant, exponential distribution can be used to model the reliability function [5]. For exponential distribution, the density function is expressed as [6]:

$$f(t) = \lambda e^{-\lambda t} \qquad t \geq 0, \lambda \geq 0 \tag{2.3}$$

Where λ is defined as the constant failure rate.

Since *f(t)* is only defined for t ≥ 0 for exponential distribution, evaluating the integral in (2.2) gives

$$F(t) = 1 - e^{-\lambda t} \tag{2.4}$$

The reliability function can then be re-written as:

$$R(t) = e^{-\lambda t} \tag{2.5}$$

The graphs of typical density and reliability functions are illustrated in figure 4 and 5.

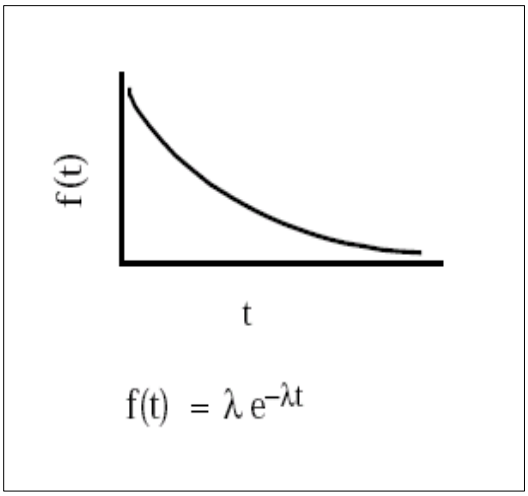

Figure 4: Exponential Density Function

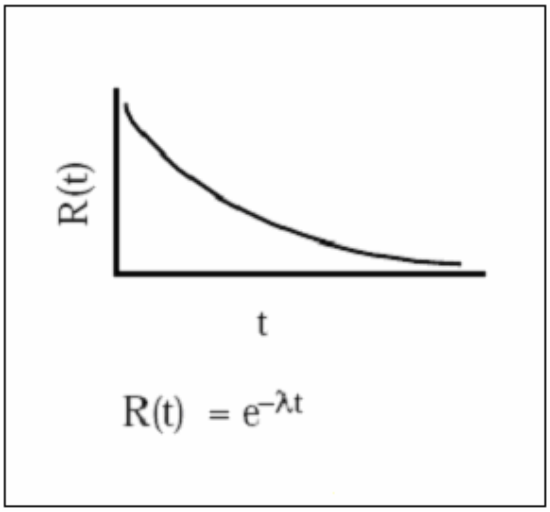

Figure 5: Exponential Reliability Function

2.1.2 Constant Failure Rate

The constant failure rate can be used since it is true for most electronics systems, where

moving parts are not present [4]. The widely used bathtub curve, depicted in figure 6, can be used to illustrate the concept of constant failure rate. On the graph, the first interval represents the decreasing failure rate (also called infant mortality period), where high initial rate is seen; due mainly to the lack of adequate quality control. The high failure rate in this interval can normally be reduced by the use of "burn-in" test, where the parts are operated at maximum operating conditions, in order to speed up the failure mechanism, so that early failures can be screened out [3]. The middle interval of the curve represents the period of usefulness, or the lifetime, of the equipment. During this period, the failures are mostly by random, having a number of possible causes such as human factors, usage outside specified boundaries (i.e. higher stresses), or low design factors [4]. The last interval – the wear out period, is characterized by an increasing failure rate representing the natural deterioration of the equipment as a result of the aging process or due to the depletion of material [22].

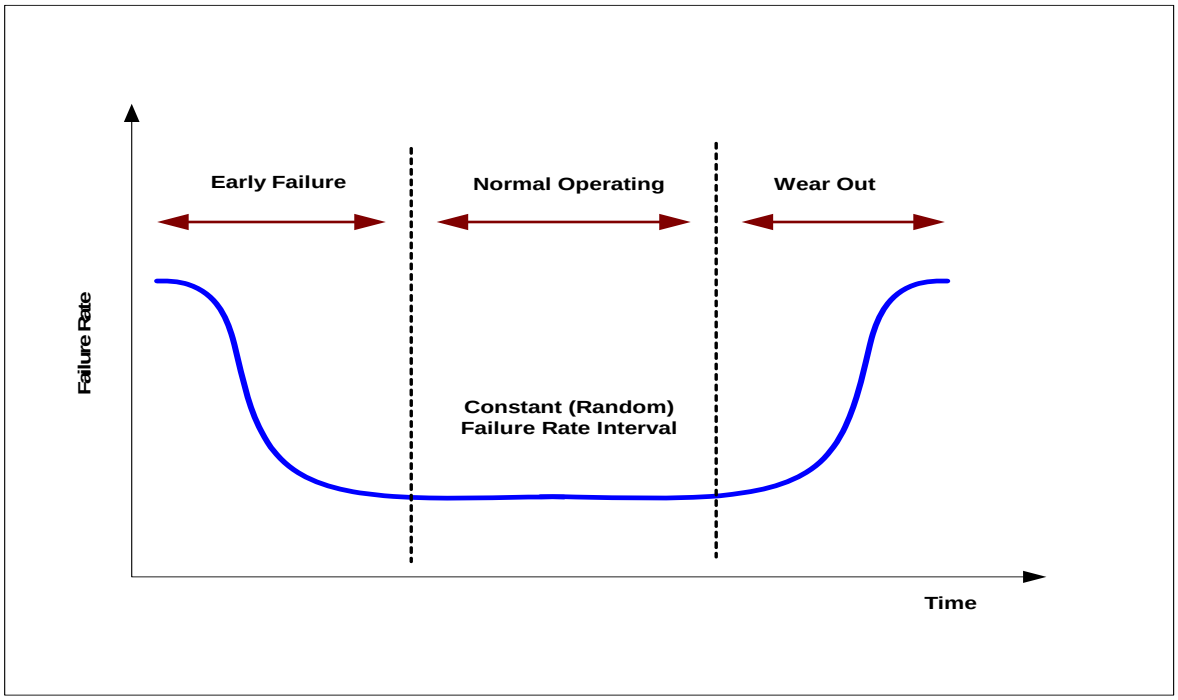

Figure 6: BathTub Curve - Failure Rate vs. Time

2.1.3 Mean Time Between Failure (MTBF)

MTBF is defined as the expected time between consecutive failures in a system or component [1]. It is expressed as:

$$\text{MTBF} = \frac{1}{\lambda} \tag{2.6}$$

Where λ is the constant failure rate, as mentioned above.

The reliability function can then be expressed in terms of MTBF as [2]:

$$R(t) = e^{-t/MTBF} \tag{2.7}$$

2.1.4 Mean Time To Repair (MTTR)

MTTR is defined as the expected time required to repair a system or component to bring it back to its normal (working) state [1]. It can be thought of as a measurement of maintainability. It follows that the higher the MTTR, the lower the maintainability.

2.1.5 Mean Time To Failure (MTTF)

MTTF is the expected time to failure and is defined as [2]:

$$MTTF = \int_0^\infty tf(t)dt \tag{2.8}$$

From [2.1] and [2.2],

$$R(t) = 1 - \int_{-\infty}^{t} f(t)dt$$

Since unreliability has no meaning for t < 0, the equation can be re-written as:

$$R(t) = 1 - \int_0^t f(t)dt$$

However,

$$\int_0^t f(t)dt = 1 - \int_t^\infty f(t)dt$$

Hence [2],

$$R(t) = \int_t^\infty f(t)dt \tag{2.9}$$

Differentiating gives [2]

$$\frac{dR(t)}{dt} = -f(t) \tag{2.10}$$

Thus,

$$MTTF = \int_0^\infty t\left[-\frac{dR(t)}{dt}\right]dt \tag{2.11}$$

Applying integration by parts yields:

$$MTTF = -[tR(t)]_0^\infty + \int_0^\infty R(t)dt$$

Since tR(t) evaluates to 0, for both t=0 and t=∞, MTTF equation becomes:

$$MTTF = \int_0^\infty R(t)dt \tag{2.12}$$

2.1.6 Availability

Availability is defined as the degree to which a system or component is operational and accessible when required for use [1]. The steady state availability is defined as:

$$A_v = \frac{MTTR}{MTTR + MTBF} \tag{2.13}$$

2.1.7 Maintainability

Maintainability is defined as the ease at which a system can be restored to its operational state, upon failure [1]. It can also be thought as the ease at which the system can be modified, upgraded or expanded to improve its performance, correct its shortcomings, or to adapt it to new requirements. The maintainability function is given as [2]:

$$M(t) = \int_0^t g(t)\,dt \tag{2.14}$$

Where $g(t)$ is the repair rate density function, and is defined as:

$$g(t) = \mu e^{-\mu t} \tag{2.15}$$

μ is the repair rate. For exponential distribution, it is constant and defined as:

$$\mu = \frac{1}{MTTR} \tag{2.16}$$

Equation (2.14) then becomes:

$$M(t) = \int_0^t \mu e^{-\mu t} dt = 1 - e^{-\mu t} \tag{2.17}$$

2.2 RELIABILITY PREDICTION METHODS

There are various methods that have been developed to help with reliability prediction. According to the MIL-HDBK-388 handbook [2], these methods can be categorized into 4 groups: similar item, part counts, stress, and physics-of-failure analysis. In the following a summary of these methods will be presented. The information is mainly based on [2] and [7].

2.2.1 Similar Item Analysis

With this technique, the reliability of the item under consideration can be estimated by

comparing it with similar items whose reliability is known. This is the quickest method to estimate reliability. It is best used early in the design cycle. Using this method, the reliability level of a new component is estimated based on past experiences of similar known components. This method assumes that the new component, due to its similarity with the existing components, will behave in a similar fashion. While this assumption is reasonable, the accuracy of the estimation totally depends on the accuracy of the data collected from the existing components, and care must always be exercised to validate the similarity assumption. For instance, components having the same functionality may not be produced using the same technologies, and therefore may not be considered similar.

2.2.2 Parts Count Analysis

This method estimates the equipment's level of reliability based on the total number of parts utilized. It is normally used in the preliminary stage of the design cycle, when data (stress data, in particular), is not readily available. It can also be useful when one has access to the bill of materials (BOM) but lacks other data that allows the determination of the parts operating conditions (i.e. no detailed schematic). A typical and well known method that employs this concept is the Reliability Prediction of Electronic Equipment MIL-HDBK-217 [6] part counts method. It defines the failure rate of an equipment as the summation of all parts failure rates. The use of this technique requires the following data:

- Generic part types
- Quality of the parts
- Quantity of the parts

The general equation for total failure rate of an equipment is given in the MIL-HDBK-217 handbook as [7]:

$$\lambda_{TOTAL} = \sum_{i=1}^{i=n} N_i \left(\lambda_{gi} \, \pi_{Qi} \right) \tag{2.18}$$

Where

λ_{TOTAL} is the total failure rate of the equipment;

λ_g is the generic failure rate of the i^{th} part;

π_Q is the quality factor of the i^{th} part;

N_i is the quantity of the i^{th} part, and

n is the number of the different part types utilized in the equipment.

As such, in calculating the failure rate of an equipment, one would, for every part type,

1. look up the generic failure rate of that type (i.e. general purpose ceramic capacitor) in one of the tables provided in the MIL-HDBK-217 handbook,
2. multiply it with the corresponding quality factor, then
3. multiply the result with that part type quantity.

These steps are repeated for every part type being used in the equipment. The equipment failure rate is then calculated by summing failure rates of all part types. In the following, two typical part counts tables from the handbook are shown. An example calculation is also presented.

Example:

Referring to table 1 and 2, the failure rate of a hermetically-packaged general purpose diode, having a junction temperature of 50 degree C, operating in a ground benign environment (non-mobile, temperature and humidity controlled), would be 0.0036 failures per 10^6 hours.

$\lambda_{diode} = \lambda_g \, \pi_Q = 0.0036 * 1$

Section #	Part Type	Env→ G_B T_J(°C)→50	G_F 60	G_M 65	N_S 60	N_U 65	A_C 75	A_R 75	A_{UC} 90	A_{US} 90	A_{RW} 75	S_F 50	M_L 65	M_I 75	C_L 60
	DIODES														
6.1	General Purpose Analog	.0036	.028	.049	.043	.10	.092	.21	.20	.44	.17	.0018	.076	.23	1.5
6.1	Switching	.00094	.0075	.013	.011	.027	.024	.054	.054	.12	.045	.00047	.020	.060	.40
6.1	Fast Recovery Pwr. Rectifier	.065	.52	.89	.78	1.9	1.7	3.7	3.7	8.0	3.1	.032	1.4	4.1	28
6.1	Power Rectifier/Schottky Pwr.	.0028	.022	.039	.034	.082	.073	.16	.16	.35	.13	.0014	.060	.18	1.2
6.1	Transient Suppressor/Varistor	.0029	.023	.040	.035	.084	.075	.17	.17	.36	.14	.0015	.062	.18	1.2
6.1	Voltage Ref/Reg. (Avalanche and Zener)	.0033	.024	.039	.035	.082	.066	.15	.13	.27	.12	.0016	.060	.16	1.3
6.1	Current Regulator	.0056	.040	.066	.060	.14	.11	.25	.22	.46	.21	.0028	.10	.28	2.1
6.2	Si Impatt (f ≤ 35 GHz)	.86	2.8	8.9	5.6	20	11	14	36	62	44	.43	16	67	350
6.2	Gunn/Bulk Effect	.31	.76	2.1	1.5	4.6	2.0	2.5	4.5	7.6	7.9	.16	3.7	12	94
6.2	Tunnel and Back	.004	.0096	.0026	.0019	.058	.025	.032	.057	.097	.10	.002	.048	.15	1.2
6.2	PIN	.028	.068	.19	.14	.41	.18	.22	.40	.69	.71	.014	.34	1.1	8.5
6.2	Schottky Barrier and Point Contact(200 MHz ≤ f ≤ 95 GHz)	.047	.11	.31	.23	.68	.30	.37	.67	1.1	1.2	.023	.56	1.8	14
6.2	Varactor	.0043	.010	.029	.021	.063	.028	.034	.062	.11	.11	.0022	.052	.17	1.3
6.10	Thyristor/SCR	.0025	.020	.034	.030	.072	.064	.14	.14	.31	.12	.0012	.053	.16	1.1
	TRANSISTORS														
6.3	NPN/PNP (f < 200 MHz)	.00015	.0011	.0017	.0017	.0037	.0030	.0067	.0060	.013	.0056	.000073	.0027	.0074	.056
6.3	Power NPN/PNP (f < 200 MHz)	.0057	.042	.069	.063	.15	.12	.26	.23	.50	.22	.0029	.11	.29	2.2
6.4	Si FET (f ≤ 400 MHz)	.014	.099	.16	.15	.34	.28	.62	.53	1.1	.51	.0069	.25	.68	5.3
6.5	Unijunction	.016	.12	.20	.18	.42	.36	.80	.74	1.6	.66	.0079	.31	.88	6.4
6.6	RF, Low Noise (f > 200 MHz, P < 1W)	.094	.23	.63	.46	1.4	.60	.75	1.3	2.3	2.4	.047	1.1	3.6	28
6.7	RF, Power (P ≥ 1W)	.074	.15	.37	.29	.81	.29	.37	.52	.88	.037	.33	.66	1.8	18
6.8	GaAs FET (P < 100 mW)	.17	.51	1.5	1.0	3.4	1.8	2.3	5.4	9.2	7.2	.083	2.8	11	63
6.8	GaAs FET (P ≥ 100 mW)	.42	1.3	3.9	2.5	8.5	4.5	5.6	13	23	18	.21	6.9	27	160
6.9	Si FET (f > 400 MHz)	.099	.24	.64	.47	1.4	.61	.76	1.3	2.3	2.4	.049	1.2	3.6	30

Table 1: Generic Failure Rate (per 10^6 hours) for Discrete Semiconductor

Section Number	Part Types	JANTXV	JANTX	JAN	Lower	Plastic
6.1, 6.3, 6.4, 6.5, 6.10, 6.11, 6.12	Non-RF Devices/ Opto-Electronics*	.70	1.0	2.4	5.5	8.0
6.2	High Freq Diodes	.50	1.0	5.0	25	50
6.2	Schottky Diodes	.50	1.0	1.8	2.5	- - - -
6.6, 6.7, 6.8, 6.9	RF Transistors	.50	1.0	2.0	5.0	- - - -
6.13	*Laser Diodes	π_Q = 1.0 Hermetic Package = 1.0 Nonhermetic with Facet Coating = 3.3 Nonhermetic without Facet Coating				

Table 2: Discrete Semiconductor Quality Factor

2.2.3 Parts Stress Analysis

The part counts prediction method is based on generic parts failure rates, and does not take into account the stress factor. Parts failure rates, however, can vary significantly with different levels of stress that the parts are exposed to. The burn-in test is a good

example of the effect of stress on failure rate, where parts are operated in over-stressed conditions (i.e. outside normal operating specifications) to speed up the failure process. Figure 7 illustrates the relationship between stress levels and failure rates [8].

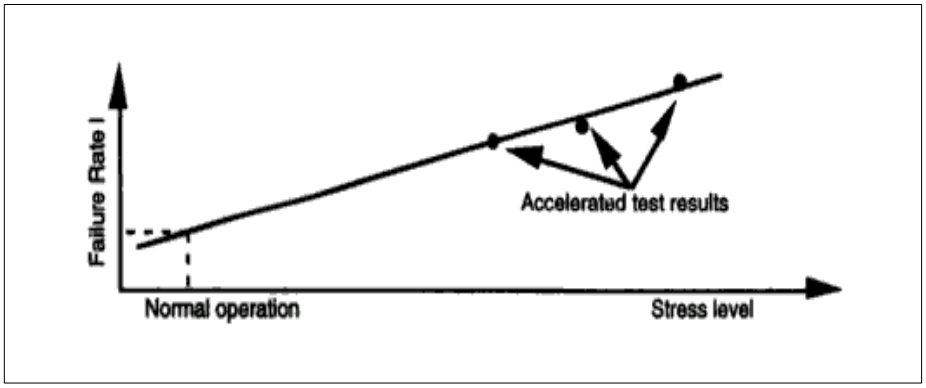

Figure 7: Failure Rate vs. Stress Level

For the above reasons, whenever sufficient data is available, the parts stress method should be used in lieu of the parts count method. According to the MIL-HDBK-217 handbook, the parts stress method should be used when the design is complete, and a detailed parts list and operating data, including stress data are available. This method is based on a set of empirical models fitted to field data to calculate the failure rates of different part types. The most important factors that affect the component failure rate are parts quality, environment factor, and stress applied (i.e. operating temperature and power). The MIL-338 provides a comprehensive list of factors that affect parts reliability. This list is cited in table 3.

Part Type	Influence Factors
Integrated Circuits	• Temperature • Complexity • Supply Voltage
Semiconductors	• Temperature • Power Dissipation • Voltage Breakdown
Capacitors	• Temperature • Voltage • Type
Resistors	• Temperature • Power Dissipation • Type
Inductors	• Temperature • Current • Voltage • Insulation

Table 3: Major Factors on Part Reliability

In the following a few models used to calculate various part types are cited. A sample calculation will then be provided to demonstrate the use of the MIL-HDBK-217 parts stress failure rate models.

Components	Failure Rates (per 10^6 hours)
Microcircuits, gate/logic arrays and microprocessor	$\lambda = (C1\pi T + C2\pi E)\ \pi Q\pi L$
Microcircuits, VHSIC and VLSI CMOS	$\lambda = \lambda_{BD}\pi MFG\pi T\pi CD +$ $\lambda_{BP}\pi Q\pi E\pi PT + \lambda_{BEOS}$
Diodes, low frequency	$\lambda = \lambda_b\pi Q\pi T\pi S\pi C\pi E$
Transistors, low frequency, bipolar	$\lambda = \lambda_b\pi T\pi A\pi R\pi S\pi Q\pi E$
Transistors, high frequency, GaAs FET	$\lambda = \lambda_b\pi T\pi A\pi M\pi Q\pi E$
Resistors, fixed, composition	$\lambda = \lambda_b\pi R\pi Q\pi E$
Resistors, variable, wirewound	$\lambda = \lambda_b\pi TAPS\pi R\pi V\pi Q\pi E$
Capacitor, fixed, paper, by-pass	$\lambda = \lambda_b\pi CV\pi Q\pi E$
Inductive devices, coils	$\lambda = \lambda_b\pi C\pi Q\pi E$
Relays, solid state and time delay	$\lambda = \lambda_b\pi Q\pi E$

Connectors, general (except printed circuit board)	$\lambda = \lambda_b \pi P \pi K \pi E$
Quartz Crystals	$\lambda = \lambda_b \pi Q \pi E$

Table 4: Parts Stress Method Failure Rate Models

Parameters	Description
λ_b	Base failure rate calculated using models that reflect the effect of temperature and stress on the parts.
λ_{BD}	Die base failure rate, based on type of IC (i.e. gate array or logic)
λ_{BP}	Package base failure rate, based on number of pins.
λ_{EOS}	Electrical overstress failure rate, based on voltage range that will cause part failure
$C1$	Die complexity failure rate, based on number of gates
$C2$	Package failure rate for microcircuits, based on number of functional pins and package type (i.e. DIP)
πA	Application factor (i.e. low power, driver, etc.)
πC	Construction factor (i.e. πC = 1 fixed; πC = 2 for variable capacitors)
πCD	Die complexity correction factor for VHSIC & VLSI
πCV	Capacitance factor
πE	Environment factor (i.e. non-mobile ground benign).
πK	Mating factor, based on connecting and disconnecting cycles.
πL	Learning factor, base on number of years in production

πM	Matching network factor (i.e. both input and output are matched or none is matched)
πMFG	Manufacturing process correction factor (i.e. QML or QPL)
πP	Active pin factor
πPT	Package type correction factor (i.e. DIP or SMT)
πR	Resistance factor (for e.g. a >10MOhm resistor will have a πR of 2.5)
πS	Voltage stress factor, based on the ratio of Applied VCE over Rated VCEO. VCEO is the Collector to Emitter voltage with the base open.
πT	Temperature factor, based on junction temperature (T_J)
$\pi TAPS$	Potentiometer taps factor, based on number of taps.
πV	Voltage factor, based on the ratio of applied voltage over rated voltage.

Table 5: Parts Stress Method Failure Rate Factors

Sample calculation:

In the following example, the failure rate calculation of a JAN grade bipolar transistor is shown. Its operating conditions are:

- Operating power, P_{op} = 0.12W, rated at 0.625W.
- Thermal resistance (junction-to-case) θ_{JC} = 83.3^{0}C/W.
- Case temperature, T_C = 35^{0}C.
- Operating voltage is 30% of rated voltage.
- Ambient temperature = 25^{0}C with a specified T_{max} = 150^{0}C.
- Temperature and humidity controlled environment.

- Frequency range < 200 MHz.
- Linear range.

For a bipolar transistor operating at low frequency (i.e. < 200MHz), the failure rate model is [7]:

$$\lambda = \lambda_b \pi T \pi A \pi R \pi S \pi Q \pi E$$

The values of the parameter are calculated in reference to tables 6-12 cited from the handbook. These tables provide the factors required for the failure rate calculation of low frequency bipolar transistors.

1. λ_b = 0.00074 # base failure rate
2. πE = 1.0 # ground benign
3. πA = 1.5 # linear application
4. πS = 0.11 # $0 < \frac{VCE}{VCEO} \leq 0.3$
5. πQ = 2.4 # JAN grade
6. $\pi R = (P_r)^{0.37} = (0.625)^{0.37} = 0.8404$ # for rated power > 0.1W.
7. $T_J = T_C + \theta_{JC} * P_{op}$

   $= 35 + 83.3 * 0.12 = 45^0C$ # [7] and [16]
8. πT = 1.6 # for $T_J = 45^0C$

Thus, the failure rate of the transistor is:

λ = (0.00074)*(1.6)*(1.5)*(0.8404)*(0.11)*(2.4)*(1) = 3.94E-4 (failures/10^6 hours)

Type	λ_b
NPN and PNP	.00074

Table 6: Base Failure Rate - Bipolar Transistor

Application	π_A
Linear Amplification	1.5
Switching	.70

Table 7: Application Factor – Bipolar Transistor

T_J (°C)	π_T	T_J (°C)	π_T
25	1.0	105	4.5
30	1.1	110	4.8
35	1.3	115	5.2
40	1.4	120	5.6
45	1.6	125	5.9
50	1.7	130	6.3
55	1.9	135	6.8
60	2.1	140	7.2
65	2.3	145	7.7
70	2.5	150	8.1
75	2.8	155	8.6
80	3.0	160	9.1
85	3.3	165	9.7
90	3.6	170	10
95	3.9	175	11
100	4.2		

$$\pi_T = \exp\left(-2114\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right)$$

T_J = Junction Temperature (°C)

Table 8: Temperature Factor – Bipolar Transistor

Rated Power (P_r, Watts)	π_R
$P_r \leq .1$	.43
$P_r = .5$	.77
$P_r = 1.0$	1.0
$P_r = 5.0$	1.8
$P_r = 10.0$	2.3
$P_r = 50.0$	4.3
$P_r = 100.0$	5.5
$P_r = 500.0$	10

$\pi_R = .43$	Rated Power ≤ .1W
$\pi_R = (P_r)^{.37}$	Rated Power > .1W

Table 9: Power Rating Factor - Bipolar Transistor

Applied V_{CE}/Rated V_{CEO}	π_S
$0 < V_S \leq .3$	.11
$.3 < V_S \leq .4$	.16
$.4 < V_S \leq .5$	.21
$.5 < V_S \leq .6$	.29
$.6 < V_S \leq .7$	.39
$.7 < V_S \leq .8$	.54
$.8 < V_S \leq .9$	.73
$.9 < V_S \leq 1.0$	1.0

π_S	=	$.045 \exp (3.1(V_S))$ $(0 < V_S \leq 1.0)$
V_S	=	Applied V_{CE} / Rated V_{CEO}
V_{CE}	=	Voltage, Collector to Emitter
V_{CEO}	=	Voltage, Collector to Emitter, Base Open

Table 10: Voltage Stress Factor - Bipolar Transistor

Environment	π_E
G_B	1.0
G_F	6.0
G_M	9.0
N_S	9.0
N_U	19
A_{IC}	13
A_{IF}	29
A_{UC}	20
A_{UF}	43
A_{RW}	24
S_F	.50
M_F	14
M_L	32
C_L	320

Table 11: Environment Factor - Bipolar Transistor

Quality	π_Q
JANTXV	.70
JANTX	1.0
JAN	2.4
Lower	5.5
Plastic	8.0

Table 12: Quality Factor - Bipolar Transistor

2.2.3.1 Other Stress Analysis Techniques

Besides the MIL-HDBK-217, there are several other prediction techniques. Among them the most popular are Bellcore (Telcordia), HRD5, NTT Procedure, and RDF 2000. These techniques will be briefly described below.

- Telcordia [23]: Telcordia's reliability prediction procedure (RPP) was developed by AT&T Bell Labs in 1975 and later issued by Bellcore (which later became Telcordia) in 1984. It was originally developed mainly for use in the telecommunication industry, but has been used in other industries as well.

Telcordia method allows the incorporation of additional data such as burn-in, field and laboratory into the reliability prediction. This method also allows the calculation of infant mortality rate. In general, the RPP includes three different calculation models: method I (previously known as the black box method), method II (previously known as the black box method integrated with laboratory data), and method III (previously known as the black box method integrated with field data). Method I is, in general, similar to the MIL-HDBK-217, and is based on generic failure rates. Method II combines the generic failure rates and the weighted laboratory data. Method III combines the generic failure rates and the weighted field data.

- HDR5: HDR5 is the British telecom handbook of reliability data used primarily, as Telcordia, in the telecom industry. It is, in general, less detailed than the MIL-HDBK-217 [15].
- NTT Procedure: This procedure was developed by the Nippon Telegraph and Telephone Corporation as a means to determine the reliability for semiconductor devices. This procedure uses one temperature acceleration factor for all components, while other procedures use different factors for different components [24].
- RDF 2000 [23]: previously known as CNET, RDF 2000 is a French telecom standard developed by the Union Technique de l'Ectricite, this method is rather different than other methods, in that it combines empirical model with mission profiles including operational cycling thermal variations.

2.2.4 Physics-of-failure analysis

This science-based physics-of-failure method makes use of detailed fabrication and materials data in modeling parts failure mechanism by utilizing the root cause analysis of

failure such as fatigue, fracture, wear, and corrosion [9]. For electronic equipment, the physics-of-failure method can be used to perform:

- Circuit card vibration and thermal analysis.
- Circuit card failure mechanism modeling and life prediction.
- Device level failure mechanism.
- Accelerated test design.
- Box-level thermal analysis.
- Virtual qualification.
- Probabilistic modeling.
- Technology expansion assessments.
- Commercial off-the-shelf (COTS) product evaluation.

The difference between physics-of-failure method and others is the fact that this approach can be incorporated into early design cycle to effectively prevent, detect and/or correct failures [10].

2.2.5 State of the art – newer methodologies

In 2006, the Reliability Information Analysis Center (RIAC), released a new method called 217Plus, as an alternate to the long overdue MIL-217. While largely based on the its predecessor (MIL-217), 217Plus incorporates new aspects of reliability modeling to increase the accuracy of the prediction. These can be listed as:

- Process grades: To address the fact that single part failure is not the sole factor that accounts for system failure, process grades take into accounts the effect of manufacturing and design process on reliability. As such, factors including manufacturing, part quality, design, system management, induced and no-defect-found, wear-out, growth, and can-not-duplicate are covered during the

prediction process. As an example, in the part quality section, questions such as how and with which standards the parts are selected are to be answered.

- Infant mortality and environmental factors: the prediction also considers conditions during screening tests, such as temperature and vibration type, stress condition, detection efficiency, estimated percentage of infant mortality, and instantaneous failure time base.
- Predecessor analysis: in case the new system is built out of an existing one, the existing system's predicted failure rate and actual failure rate are combined into an average failure rate which is subsequently used in the reliability prediction of the new system.
- In addition, Bayesian analysis is used to improve the accuracy of the prediction by factoring in test data (with optional acceleration factor) such as number of failure during tests and the duration of the tests.

Before being named 217Plus this model was known as PRISM (Reliability Prediction and Database for Electronic and Non-Electronic Parts). This was the time when it was still owned by RAC. The PRISM system failure rate model is [14]:

$$\lambda_S = \lambda_{IA} \cdot (\Pi_P \cdot \Pi_{IM} \cdot \Pi_E + \Pi_D \cdot \Pi_G + \Pi_S \cdot \Pi_G + \Pi_M \cdot \Pi_{IM} \cdot \Pi_E \cdot \Pi_G + \Pi_I + \Pi_N + \Pi_W) + \lambda_{SW} \quad (2.19)$$

Where the factors are defined as follows:

λ_{IA}: Initial assessment of the failure rate of the system;
Π_P: Parts process multiplier;
Π_{IM}: Infant mortality;
Π_E: Environmental;
Π_D: Design process;
Π_G: Reliability growth;
Π_S: System management process;
Π_M: Manufacturing process multiplier;
Π_I: Induced process;

Π_N: No-defect process;
Π_W: Wear-out process multiplier, and
λ_{SW}: Software failure rate detection.

Of the above factors, the initial assessment failure rate is derived from the RAC Rates failure rate model and RAC database, combined with user-defined failure data. Other factors are determined using a rigorous question and answer process to confirm measures are taken to improve reliability during design, manufacturing and management process. The RAC Rates are component reliability prediction models where a separate failure rate is used for each generic class of failure of a component. In addition, these rates are accelerated by an appropriate stress multiplier. The model takes the following form [14]:

$$\lambda_p = \lambda_o \cdot \Pi_o + \lambda_e \cdot \Pi_e + \lambda_c \cdot \Pi_c + \lambda_i + \lambda_{sj} \cdot \Pi_{sj} \quad (2.20)$$

Where the factors are defined as follows:

λ_p: Predicted failure rate;
λ_o: Failure rate resulting from operational stress;
Π_o: Product of failure rate multiplier resulting from operational stress;
λ_e: Failure rate caused by environmental stress;
Π_e: Product of failure rate multiplier resulting from environmental stress;
λ_c: Failure rate due to temperature or power cycling stress;
Π_c: Product of failure rate multiplier for cycling stress;
λ_i: Failure rate due to induced stress;
λ_{sj}: Failure rate from solder joint;
Π_{sj}: Product of failure rate multiplier for solder joint stress.

FIDES

This newest methodology is the result of a joint effort between the French Ministry of Defense and a group of aeronautical companies [14]. According to the FIDES group [11], the goal of this (constant failure rate) methodology is to provide a means to realistically predict reliability of systems, especially for those operating under severe

conditions, such as those found in transport, defense or aeronautical. Meanwhile, the methodology also intends to create a concrete tool set to aid in developing and controlling reliability.

FIDES covers both intrinsic and extrinsic failures. The former depends on factors such as item technology and distribution quality, while the latter depends on equipment specification, design, production, and integration, plus procurement route selection [12]. In its simplest form (i.e. top level), the FIDES model can be expressed as:

$$\lambda_{Item} = \lambda_{Physical} \bullet \Pi_{Part\ Manufaturing} \bullet \Pi_{Process} \tag{2.21}$$

As shown, the item failure rate (λ_{Item}) depends on the physical contribution, the quality and manufacturing technical control ($\Pi_{Part\ Manufaturing}$), and the processes, including all from development to field operation and maintenance.

The physical contribution can be expressed as:

$$\lambda_{Physical} = \left[\sum_{PhysicalContribution} (\lambda_0 . \Pi_{Acceleration}) \right] . \Pi_{Induced} \tag{2.22}$$

Where λ_0 denotes the base failure rate; $\Pi_{Acceleration}$ denotes the acceleration factor which reflects the sensitivity to usage conditions, and $\Pi_{Induced}$ represents the induced factors that reflect the actual field conditions, such as over-stresses.

$\Pi_{Part\ Manufacturing}$ represents component quality and can be expressed as:

$$\Pi_{Part\ \_\ Manufacturing} = \exp\left[\delta_1 . (1 - Part\ \_\ Grade) - \alpha_1\right] \tag{2.23}$$

and

$$Part\_Grade = \left[\frac{(QA_{manufacturer} + QA_{component} + RA_{component}) . \varepsilon}{36} \right] \tag{2.24}$$

In the above equations, δ_1 and α_1 represent the correlating factors that dictate how Π_{Part}

$_{Manufacturing}$ affects items reliability; $QA_{manufacturer}$ reflects manufacturer quality assurance criteria; $QA_{component}$ represents component quality assurance criteria, and $RA_{component}$ represents component reliability assurance.

The process factor can be expressed as:

$$\Pi_{\text{Pr}\,ocess} = \exp\ \left[\delta_2.(1 - Process\_Grade)\right] \tag{2.25}$$

The $Process\_Grade$ indicates the process control, and δ_2 represents the correlation factor that dictates the range of the $\Pi_{Process}$.

Among the three methodologies (MIL-217, PRISM and FIDES), MIL-217 takes the most conservative approach. Its results are, therefore, rather pessimistic. The PRISM prediction, on the other hand, tends to be most optimistic, while FIDES stands somewhere in between the other two. According to [12], this is an indication that FIDES is a valid tool.

As of the writing of this report, according to [13], MIL-217 continues to be used by the majority of engineers (80% - according to a Crane survey), despite of the fact that it has not been updated for a long time. This is probably due to the reasons mentioned in [14], which state that the PRISM software is relatively expensive, while the FIDES method is rather new, and perhaps has not been sufficiently validated in practice.

CHAPTER 3: THE RELIABILITY PREDICTION OF THE NEW AND EXISTING BUS INTERFACE CONTROLLERS

3.1 DESCRIPTION OF THE HARDWARE

In this section, a functional description of the hardware components under analysis is provided. As mentioned in chapter I, a total of four circuit boards will be analyzed; three from the existing architect, and one from the new architect.

3.1.1 The existing Bus Interface Controller Architect

- **Bus Interface Controller (BIC)**

  The BIC is essentially a three-port device. These ports are formed by the DACBUS (P3), CBUS (P1) and DBUS (P2) through which the BIC communicates with the host, the I/O cards and the IOB, respectively, as seen from figure 8. For the DBUS, it acts as a relay, simply passing on the data from the host to the IOB. For the CBUS, the BIC acts as a bus master, organizing the data flow between the host and the I/O function cards. A typical transfer cycle starts with an address (ADR) probe, followed by either a data request (DR) or data available (DA) probe from the host. The function card with the matching address will acknowledge the request and send or accept the data, provided that the parity check is satisfactory.

- **IOB**

  In simplest form, the IOB performs the function of a buffer. It is equipped with a set of drivers and receivers to provide the electrical interface between the DBUS and DACBUS. It functions in two modes: relay and receive. In the former mode, the receiver is disabled allowing data to flow directly from the DBUS to the drivers though which the TTL data and control signals are

converted to differential signals and passed on to the remote BIC. In the latter mode, the driver is disabled, permitting the data to flow in the reverse direction: from the DACBUS to the DBUS. The simplified data flow is shown in figure 9.

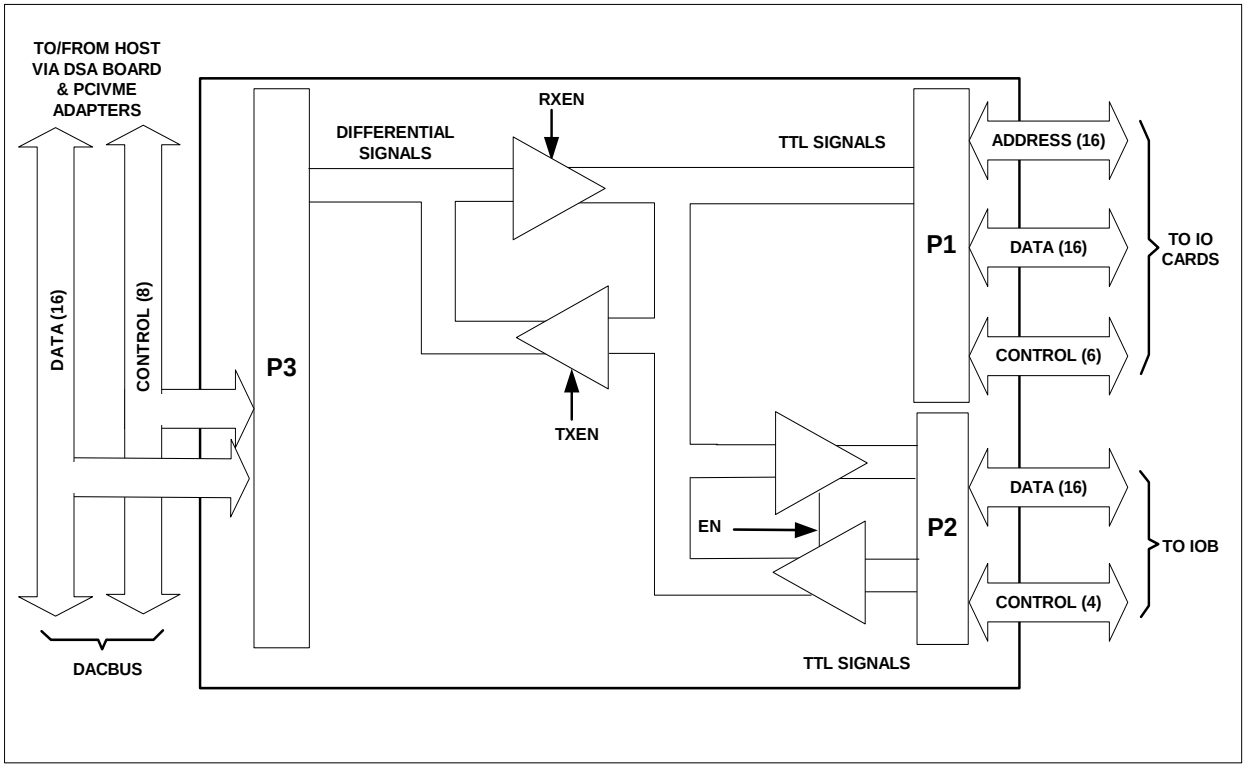

Figure 8: BIC Functional Block Diagram

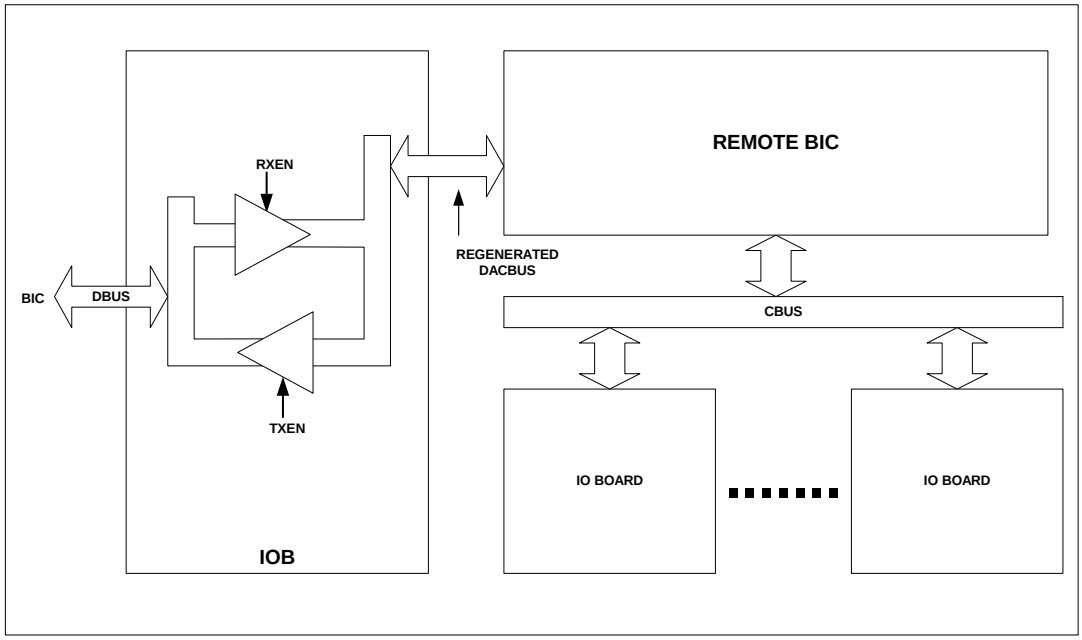

Figure 9: IOB Functional Block Diagram

- **DSA board**

  The DSA board is essentially a bus controller that interfaces two different buses, VME and DACBUS. The latter is a proprietary bus system developed by CAE. The DSA is responsible for the data transfer between the host computer and the MCPI, utilizing the DMA (direct memory address) method. Its main component is a dual port RAM which is mapped into host computer's VME address space. At start up, as part of the initialization, the host downloads all valid DACBUS addresses to the DSA's address table residing in its RAM. During normal operation, the host initiates a transfer cycle which includes a read and a write operation. During the write operation, the host sends a block of I/O data (including host memory address, DACBUS address and word count) to the DSA by writing directly to its data table (which also resides in the RAM). The DSA then writes the data out to the MCPI. During a read operation, the host initiates a data request

to the DSA, which then scans the MCPI and stores the data in its data table. The host then reads the data directly from there. The DSA can operate in two modes: free run, where it continually cycles through each point in its address table, writing to or reading from the MCPI, and trigger, where it scans the MCPI whenever triggered by the hosts. The timing requirement for a transfer cycle is 50 milliseconds. Any errors encountered during the transfer cycles (e.g. address time out) are logged into a serial FIFO (first in first out) memory, where they can be read back to the host for diagnostic purposes. A simplified block diagram of the DSA is presented in figure 10.

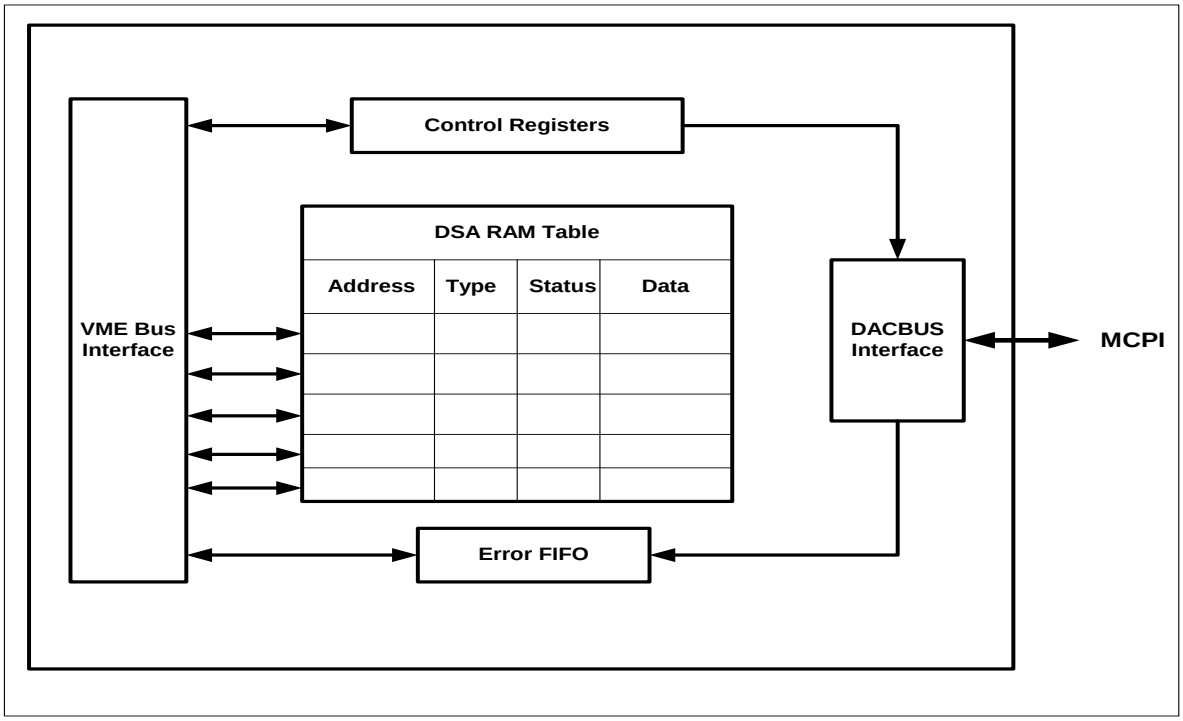

Figure 10: DSA Functional Block Diagram

- **PCI-VME adapters**

  The application software running on the Alpha host computer (Unix Tru64 OS) requires some interface to allow it to communicate to the DSA board. The PCI-VME adapters provide that capability. These bidirectional bus

adapters allow the direct connection between the two bus systems, utilizing the concept of virtual bus to make them work as one. One of its main advantages is that it allows the sharing of memory and a special purpose board between a PCI local bus and VME bus. For the simulator case, this special purpose board is the DSA board. The PCI-VME adapters are manufactured by SBS Technologies. A brochure is attached in appendix G.

3.1.2 The new Bus Interface Controller Architecture (eBIC)

As described above, for the old system, the data flow from the host to the function card goes through several bus systems, namely the PCI, VME, DACBUS, DBUS, and CBUS. This makes the control and interfacing rather complicated. The eBic, by contrast, implemented using the ModBus TCP/IP protocol, is far simpler. Its key components are, as illustrated in figure 11, the microcontroller, the Ethernet controller, the data and control bi-directional drivers, plus the address drivers.

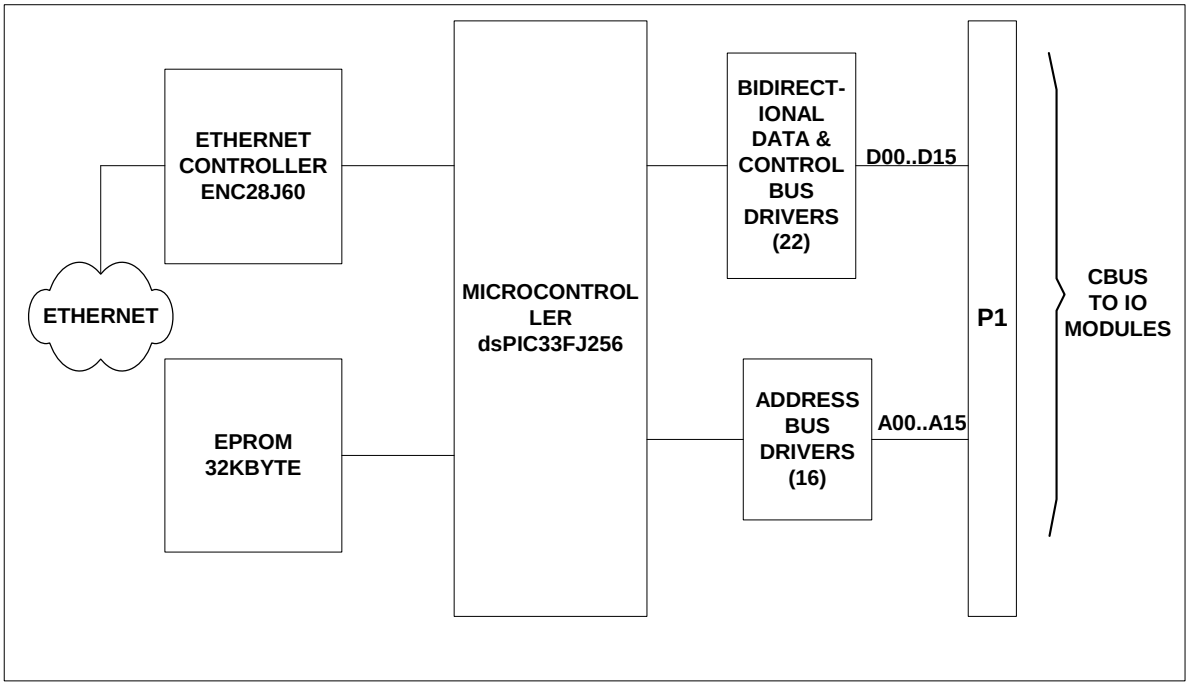

Figure 11: eBIC Functional Block Diagram

- **Microcontroller**

  The microcontroller is a 16-bit, 40 MIPS digital signal controller, with up to 85 programmable digital I/O pins. The controller operates at 3.3V and also provides a built-in A/D converter.

- **C-Bus drivers and receivers**

  These drivers provide the necessary electrical interface between the controller and the function cards. The scanning of the function card is done via the C-bus.

- **Ethernet controller**

  The Ethernet controller is a stand-alone IEEE 802.3 compatible controller, with SPI (serial peripheral interface) via which it communicates with microcontroller.

- **EPROM**

  The memory is basically the storage area for an HTTP server though which on line diagnostic is provided.

3.2 PREDICTION METHOD SELECTION

The prediction method deemed most suitable for the objective of the project is the MIL-HDBK-MIL-217F (Notice 2). It was selected because of the following reasons:

- The analysis will be done at the component level.
- Up-to-date, the company (OPG) still accepts reliability evaluations done using this method from vendors, whenever new electronic designs are to be procured.
- The circuit boards to be evaluated in this project are all used in an OPG environment. As such it makes sense to employ the same method.

- As mentioned earlier, MIL-217 is still being used by 80% of engineers [13].
- For two of the boards in the old system, the PCI- VME adapters, no schematics or parts lists are available. Consequently, reliability reports must be obtained from the vendor. These reports were done using Relex's MIL-217. Thus, it is sensible to employ the same method to evaluate other components.

3.3 SOFTWARE AIDS

Calculating the components failure rates of large, complex circuit board is time consuming. In order to help alleviate the tediousness of the calculation process, it will be essential that software tools be utilized.

Two software package demos were evaluated. These are the Reliasoft's Lambda Predict, and Relex's suite Architect 2007. Both packages offer a wide variety of reliability prediction models in their reliability suites, such as Bellcore, HRD5, RDF 2000, MIL-HDBK-217, etc…While they cost about the same, the Relex suite claims to have a more extensive component library (400,000 as compared to 240,000 from Reliasoft). In addition, as shown in appendixes D and E, the prediction reports provided by the vendor of the PCI-VME adapters (SBS Technologies) are actually prepared using Relex's software. As such it is sensible to use the same tool to analyze the rest of the circuit boards. Consequently, the Relex software was selected as the analysis tool for this project.

3.4 ANALYSIS PROCESS

The analysis process includes the following steps:

1. Gather needed information, such as bill of materials, schematic (where possible), and parts data sheets.
2. Calculate required inputs to the prediction software (i.e. operating power)

3. Calculate the failure rates and MTTB of each circuit board using the prediction software.
4. Summarize the failure rates of the new and existing BICs, and compare the results.

3.5 INPUTS REQUIRED TO THE SOFTWARE

Table 13 shows the inputs required by the Relex software. In addition to these parameters, the global settings such as temperature and environment (i.e. ground benign) must be specified at the board level. A snapshot of the prediction data window for a microprocessor using the MIL-HDBK-217 FN2 (version F, notice 2) is provided in figure 12.

Prediction Method	Part Type	Parameters Required
Parts Count	IC, Microprocessor	Quality Level, Technology, Word Size, Years in Production.
	IC, Logic	Quality Level, Technology, Number of Gates, Years in Production.
	IC, Memory	Quality Level, Technology, Type (i.e. Flotox), Number of Bits, Years in Production.
	Transistor	Quality Level, Power Level (e.g. High or Low).
	Capacitor	Quality Level.
	Resistor	Quality Level, Type (e.g. RN, RL, etc…)
	Inductor	Quality Level, Type (i.e. Fixed or Variable)
	Diode	Quality Level, Type (i.e. rectifier).
	Crystal	Quality Level
	Connector	Quality Level, Connector Type (e.g. RF Coaxial).
Parts Stress	IC, Microprocessor	Quality Level, Technology Type (i.e. MOS), Word Size, Pins, Package, Years in Production, Operating Power, Thermal Resistance.
	IC, Logic	Quality Level, Technology Type (i.e. MOS), Gates, Pins, Package, Years in Production, Operating Power, Thermal Resistance.
	IC, Memory	Quality Level, Technology Type (i.e. MOS), Type (i.e. Flotox), Bits, Package, Years in Production, Operating Power, Thermal Resistance.
	Transistor	Quality Level, Operating Voltage and Power, Thermal Resistance, Application, Voltage and Power Ratings .
	Capacitor	Quality Level, Applied DC Voltage, Voltage Rating, Capacitance, Ambient Temperature.
	Resistor	Quality Level, Operating Power, Type (e.g. RN, RL,etc…), Power Rating

	Inductor	Quality Level, Type (I.e. coil), Hot Spot Temperature.
	Diode	Quality Level, Type (I.e. rectifier), Operating Voltage and Power, Voltage Rating, Construction Type (i.e. Metallurgically), Thermal Resistance.
	Crystal	Quality Level, Frequency.
	Connector	Quality Level, Pairing (i.e. mated), Mating Cycles, Contact Rating, Case Temperature

Table 13: Relex Reliability Prediction Parameters

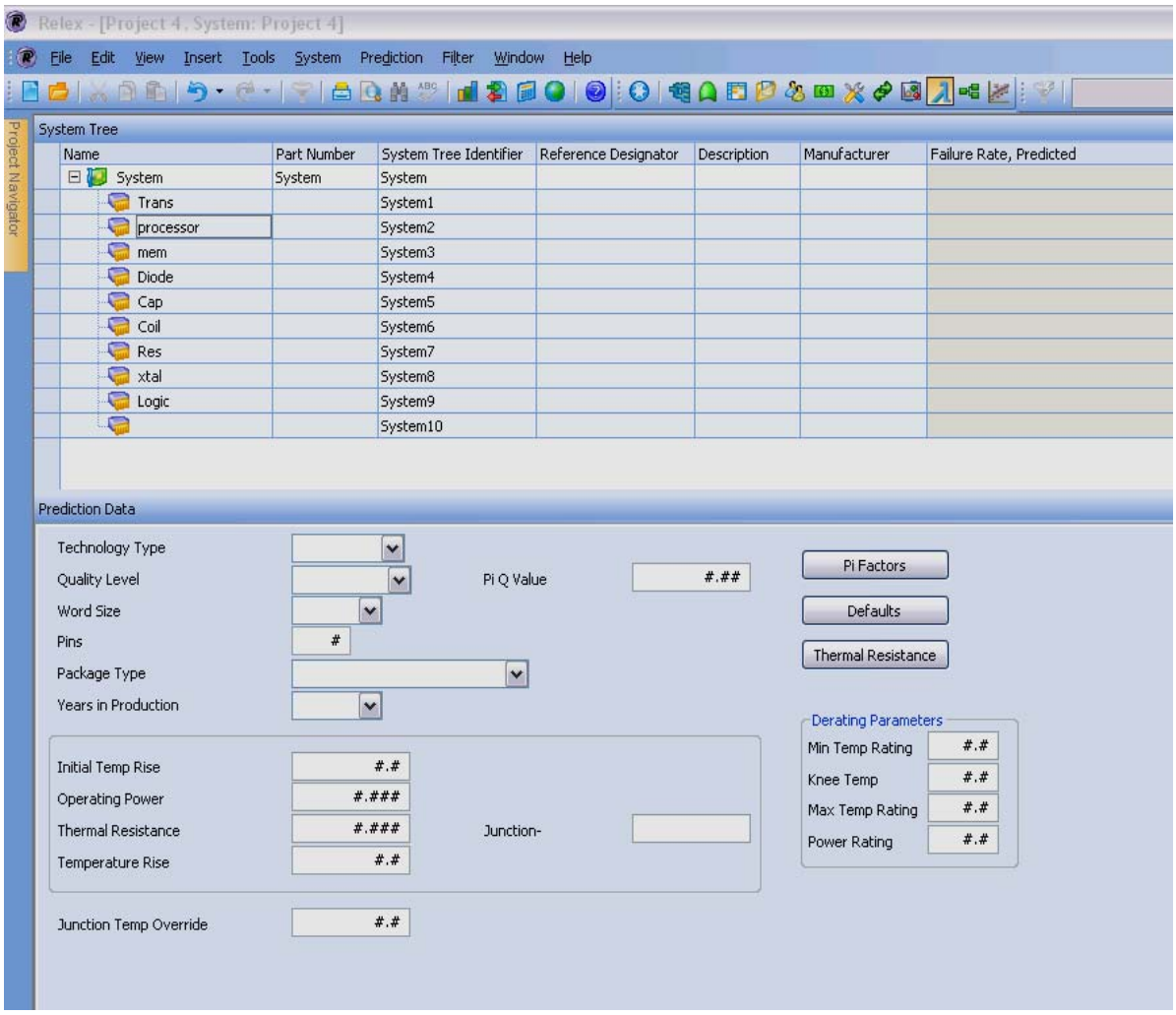

Figure 12: Typical Relex Prediction Data Window

As mentioned above, the Relex's software has an extensive components library. Since information such as technology, maximum ratings (power, voltage and thermal), learning factor (i.e. years in production) are taken care of by the software, the efforts to find and

provide such information are reduced significantly. Other inputs such as applied voltage (DC and AC RMS), and operating power are obtained, either from the designer (as the case of the eBIC), or calculated from the schematics (as the case of the IOB and BIC). A few samples of such calculations are presented below.

- Power dissipation in ICs:

The following equation from the dsPIC33F (shown as U1 in the eBIC Relex report) microcontroller data sheet is used to calculate ICs power dissipation:

$$P_D = P_{INT} + P_{I/O}$$

Where $P_{I/O}$ is the I/O pin power dissipation,

$$P_{I/O} = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$$

and P_{INT} is the internal power dissipation, calculated as

$$P_{INT} = V_{DD} (I_{DD} - \sum I_{OH})$$

In the above equations, the parameters are defined as follows:

- I_{OH}: output current when the output voltage is high.
- I_{OL}: output current when the output voltage is lo.
- V_{OH}: minimum output voltage when the gate is at logic high level.
- V_{OL}: maximum output voltage when the gate is at logic low level.
- V_{DD}: supply voltage.
- I_{DD}: operating current.

A thorough discussion of these parameters, as applied to digital circuits can be found in (17).

From the data sheet,

I_{DD} = 74mA (for 40MIPS); V_{DD} = 3.3V; V_{OH} = 2.4V; V_{OL} = 0.4V;

I_{OH} = -3.0mA; I_{OL} = 4mA

Thus, given the number of I_{OH}'s is 9 (8 data lines, plus one clock), and that of I_{OL}'s is 29 (21 address and control lines, plus 8 data lines), the total power dissipation would be:

$$P_D = 3.3(74-9*3) + [\ 9(3.3-2.4)3.0 + 29*0.4*4] = 0.226W$$

Alternatively, the typical power dissipation can be approximated using I_{DD} and V_{DD}, which results in a power dissipation of 244mW (74*3.3). Since the typical value is larger, for conservative reason, it will be used.

- AC Voltage RMS

In figure 13, a portion of the O/P section of the IOB, presenting a differential data line, is shown. The differential signal can be approximated as a square wave having period of T and a duty cycle of 50%, as shown in figure 14.

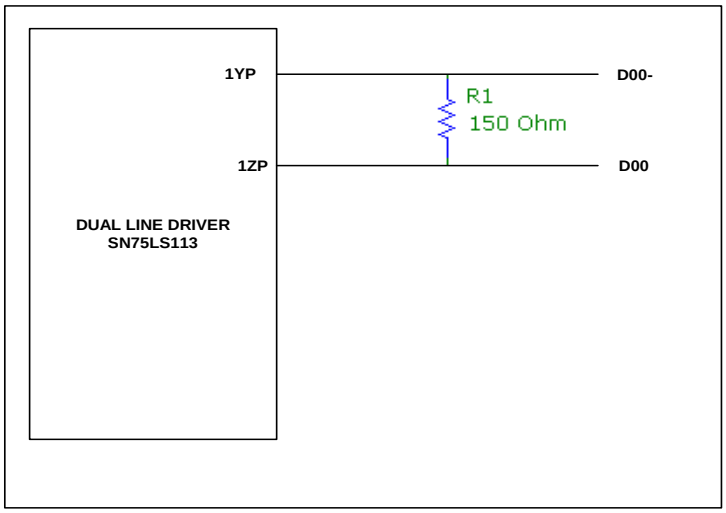

Figure 13: IOB Differential Outputs To DACBUS Cable

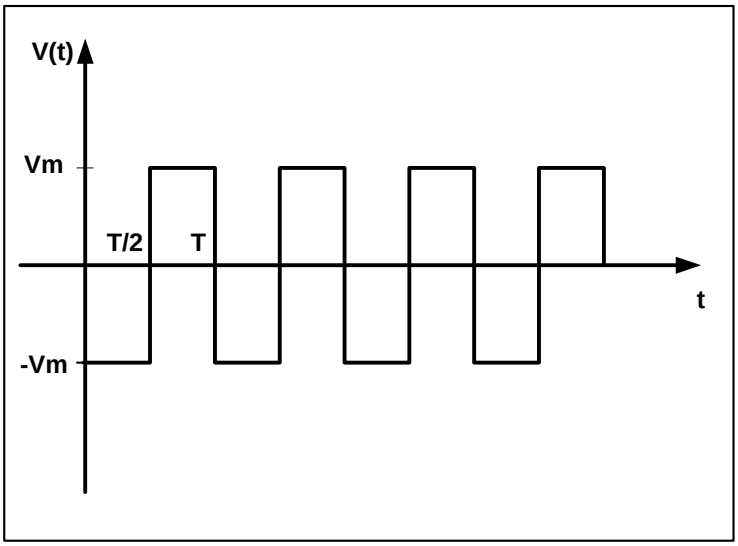

Figure 14: Differential Signals Waveform

The RMS voltage can then be calculated as;

$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V(t)\,dt}$, where

$V(t)$ = -V_m, for $0 < t \leq T/2$, and

$V(t)$ = V_m, for $T/2 < t \leq T$.

Thus,

$V_{rms} = V_m$

Given V_m = 5V, the power dissipated in the resistor can be calculated as:

$P = (5)^2 / 150 = 167mW$.

3.6 ASSUMPTIONS

In performing the reliability prediction of the two I/O architectures, the following assumptions are made:

- The equipment under consideration is in its normal operating life, hence constant

failure rate is assumed.

- The equipment is operating in a non-mobile, temperature and humidity control environment. In light of these conditions, the environmental settings are set at ground benign, 25^0C.
- The equipment is repairable. Otherwise the definition of MTBF, as presented in 2.2.1 does not apply.
- Where detailed schematics or stress data are not available, the parts count prediction method will be used. This condition applies to the DSA board.
- In case where even a part list is not available, the vendor reliability report will be used. This condition applies to the PCI-VME adapters.

3.7 RELIABILITY PREDICTION RESULTS

3.7.1 Prediction Method Summary

As previously mentioned, the prediction method being used to evaluate the individual hardware components is dictated by the availability of data. If both schematic and BOM are available, part stress can be used (as power consumption and voltage level can be calculated); whereas if only BOM is available, part counts is the only option. In the worst case, where neither schematic nor BOM is available, reliability evaluation must be obtained from the vendor. The method used for each hardware component is summarized in table 14.

HW Component	Prediction Method	Comments
EBIC Board	Part Stress	Both schematic and BOM are available
BIC Board	Part Stress	Both schematic and BOM are available
IOB Board	Part Stress	Both schematic and BOM are available

DSA Board	Part Counts	Only BOM is available
PCI Adapter	Vendor Data	Schematic and BOM are not available. Reliability Evaluation provided by vendor
VME Adapter	Vendor Data	Schematic and BOM are not available. Reliability Evaluation provided by vendor

Table 14: Prediction Method Summary

3.7.2 Reliability Analysis Part Data

While appendices A, B C and F show the final failure rates of the hardware components of the old and new system, they do not show the specific part data being used. For this reason, appendix H was provided. It lists all the parameters input into the reliability software to arrive at the results shown in appendices A, B, C and D. Two snapshots taken from appendix H will be used to explain where and how the data is used. Figure 15 shows an excerpt from the specific data listing of the EBIC module. In this figure, the data pertaining to U1 are as follows.

- Type: this field indicates the technology type.
- Quality: commercial grade was used (the eBIC module uses commercial grade parts, while the existing BIC uses military grade).
- Pi Q: a quality factor of 10 was used as recommended by the handbook, since the screening process is not known.
- Word: the IC is 16 bit.
- Pin: the 100-pin version was used in the eBic design.
- Package: the flatpack package was used.
- Years: the number of years in production of equal or greater than 2 was used since the part has been around for a few years.
- Power: the power dissipation as calculated above was used (i.e. 244mW).
- Thermal resistance: a typical thermal resistance of 48.4 for the 100-pin TQFP

(Microchip datasheet) was used.

- Thermal rise: this value is calculated by the software.

File Name: Project 2.rfp (EBIC)
Assembly: System
Ref Des:
Description:

Failure Rate: 4.158803
MTBF (hrs): 240,454
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
MA330011	U1	Type: MOS, Qual: Commercial, Pi Q: 10.00, Word: 16 Bits, Pins: 100, Type: Flatpack, Yrs: >=2.0, OpPwr: 0.244, ThRes: 48.400, TRise: 11.8	1.125343
25LC256	U3	Type: Other, Corr: None, Qual: Commercial, Pi Q: 10.00, Bits: 256, Units: Kb, Pins: 8, Type: DIP, Glass Seal, Yrs: >=2.0, OpPwr: 0.020, ThRes: 171.002, TRise: 3.4	0.014822

Figure 15: eBIC Module Part Stress Data

In figure 16, a snapshot from the specific data listing of the IOB module is shown. As an example, the parameters used for C2-10 are listed below:

- Quality: these capacitors are military grade.
- Operating DC voltage: from the IOB schematic, these capacitors are operating at 5.0V.
- Their rated voltage is 100V.
- Their voltage ratio is calculated by the software.
- Their capacitance is 10nF.

File Name: IO Buffer.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.396088
MTBF (hrs): 294,456
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
CK05BX103K	C2-C10	Qual: Mil-Spec, Op DC: 5.00, RtVt: 100.00, V S/R: 5.0, Cap: 10.000, Units: nF	0.001963
M39003/01-2409	C1	Qual: Mil-Spec, Op DC: 5.00, RtVt: 75.00, V S/R: 6.7, Cap: 3.300, Units: uF, Series: >0.8	0.001042
SN74LS14N	U1	Type: LSTTL, Qual: Commercial, Pi Q: 10.00, Gates: 6, Pins: 14, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.064, ThRes: 28.000, Junct: Case, TRise: 1.8	0.033934

Figure 16: IOB Module Part Stress Data

The data as explained above are used to populate the fields shown in figure 12. The analysis was run and the failure rates are tabulated in the final prediction reports attached in appendices A, B, C and F.

3.7.3 Results

A summary of the prediction results is shown in table 14. Detailed prediction reports will be shown in the appendices.

OLD BIC ARCHITECTURE			
Components	**Description**	**MTBF (hrs)**	**Failure Rate (/10^6 hours)**
1	PCI bus adapter	202,350	4.941934
2	VME bus adapter	156,394	6.394119
3	DSA board	338,328	2.955715
4	IOB board	294,456	3.396086
5	BIC board	290,332	3.444329
Total		**47,321**	**21.132183**
NEW BIC ARCHITECTURE			
1	EBIC board	240,454	4.158803
Total		**240,454**	**4.158803**

Table 15: Reliability Prediction Results

Note: The combined MTBF of the old system is calculated as 10^6 / Total failure rate.

3.7.4 Discussion

From table 15, it is quite evident that the new architecture is far more reliable than the old one. The combined failure rate of the old architecture is 21.132183 (failures per 10^6 hours), around five times higher than that of the new architecture, 4.158803. The main factors that contribute to this much higher failure rate are the parts quality, the components count and the overall system complexity.

3.7.4.1 Parts Quality

Looking at the predictions reports in the appendices, the following can be noticed:

- The highest individual part failure rate is found in the eBIC's report. The failure rate of the digital signal processor microcontroller is 1.125343/10^6 hours. The high rate is mainly due to the complexity of the microcircuit, and a conservative value of the quality factor used in the calculation of the failure rate ($\pi Q = 10$, as recommended in the handbook for products with unknown screening level).
- The failure rates of discrete components are low for the BIC and IOB. It is so because all discrete components used on these boards are of military grade. The eBIC, on the other hand, uses all commercial grade parts, resulting in higher failure rates for its discrete parts.

3.7.4.2 Components Count

The most complex board in the old system is the BIC board. It has a components count

of 214. The components count of the new eBIC, in contrast, is only 52. If one were to add the components of all boards together, the components count of the old system will be several times higher than that of the new system. From the parts count aspect, a higher parts count would likely contribute to a higher system failure rate. O'Connor points out that reducing the number of components and their connections not only reduces the cost, but also improves the reliability [20]. As such, even though better quality parts are used in the old design, its combined failure rate is still higher than that of the new design.

3.7.4.3 System complexity

The existing architecture requires five different circuit boards: the BIC, the DSA board, the PCI-VME adapters, and the IOB, with five different types of buses, namely the PCI bus, the VME bus, the DACBUS, the CBUS, and the DBUS. That is not to mention the two fan-out chassis that are not covered in this analysis, due to the lack of data. This level of complexity of the existing system makes it rather hard to diagnose, repair and maintain. In fact, in order to maintain high availability, preventative maintenance has to be performed on a regular basis. Failed boards are normally replaced instantly with spares, and then repaired later. As such, at any time, a good spare inventory has to be maintained. In addition, the system had occasionally failed in such a way that the provided diagnostic tools fail to pin-point where the problem is. In such situations, lengthy trouble-shootings are entailed. Finally, due to the complexity of the existing system, modifications to the I/O system required for different simulator usage are not easy. For instance, at one point in time, due to the increasing need of simulator usage, it was required that the simulator be split in half, allowing two training sessions to be run simultaneously, one on each side (i.e. Unit 2 and Unit 0). To meet that requirement, the simplest approach was to split the I/O system in half. One half serves Unit 2 control

panels, and the other serves Unit 0. It was found that due to the complexity of the existing system, splitting the I/O in a certain way affects the quality of the signals, due to the use of additional hardware (.i.e. switches), causing the I/O system to intermittently malfunction. In this aspect, it is evident that the existing system is not highly maintainable. For, the ease to adapt to arising requirement is one important aspect of maintainability, as defined in section 2.2.5.

The new design, in contrast, consists of only one board, communicating to the simulation computer via the Ethernet, using MODBUS TCP/IP. The overall architecture is simple and effective, making it easier to maintain, and hence more reliable. In addition, since it is implemented using the well-established MODBUS TCP/IP protocol, a widely used protocol in the industry, it would be easy to modify it to meet future requirement, should such a need arise. Even though the eBIC is still in its design stage, it has already been foreseen that the task of splitting up the simulator as described above, would be straight forward, as no additional hardware is required to achieve that goal. Further, in the existing system, the use of the intermediate circuit boards operating on different types of buses requires different drivers to be written (for instance, the DSA board), or acquired (i.e. the PCI-VME adapters). Such an issue will not arise with the eBIC, as it utilizes the standard TCP/IP protocol. Writing an application to handle the I/O communication is, in general, simpler using TCP/IP, as compared to other bus architectures. Finally, the simulation software is currently running on Tru64 Unix, a soon-to-be obsolete OS. It is inevitable that the simulation software will, sooner or later, have to be migrated to another OS. Be it Windows or be it Linux, the task of converting the I/O application from Unix to other operating systems will not be an issue, as the implementation of the TCP/IP protocol would be greatly similar between different platforms.

3.7.5 Recommendation

As described in section 3.1.1, the timing requirement for a complete I/O transfer cycle is 50ms. This is an important requirement due to the real-time nature of the simulation software application. As of the writing of this report, a program has been written to test the communication of the eBIC to the Alpha computer, and to preliminarily evaluate the performance of the new design. While the board works well, it was observed that timeouts do occur occasionally. Although this is normal for a network application, and the program can be written to minimize the effect of the timeouts (i.e. retry), it would be desirable to not have the timeouts at all. The eBIC is currently built around a 16-bit DSP microcontroller. It is expected that the use of a 32-bit DSP microcontroller will significantly boost the performance of the board, thus eliminating the timeout issue. Further, commercial grade parts are used in the eBIC design; it is expected that using military grade would yield higher reliability.

CHAPTER 4: CONCLUSION

As summarized in the last section, the new eBIC design possesses many outstanding features. It is designed with the capability to adapt to new requirements, be it the expansion of the hardware, or be it the migration of the software application. The eBIC eliminates all intermediate hardware required by the old system, such as the PCI-VME, the DSA, and the IOB circuit boards. As such, it greatly simplifies the hardware architecture. The end results are the reduced cost and the higher maintainability. At the beginning, it is expected that due to its many advantages over the old system, the eBIC will be more reliable and robust. The results of the reliability evaluation have proved just that: the predicted failure rate of the new system is five times lower than the failure rate of the existing system; its predicted MTBF of approximately 27 years looks rather promising, and would even stand out better, considering the (overly) pessimistic nature of the MIL-217. As this is a new design, the incorporation of the reliability evaluation into the design cycle is useful, especially in raising the level of confidence in the new design.

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APPENDIX A: BIC BOARD RELIABILITY PREDICTION REPORT

Relex

Reliability Prediction Summary
Bus Interface Controller (BIC)

Failure Rate: 3.444329
MTBF (hrs): 290,332

Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Category	Ref Des	Unit Failure Rate	Quantity	Total Failure Rate
CK05BX102K	Capacitor	C1-18	0.001595	18	0.028710
CK05BX102K	Capacitor	C20,21,28-,31,68	0.005131	5	0.025657
CK05BX103K	Capacitor	C19,22,36-,67	0.001971	33	0.065054
CK05BX103K	Capacitor	C26,27,29	0.001962	3	0.005887
M39003/01-2409	Capacitor	C23	0.001042	1	0.001042
M39003/01-2409	Capacitor	C24	0.001042	1	0.001042
CK05BX102K	Capacitor	C25	0.001595	1	0.001595
CK05BX102K	Capacitor	C34	0.001595	1	0.001595
M39003/01-2409	Capacitor	C35	0.001579	1	0.001579
CM05FD221F03	Capacitor	C36	0.001068	1	0.001068
CK05BX390K	Capacitor	C69	0.001191	1	0.001191
JAN1N914	Semiconductor	CR4	0.000492	1	0.000492
JAN1N914	Semiconductor	CR1	0.000492	1	0.000492
JAN1N914	Semiconductor	CR3	0.000492	1	0.000492
8T98N	Integrated Circuit	U1,5,10	0.095144	3	0.285431
SN74LS174N	Integrated Circuit	U2,11,14,-22,24,33	0.039246	6	0.235478
SN74LS257AN	Integrated Circuit	U3,6,12,13	0.039246	4	0.156986
SN74LS280N	Integrated Circuit	U4,15	0.039246	2	0.078493
SN74LS10N	Integrated Circuit	U7	0.039246	1	0.039246
SN74LS175N	Integrated Circuit	U8	0.039246	1	0.039246
LM319AN	Integrated Circuit	U9,16	0.095144	1	0.095144
SN7428N	Integrated Circuit	U16	0.036310	1	0.036310
SN74LS00N	Integrated Circuit	U17,28,29-,35	0.039246	4	0.156986
LM311H	Integrated Circuit	U19	0.095144	1	0.095144
316A	Resistor	U20	0.002842	1	0.002842
8T26AN	Integrated Circuit	U21,23,31-,32,46,47,-52,55	0.095144	8	0.761150
SN74LS74AN	Integrated Circuit	U25	0.033755	1	0.033755
SN74LS02N	Integrated Circuit	U26,36	0.039246	2	0.078493
SN74LS04N	Integrated Circuit	U27,30,48	0.039246	3	0.117739
SN74LS132N	Integrated Circuit	U34	0.039246	1	0.039246
SN74LS08N	Integrated Circuit	U37	0.039246	1	0.039246
MC3487P	Integrated Circuit	U38,44,50-,54,58,62	0.036310	6	0.217860
MC3486P	Integrated Circuit	U40,45,49-,53,57,61	0.036310	6	0.217860
LM339AN	Integrated Circuit	U41	0.095144	1	0.095144
SN74LS38N	Integrated Circuit	U42,43	0.039246	2	0.078493
316A	Resistor	U51	0.001895	1	0.001895
SN74LS266N	Integrated Circuit	U56,59,60	0.039246	3	0.117739
RCR07G131JS	Resistor	R1-18	0.000053	18	0.000961
RN55D1002F	Resistor	R19,28	0.000680	2	0.001361
RN55D5902F	Resistor	R20	0.001455	1	0.001455
RN55D4021F	Resistor	R21	0.000948	1	0.000948

Reliability Prediction Summary
Bus Interface Controller (BIC)

Failure Rate: 3.444329

MTBF (hrs): 290,332

Temperature: 25

Environment: GB, GC - Ground Benign, Controlled

Part Number	Category	Ref Des	Unit Failure Rate	Quantity	Total Failure Rate
RN55D4021F	Resistor	R33	0.000538	1	0.000538
RCR07G472JS	Resistor	R22,37,30-,34	0.000066	4	0.000265
RN55D1962F	Resistor	R23	0.002421	1	0.002421
RN55D1001F	Resistor	R24,32	0.000597	2	0.001194
RN55D1001F	Resistor	R69	0.001687	1	0.001687
RN55D1001F	Resistor	R70	0.001191	1	0.001191
RCR07G101JS	Resistor	R25,26	0.000066	2	0.000133
RN55D3652F	Resistor	R29	0.001194	1	0.001194
RN55D1212F	Resistor	R31	0.001809	1	0.001809
RCR07G102JS	Resistor	R36,47,50-,54,64,66,-68,71,84	0.000066	9	0.000596
RCR07G221JS	Resistor	R67,83	0.000066	2	0.000133
RCR07G333JS	Resistor	R44,85	0.000001	2	0.000002
RN55D1052F	Resistor	R45,46	0.000347	1	0.000347
RN55D1542F	Resistor	R48	0.000431	1	0.000431
RN55D1782F	Resistor	R49	0.000424	1	0.000424
RCR07G330JS	Resistor	R51	0.000000	1	0.000000
RCR07G100JS	Resistor	R52,81	0.000001	2	0.000002
RCR07G152JS	Resistor	R57-59	0.000066	3	0.000199
RN55C2740F	Resistor	R60,61	0.002995	2	0.005991
RN55D8660F	Resistor	R62	0.001187	1	0.001187
RN55C3320F	Resistor	R63	0.001026	1	0.001026
RCR07G332JS	Resistor	R79	0.000066	1	0.000066
RCR07G471JS	Resistor	R80	0.000066	1	0.000066
RCR07G331JS	Resistor	R82	0.000000	1	0.000000
RCR07G472JS	Resistor	R78	0.000004	1	0.000004
RCR07G102JS	Resistor	R77	0.000000	1	0.000000
RCR07G221JS	Resistor	R74,40,37-,43,53	0.000001	4	0.000003
RCR07G221JS	Resistor	R76,42,56	0.000000	2	0.000001
RCR07G221JS	Resistor	R35,39	0.000030	2	0.000059
RCR07G131JS	Resistor	R75	0.000020	1	0.000020
RCR07G131JS	Resistor	R38,41,55	0.000066	3	0.000199
182154	Connection	P1-3	0.087531	3	0.262593

APPENDIX B: IOB BOARD RELIABILITY PREDICTION REPORT

Relex

Reliability Prediction Summary
Input OutPut Buffer (IO)

Failure Rate: 3.396088

MTBF (hrs): 294,456

Temperature: 25

Environment: GB, GC - Ground Benign, Controlled

Part Number	Category	Ref Des	Unit Failure Rate	Quantity	Total Failure Rate
CK05BX103K	Capacitor	C2-C10	0.001963	1	0.001963
M39003/01-2409	Capacitor	C1	0.001042	1	0.001042
SN74LS14N	Integrated Circuit	U1	0.033934	1	0.033934
SN75175N	Integrated Circuit	U4-U7,U1-4-U19	0.069590	10	0.695901
SN75LS113	Integrated Circuit	U9-U13,U-19-U25	0.235926	10	2.359261
SN7437N	Integrated Circuit	U8	0.033926	1	0.033926
RCR07G153JS	Resistor	U2,U3	0.000471	2	0.000941
RCR07G150JS	Resistor	R2-R5,R1-6-R32	0.000054	21	0.001124
RCR07G102JS	Resistor	R1,R14	0.000007	1	0.000007
RCR07G221JS	Resistor	R7-8,R11--12,R33,R-35	0.000005	6	0.000032
RN55C3740F	Resistor	R13	0.002285	1	0.002285
RCR07G681JS	Resistor	R9-10,R34	0.001025	3	0.003076
RCR07G153JS	Resistor	R6	0.000002	1	0.000002
182154	Connection	P1-3	0.087531	3	0.262593

APPENDIX C: DSA BOARD RELIABILITY PREDICTION REPORT

Relex

Reliability Prediction
Specific Part Data

File Name: DSA Board.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 2.955715
MTBF (hrs): 338,328
Temperature: 30
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
681-10339	C1,2	Qual: C, T	0.000034
CZ20C104M	C3-52	Qual: Mil-Spec	0.076353
A-10.000000-18	X1		0.031967
5309K1	D1		0.003565
XC3064-100PP132C	IC1,25	Type: MOS, Qual: Commercial, Gates: 4750, Yrs: >=2.0	0.121879
MC3486	IC9,10,12-14	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.181550
MC3487	IC16,17,19,20--22	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.217860
NMC27C010Q-120	IC2	Qual: Commercial, Bits: 1, Units: Mb, Yrs: >=2.0	0.116712
MC34064P-5	IC23	Qual: Commercial, Xstrs: 50, Yrs: >=2.0	0.095144
IDT72215LB25J	IC3	Type: SRAM, Type: CMOS, Qual: Commercial, Bits: 9216, Units: b, Yrs: >=2.0	0.079345
74HC245AN	IC26-31,33-37	Type: MOS, Qual: Commercial, Gates: 18, Yrs: >=2.0	0.623491
SN74LS38N	IC32	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.039246
GAL22V10B-15LP	IC38	Type: ASTTL, Qual: Commercial, Gates: 350, Yrs: >=2.0	0.113445
IDT7133SA55J	IC3-8		0.060407
100-096-033	P1,2		0.087531
CR25130R	R8-19,20-23	Qual: Commercial, Type: Chip (RM)	0.585285
CR251M0	R1	Qual: Commercial, Type: Chip (RM)	0.036580
CR251K0	R2,35,36,39	Qual: M	0.014632
CR25300R	R24-33	Qual: Commercial, Type: Chip (RM)	0.365803
CR2510K	R3-7,37,38,47-,48	Qual: M	0.032922
CR254K7	R34		0.003658
PGM132-1A1414-V	XIC1,25		0.000001
316-AG19DC	XIC9,10,12-14-,16,17,19-22		0.000004
PCS-068A-1	XIC3-8,24		0.024530
320-AG19DC	XIC26-31,33-37		0.000004
314-AG19DC	XIC32		0.000000
324-AG10DC	XIC38		0.000000
TSW-103-07-G-S	J1-17		0.018600

Relex

Reliability Prediction
Specific Part Data

File Name: DSA Board.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 2.955715
MTBF (hrs): 338,328
Temperature: 30
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
TSW-108-07-G-S-	CN1-12,16		0.014224
TSW-106-07-G-S-	CN17,18		0.002188
UTH14X2P	CN13,14		0.002188
105-0852-001	CN15,19,24,25		0.004377
105-0853-001	CN22,23		0.002188

APPENDIX D: PCI ADAPTER VENDOR RELIABILITY PREDICTION REPORT

Standard Reliability Prediction Report

Part Number	System-001	**Description**	Top-level assembly
Reference Des	S1	**File Name**	P32F-1-3_M217GB.RPJ
Date	February 6, 2006	**Time**	1:31 PM
Environment	GB, GC - Ground Benign, Controlled	**Failure Rate**	0.000000
Temperature	25.00	**MTBF**	0

Assembly Name	Part Number	Ref Des	Qty	Failure Rate	MTBF
SAM_H	System-001	S1	1.00	0.000000	0
P32F-1-3	85851330	A1	1.00	4.941934	202,350

APPENDIX E: VME ADAPTER VENDOR RELIABILITY PREDICTION REPORT

Standard Reliability Prediction Report

Part Number	System-001	**Description**	Top-level assembly
Reference Des	S1	**File Name**	V32F-1-3_M217GB.RPJ
Date	February 6, 2006	**Time**	1:32 PM
Environment	GB, GC - Ground Benign, Controlled	**Failure Rate**	0.000000
Temperature	25.00	**MTBF**	0

Assembly Name	Part Number	Ref Des	Qty	Failure Rate	MTBF
SAM_H	System-001	S1	1.00	0.000000	0
V32F-1-3	85853635	A1	1.00	6.394119	156,394

APPENDIX F: eBIC ADAPTER RELIABILITY PREDICTION REPORT

Relex

Reliability Prediction Summary
Ethernet BIC

Failure Rate: 4.158803
MTBF (hrs): 240,454

Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Category	Ref Des	Unit Failure Rate	Quantity	Total Failure Rate
MA330011	Integrated Circuit	U1	1.125343	1	1.125343
25LC256	Integrated Circuit	U3	0.014822	1	0.014822
SR215C104KAR	Capacitor	C23, C11	0.008058	2	0.016115
RPE5C1H220J2P1Z0-3B	Capacitor	C9,C10	0.003771	2	0.007542
CFR-25JB-1M0	Resistor	R14	0.000184	1	0.000184
ATS08A	Miscellaneous	Y1	0.044043	1	0.044043
ENC28J60/SP	Integrated Circuit	U2	0.120010	1	0.120010
TAP106K010SCS	Capacitor	C5,C6	0.004484	2	0.008967
RPE5C1H330J2P1Z0-3B	Capacitor	C7,C8	0.003916	2	0.007833
CFR-25JB-180R	Resistor	R7-9	0.024423	3	0.073270
MFR-25FBF-2K32	Resistor	R5	0.004556	1	0.004556
ECS-250-18-4-F	Miscellaneous	Y2	0.057239	1	0.057239
SN74ABT541BN	Integrated Circuit	U4,5	0.274551	2	0.549103
SN74ABT541BN	Integrated Circuit	U6,7	0.274551	2	0.549103
SN74ABT541BN	Integrated Circuit	U8	0.274551	1	0.274551
SR215C104KAR	Capacitor	C12-15,18	0.008084	5	0.040421
SR215C104KAR	Capacitor	C16,17	0.008058	2	0.016115
SN74CB3T3245DBQR	Integrated Circuit	U9,10	0.074875	2	0.149751
TAP106K010SCS	Capacitor	C3,4	0.004685	2	0.009371
TAP106K010SCS	Capacitor	C1,C2	0.004484	2	0.004484
LM1086CS-3.3	Integrated Circuit	U11	0.968344	1	0.968344
5555165-1	Connection	J2	0.015165	1	0.015165
JP011821UNL	Connection	J1	0.015165	1	0.015165
MFR-25FBF-49R9	Resistor	R1-4	0.002836	4	0.011343
CFR-25JB-180R	Resistor	R10,11	0.008990	2	0.017980
MFR-25FBF-205R	Resistor	R6	0.023580	1	0.023580
4310R-101-153LF	Resistor	RN1	0.001836	1	0.001836
SR215C104KAR	Capacitor	C21	0.008217	1	0.008217
SR215C104KAR	Capacitor	C22	0.008084	1	0.008084
SR215C104KAR	Capacitor	C19,20	0.008058	2	0.016115
MI1210K600R-10	Inductor	L1	0.000149	1	0.000149

APPENDIX G: PCI-VME BUS ADAPTERS DATA SHEETS

SBS Technologies.

Model 618-3/620-3

VMEbus to PCI Adapters with DMA

I/O & COMMUNICATIONS

Features

- Bi-directional bus mastership
- Memory and I/O mapping
- Controller Mode DMA: 35 MB/s
- Slave Mode DMA: 13 MB/s
- DMA modes support Dual Port RAM
- VMEbus System Controller Mode
- Byte and word swapping functions
- Cable interface supports fiber-optic cable up to 500 meters
- IRQ1-7 and two programmable interrupts can be passed across cable
- Parity checking on address, control and data lines (PCI card)
- Data checking on the interface between cards
- 128 KB and 8 MB optional Dual Port RAM available for VME adapter card
- Loopback diagnostics for PIO transfers (618-3 only)
- Supports both 3.3V and 5.0V signalling

Model 618-3 and 620-3 bus adapters are cost-effective solutions for applications requiring VMEbus to PCI connectivity and fiber-optic capabilities. SBS bus adapters directly connect the VMEbus and PCI bus creating a virtual bus that allows the two systems to operate as one, enabling seamless operation, superior performance and the combined benefits of two diverse systems.

A standard PC or workstation can be used with the 618-3/620-3 bus adapter instead of a single board computer allowing the user to take advantage of a wealth of off-the-shelf software, the latest processor technology, and worldwide support from major PC, workstation, and operating system manufacturers. As a result, time to market and the overall development cycle are greatly reduced.

Because of their fiber-optic features, 618-3/620-3 bus adapters are ideal for environments requiring noise immunity, high-performance, electrical safety, isolation, and long-distance system separation (up to 500 meters).

The comprehensive suite of software drivers provided with 618-3 and 620-3 bus adapters minimizes integration time. In most cases, applications can be up and running in a few days. Drivers for Solaris™, IRIX™, Windows® 95, Windows® 98, Windows NT®, VxWorks®, Linux®, and HP-UX are available with these bus adapters.

Model 618-3/620-3

Model 618-3/620-3 allows you to share memory and special purpose boards between a PCI Local Bus computer and a VMEbus system. The adapter provides high-speed data transfers between systems, and requires minimal support.

Linked by the adapter, these two powerful computing environments become even more powerful and versatile. From the VMEbus side of the adapter, you can take full advantage of PCI system resources for VMEbus applications. And, because the adapter card is treated as any other processor on the VMEbus, the PCI system, acting through the adapter, can function as either a coprocessor or as the only bus master processor on the VMEbus. Consequently, the PCI system can directly control and monitor a wide variety of VMEbus cards and high-performance processors, as well as exchange interrupts with the VMEbus.

The adapter allows each bus to operate independently. The timing of the PCI bus and VMEbus is linked only when a memory or I/O reference is made to an address on one system that translates to a reference on the other. Therefore, bus bandwidth is not affected during non-transfer periods.

The adapter supports bi-directional random access bus mastering from either system and also supports 16- and 32-bit data transfers using a built-in DMA controller. The DMA controller is a high-speed data mover engine that moves data between PCI system memory and the VMEbus at sustained data transfer rates up to 35 Megabytes per second (MB/s). It also allows a VMEbus DMA device (such as a disk controller) to DMA through the adapter directly into PCI memory at data transfer rates in excess of 13 MB/s.

Communications PCI Bus ↔ VMEbus

618-3/620-3 bus adapters support two methods of intersystem communications: Memory and I/O Mapping, and Direct Memory Access (DMA).

Transparent connectivity in which the address space of the destination bus appears as additional address space to the host bus is achieved via memory and I/O mapping. Mapping takes defined address ranges of unused memory on the host bus and transposes it to selected global memory address space and I/O on the destination bus. Once the mapping is created, there is no further software overhead; adapter and system hardware handle everything.

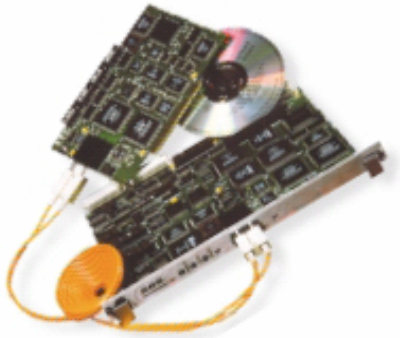
The SBS bus adapters provide bi-directional bus mastership in which address mapping is possible from both buses. Adapter memory mapping hardware allows discontiguous remote addresses to be mapped to contiguous local host addresses.

Memory mapping uses simple C language pointers to access remote resources. Any remote address space or address can be memory mapped.

DMA, the other method of communication, allows large blocks of data to be moved between the two systems at high speed with little processor overhead. The DMA engine reads data from one bus and writes data to the other bus. When the transfer is complete, the adapter interrupts the processor.

Two DMA modes are supported: Controller Mode DMA and Slave Mode DMA. Controller Mode DMA uses the adapter's DMA controller to enable high-speed transfers from one system's memory directly into the other system's memory. The local or remote processor can initiate data transfer in either direction. The DMA controller allows data transfers between PCI memory and Dual Port RAM on the VME adapter card. To achieve the best performance, VME block mode is used. A pause mode that allows other VME masters more frequent access to the VME bus during DMA is also available.

SBS Support Software, provided with the adapters, automatically engages the DMA engine for all reads or writes that are long enough to benefit from a DMA transfer.



Slave Mode DMA is the process by which a VME device uses the adapter to transfer a block of data directly into the host's memory. Slave Mode DMA transfers use the adapter's FIFOs to boost throughput to 13 MB/s. Like Controller Mode DMA, Slave Mode DMA uses very little host processing power during the transfer; the VME device actually performs the transfer and the adapter performs all host page manipulation. A programmed or VME device interrupt can be used to alert the host process when the Slave Mode DMA transfer is complete.

Because most operating systems use a memory manager, the user's buffer may be scattered across physical memory. The adapter hardware allows contiguous VME data to be transferred into the discontiguous host buffer. This feature is essential for Slave Mode DMA.

Interrupts Across the Cable

Interrupts can be passed directly between the two buses. All seven VME interrupts, IRQ1 – IRQ7, can be monitored and acknowledged from the host system. Consequently, the host system can be asynchronously notified when a VME card requires servicing and the need to poll is eliminated.

The 618-3 and 620-3 bus adapters support two programmed interrupts that can be used to communicate between host and remote processes. Adapter hardware status is monitored by an error interrupt that eliminates the need to poll the adapter for errors.

System Controller Mode Capability

In addition to VMEbus control and bus master capabilities, the adapter can provide slot 1 system controller functions. In most cases, configuring the adapter to perform system controller functions and installing it in slot 1 eliminates the need for an additional VME system controller. The adapter also allows the host to reset the VMEbus so that a system failure can be remotely reset.

In System Controller Mode, the adapter provides the VME system clock and system reset, and the bus error global timeout. The adapter card also provides four-level priority, four-level round-robin, or single-level bus arbitration.

Dual Port RAM

Up to 8 MB of optional shared memory, Dual Port RAM, can be added to the VME adapter card. Dual Port RAM does not require access to the other bus; consequently, providing system and limiting bandwidth use to only the accessing bus. Memory mapping and both DMA modes support Dual Port RAM. Arbitration is handled by the card itself.

Support Software Components

Compatible Device Drivers for:	
Pentium Platforms	Model 973 - Windows 95 & 98 Model 983 - Windows NT
HP PCI Platforms	Model 934 - HP-UX 10.20
Silicon Graphics PCI Platforms	Model 965 - IRIX 6.5
Sun Platforms	Model 946 - Solaris
Intel-based PCI Platforms	Model 993 - VxWorks Model 1003 - Linux

Example Programs Demonstrating:

- How to map remote bus and dual-port memory into an application's memory space
- Read and write functions
- Requirements for sending, receiving, and processing interrupts including those generated on the remote bus
- How applications use the device driver to process programmed and error interrupts

Tools for Installing the Device Driver

Documentation

Software Drivers

Logical devices:
Multiple adapters can be installed in a single host system. The device driver separates each physical adapter unit into several windows that are each treated as a logical device with a separate device name. One logical device is allocated to each of the following windows:

- Dual Port RAM address space
- I/O space on the remote bus
- Remote bus 24-bit memory located in the range 0x00000000 to 0x00FFFFFF
- Remote bus memory located in the range 0x00000000 to 0xFFFFFFFF
- Local system memory accessed from the remote system

DMA functions:
The device driver, for Controller Mode DMA, automatically engages the adapter's DMA engine for all reads and writes that will benefit from a DMA transfer. Slave Mode DMA transfers must be serialized through the driver.

Interrupts:
The device driver includes an interrupt handler for status error, programmed, DMA, and remote bus interrupts. Interrupt processing is controlled by interface commands that register to receive notification of an interrupt, and that allow user written remote bus interrupt handlers to be incorporated.

Interrupt call backs:
Applications can register functions that are called when error, programmed, or remote bus interrupts occur.

Atomic Instruction emulation:
Atomic Test & Set (TAS) and Atomic Compare & Swap (CAS) are emulated on the bus adapters. TAS provides an indivisible or interlocked test and set operation on either the remote bus or remote Dual Port RAM. CAS provides an indivisible or interlocked transaction on the remote bus or to remote Dual Port RAM. Both functions are useful for accessing a semaphore on the remote bus or remote Dual Port RAM, and for coordinating communication between the two systems.

Control & configuration:
Device control and configuration commands are supported. They are used to customize the device driver for your specific environment.

Model 618-3/620-3

Specifications

Model 618-3/620-3 Package Contains:
- One PCI adapter card
- One VMEbus adapter card
- Software drivers CD-ROM
- Manual

Required Components
- One short form factor PCI adapter card
- One 6U VMEbus adapter card
- A fiber-optic cable to connect adapter cards (purchased from SBS as separate item so that you can specify length and type for your application)

Power Requirements
- VMEbus adapter card draws 3.5A at 5V
- PCI adapter card draws 2.5A at 5V

VMEbus Adapter Card
- Meets IEEE 1014C specifications

PCI Adapter Card
- Meets PCI Local Bus Specification 2.0

PCI bus to VMEbus
- Accesses: A32, A24, or A16
- Data accesses: 32-, 16-, or 8-bit

VMEbus to PCI bus
- Accesses: A32
- Data accesses: 32-, 16-, or 8-bit

VMEbus to Dual Port RAM
- Accesses: A32 or A24
- Data accesses: 32-, 16-, or 8-bit
- Block Mode transfers are supported

Temperature
- Operating: 0° to 60° C
- Storage: -40° to 85° C

Humidity
- 5% to 90%, non-condensing

Configurations

Model Number	Configuration
618-3	VMEbus - PCI adapter with DMA and loopback diagnostics
618-9U	Model 618-3 adapter with VMEbus adapter card mounted in a 9U holder
620-3	VMEbus - PCI adapter with DMA
P32F-1-3	620-3 PCI card only
P32F-3	618-3 PCI card only
V32F-1-3	620-3 VME card only
V32F-3	618-3 VME card only
Dual Port RAM Options	
Model 400-202	128 Kilobytes
Model 400-206	8 Megabytes
Fiber-Optic Cable (one required)	
Model 15-103	5 meter
Model 15-101	10 meter
Model 15-102	25 meter
Model 15-104	50 meter
Model 15-105	100 meter
Custom cable available in lengths up to 500 meters	

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APPENDIX H: DETAILED SPECIFIC PART DATA

Relex

Reliability Prediction
Specific Part Data

File Name: Project 2.rfp (EBIC)
Assembly: System
Ref Des:
Description:

Failure Rate: 4.158803
MTBF (hrs): 240,454
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
MA330011	U1	Type: MOS, Qual: Commercial, Pi Q: 10.00, Word: 16 Bits, Pins: 100, Type: Flatpack, Yrs: >=2.0, OpPwr: 0.244, ThRes: 48.400, TRise: 11.8	1.125343
25LC256	U3	Type: Other, Corr: None, Qual: Commercial, Pi Q: 10.00, Bits: 256, Units: Kb, Pins: 8, Type: DIP, Glass Seal, Yrs: >=2.0, OpPwr: 0.020, ThRes: 171.002, TRise: 3.4	0.014822
SR215C104KAR	C23, C11	Qual: Commercial, Op DC: 3.30, RtVt: 50.00, V S/R: 6.6, Cap: 0.100, Units: uF	0.016115
RPE5C1H220J2P1Z03B	C9,C10	Qual: Commercial, Op DC: 0.66, RtVt: 50.00, V S/R: 1.3, Cap: 22.000, Units: pF	0.007542
CFR-25JB-1M0	R14	Qual: Commercial, OpPwr: 3.000e-006, RtPwr: 0.250, P S/R: 1.0e-003	0.000184
ATS08A	Y1	Qual: Commercial, Freq: 8.000	0.044043
ENC28J60/SP	U2	Type: MOS, Qual: Commercial, Pi Q: 10.00, Pins: 28, Type: DIP, Glass Seal, Yrs: >=2.0, OpPwr: 0.594, ThRes: 68.123, TRise: 40.5	0.120010
TAP106K010SCS	C5,C6	Qual: Commercial, Op DC: 3.30, RtVt: 10.00, V S/R: 33.0, Cap: 10.000, Units: uF, Series: >0.8	0.008967
RPE5C1H330J2P1Z03B	C7,C8	Qual: Commercial, Op DC: 3.30, RtVt: 50.00, V S/R: 6.6, Cap: 33.000, Units: pF	0.007833
CFR-25JB-180R	R7-9	Qual: Commercial, OpPwr: 0.151, RtPwr: 0.250, P S/R: 60.4	0.073270
MFR-25FBF-2K32	R5	Qual: Commercial, OpPwr: 0.010, RtPwr: 0.250, P S/R: 4.0	0.004556
ECS-250-18-4-F	Y2	Qual: Commercial, Freq: 25.000	0.057239
SN74ABT541BN	U4,5	Type: BiCMOS, Qual: Commercial, Pi Q: 10.00, Gates: 9, Pins: 20, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.054, ThRes: 28.000, Junct: Case, TRise: 1.5, TJ: 115.0	0.549103
SN74ABT541BN	U6,7	Type: BiCMOS, Qual: Commercial, Pi Q: 10.00, Gates: 9, Pins: 20, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.054, ThRes: 28.000, Junct: Case, TRise: 1.5, TJ: 115.0	0.549103
SN74ABT541BN	U8	Type: BiCMOS, Qual: Commercial, Pi Q: 10.00, Gates: 9, Pins: 20, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.035, ThRes: 28.000, Junct: Case, TRise: 1.0, TJ: 115.0	0.274551
SR215C104KAR	C12-15,18	Qual: Commercial, Op DC: 5.00, RtVt: 50.00, V S/R: 10.0, Cap: 100000.000, Units: pF	0.040421
SR215C104KAR	C16,17	Qual: Commercial, Op DC: 3.30, RtVt: 50.00, V S/R: 6.6, Cap: 100000.000, Units: pF	0.016115

Relex

Reliability Prediction
Specific Part Data

File Name: Project 2.rfp (EBIC)
Assembly: System
Ref Des:
Description:

Failure Rate: 4.158803
MTBF (hrs): 240,454
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
SN74CB3T3245DBQR	U9,10	Type: BiCMOS, Qual: Commercial, Pi Q: 10.00, Pins: 20, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 1.320e-004, ThRes: 28.000, Junct: Case, TRise: 4.0e-003, TJ: 68.0	0.149751
TAP106K010SCS	C3,4	Qual: Commercial, Op DC: 5.00, RtVt: 10.00, V S/R: 50.0, Cap: 10.000, Units: uF, Series: >0.8	0.009371
TAP106K010SCS	C2	Qual: Commercial, Op DC: 3.30, RtVt: 10.00, V S/R: 33.0, Cap: 10.000, Units: uF, Series: >0.8	0.004484
LM1086CS-3.3	U11	Qual: Commercial, Pi Q: 10.00, Pins: 3, Type: Nonhermetic: DIPs, PGA, SMT, OpPwr: 1.380, TJ: 90.6	0.968344
5555165-1	J2	Qual: Commercial, Pair: Mated Pair, Cnc Type: Telephone, Cycles: 0 to 0.05, Gauge: 20, Amps: 1, TRise: 0.6	0.015165
JP011821UNL	J1	Qual: Commercial, Pair: Mated Pair, Cnc Type: Telephone, Cycles: 0 to 0.05, Gauge: 20, Amps: 1, TRise: 0.6	0.015165
MFR-25FBF-49R9	R1-4	Qual: Commercial, OpPwr: 0.003, RtPwr: 0.250, P S/R: 1.3	0.011343
CFR-25JB-180R	R10,11	Qual: Commercial, OpPwr: 0.041, RtPwr: 0.250, P S/R: 16.2	0.017980
MFR-25FBF-205R	R6	Qual: Commercial, OpPwr: 0.146, RtPwr: 0.250, P S/R: 58.4	0.023580
4310R-101-153LF	RN1	Qual: Commercial, OpPwr: 0.003, RtPwr: 1.600, P S/R: 0.2	0.001836
SR215C104KAR	C21	Qual: Commercial, Op DC: 3.30, Op AC: 3.53, RtVt: 50.00, V S/R: 16.6, Cap: 100000.000, Units: pF	0.008217
SR215C104KAR	C22	Qual: Commercial, Op DC: 5.00, RtVt: 50.00, V S/R: 10.0, Cap: 100000.000, Units: pF	0.008084
SR215C104KAR	C19,20	Qual: Commercial, Op DC: 3.30, RtVt: 50.00, V S/R: 6.6, Cap: 100000.000, Units: pF	0.016115
MI1210K600R-10	L1	Qual: Commercial, Type: Power Filter, T Rise: 100.0, T Hot: 65.0	0.000149

Relex

Reliability Prediction
Specific Part Data

File Name: Bus Interface Controller BIC.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.444329
MTBF (hrs): 290,332
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
CK05BX102K	C1-18	Qual: Mil-Spec, Op DC: 0.00, Op AC: 4.00e-003, RtVt: 200.00, V S/R: 3.0e-003, Cap: 1000.000, Units: pF	0.028710
CK05BX102K	C20,21,28,31,-68	Qual: Mil-Spec	0.025657
CK05BX103K	C19,22,36-67	Qual: Mil-Spec, Op DC: 5.00, Op AC: 0.00, RtVt: 50.00, V S/R: 10.0, Cap: 10.000, Units: nF	0.065054
CK05BX103K	C26,27,29	Qual: Mil-Spec, Op DC: 0.00, Op AC: 0.04, RtVt: 50.00, V S/R: 0.1, Cap: 10.000, Units: nF	0.005887
M39003/01-2409	C23	Qual: Mil-Spec, Op DC: 2.50, Op AC: 0.00, RtVt: 15.00, V S/R: 16.7, Cap: 3.300, Units: uF, Series: >0.8	0.001042
M39003/01-2409	C24	Qual: Mil-Spec, Op DC: 2.97, Op AC: 0.00, RtVt: 15.00, V S/R: 19.8, Cap: 3.300, Units: uF, Series: >0.8	0.001042
CK05BX102K	C25	Qual: Mil-Spec, Op DC: 3.14, Op AC: 0.00, RtVt: 200.00, V S/R: 1.6, Cap: 1000.000, Units: pF	0.001595
CK05BX102K	C34	Qual: Mil-Spec, Op DC: 0.00, Op AC: 6.90e-005, RtVt: 200.00, V S/R: 5.0e-005, Cap: 1.000, Units: nF	0.001595
M39003/01-2409	C35	Qual: Mil-Spec, Op DC: 5.00, Op AC: 0.00, RtVt: 75.00, V S/R: 6.7, Cap: 3.300, Units: uF, Series: >0.6 to 0.8	0.001579
CM05FD221F03	C36	Qual: Mil-Spec, Op DC: 5.00, RtVt: 500.00, V S/R: 1.0, Cap: 220.000, Units: pF	0.001068
CK05BX390K	C69	Qual: Mil-Spec, Op AC: 5.00, RtVt: 200.00, V S/R: 3.5, Cap: 39.000, Units: pF	0.001191
JAN1N914	CR4	Qual: JAN, Diode: General Purpose, OpVt: 5.00, RtVt: 100.00, V S/R: 5.0, Type: Metallurgically, ThRes: 70.000, Junct: Air	0.000492
JAN1N914	CR1	Qual: JAN, Diode: General Purpose, OpVt: 0.80, RtVt: 100.00, V S/R: 0.8, Type: Metallurgically, ThRes: 70.000, Junct: Air	0.000492
JAN1N914	CR3	Qual: JAN, Diode: General Purpose, OpVt: 0.70, RtVt: 100.00, V S/R: 0.7, Type: Metallurgically, ThRes: 70.000, Junct: Air	0.000492
8T98N	U1,5,10	Qual: Commercial, Yrs: >=2.0	0.285431
SN74LS174N	U2,11,14,22,2-4,33	Type: LSTTL, Qual: Commercial, Gates: 26, Yrs: >=2.0	0.235478
SN74LS257AN	U3,6,12,13	Type: LSTTL, Qual: Commercial, Gates: 15, Yrs: >=2.0	0.156986
SN74LS280N	U4,15	Type: LSTTL, Qual: Commercial, Gates: 46, Yrs: >=2.0	0.078493
SN74LS10N	U7	Type: LSTTL, Qual: Commercial, Gates: 3, Yrs: >=2.0	0.039246
SN74LS175N	U8	Type: LSTTL, Qual: Commercial, Gates: 18, Yrs: >=2.0	0.039246
LM319AN	U9,18	Qual: Commercial, Xstrs: 22, Yrs: >=2.0	0.095144
SN7428N	U16	Type: TTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.036310

Relex

Reliability Prediction
Specific Part Data

File Name: Bus Interface Controller BIC.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.444329
MTBF (hrs): 290,332
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
SN74LS00N	U17,28,29,35	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.156986
LM311H	U19	Qual: Commercial, Xstrs: 24, Yrs: >=2.0	0.095144
316A	U20	Qual: Mil-Spec, Qty: 15	0.002842
8T26AN	U21,23,31,32,-46,47,52,55	Qual: Commercial, Yrs: >=2.0	0.761150
SN74LS74AN	U25	Type: LSTTL, Qual: Commercial, Gates: 12, Pins: 14, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.028, ThRes: 28.000, Junct: Case, TRise: 0.8	0.033755
SN74LS02N	U26,36	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.078493
SN74LS04N	U27,30,48	Type: LSTTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.117739
SN74LS132N	U34	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.039246
SN74LS08N	U37	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.039246
MC3487P	U38,44,50,54,-58,62	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.217860
MC3486P	U40,45,49,53,-57,61	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.217860
LM339AN	U41	Qual: Commercial, Xstrs: 56, Yrs: >=2.0	0.095144
SN74LS38N	U42,43	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.078493
316A	U51	Qual: Mil-Spec, Qty: 10	0.001895
SN74LS266N	U56,59,60	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.117739
RCR07G131JS	R1-18	Qual: S, OpPwr: 0.192, RtPwr: 0.300, P S/R: 64.0	0.000961
RN55D1002F	R19,28	Qual: Mil-Spec, OpPwr: 0.002, RtPwr: 0.125, P S/R: 1.4, Type: High Stability (RN, RNR)	0.001361
RN55D5902F	R20	Qual: Mil-Spec, OpPwr: 0.010, RtPwr: 0.125, P S/R: 8.3, Type: High Stability (RN, RNR)	0.001455
RN55D4021F	R21	Qual: Mil-Spec, OpPwr: 0.004, RtPwr: 0.125, P S/R: 3.2, Type: High Stability (RN, RNR)	0.000948
RN55D4021F	R33	Qual: Mil-Spec, OpPwr: 0.001, RtPwr: 0.125, P S/R: 0.8, Type: High Stability (RN, RNR)	0.000538
RCR07G472JS	R22,37,30,34	Qual: S	0.000265
RN55D1962F	R23	Qual: Mil-Spec, OpPwr: 0.027, RtPwr: 0.125, P S/R: 21.3, Type: High Stability (RN, RNR)	0.002421
RN55D1001F	R24,32	Qual: Mil-Spec, OpPwr: 0.001, RtPwr: 0.125, P S/R: 1.0, Type: High Stability (RN, RNR)	0.001194

Relex

Reliability Prediction
Specific Part Data

File Name: Bus Interface Controller BIC.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.444329
MTBF (hrs): 290,332
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
RN55D1001F	R69	Qual: Mil-Spec, OpPwr: 0.014, RtPwr: 0.125, P S/R: 11.2, Type: High Stability (RN, RNR)	0.001687
RN55D1001F	R70	Qual: Mil-Spec, OpPwr: 0.007, RtPwr: 0.125, P S/R: 5.4, Type: High Stability (RN, RNR)	0.001191
RCR07G101JS	R25,26	Qual: S	0.000133
RN55D3652F	R29	Qual: Mil-Spec, OpPwr: 0.007, RtPwr: 0.125, P S/R: 5.4, Type: High Stability (RN, RNR)	0.001194
RN55D1212F	R31	Qual: Mil-Spec, OpPwr: 0.016, RtPwr: 0.125, P S/R: 12.8, Type: High Stability (RN, RNR)	0.001809
RCR07G102JS	R36,47,50,54,-64,66,68,71,84	Qual: S	0.000596
RCR07G221JS	R67,83	Qual: S	0.000133
RCR07G333JS	R44,85	Qual: S, OpPwr: 1.900e-004, RtPwr: 0.250, P S/R: 8.0e-002	0.000002
RN55D1052F	R45,46	Qual: Mil-Spec, OpPwr: 3.300e-004, RtPwr: 0.125, P S/R: 0.3, Type: High Stability (RN, RNR)	0.000347
RN55D1542F	R48	Qual: Mil-Spec, OpPwr: 5.740e-004, RtPwr: 0.125, P S/R: 0.5, Type: High Stability (RN, RNR)	0.000431
RN55D1782F	R49	Qual: Mil-Spec, OpPwr: 5.500e-004, RtPwr: 0.125, P S/R: 0.4, Type: High Stability (RN, RNR)	0.000424
RCR07G330JS	R51	Qual: S, OpPwr: 3.100e-005, RtPwr: 0.250, P S/R: 1.0e-002	0.000000
RCR07G100JS	R52,81	Qual: S, OpPwr: 1.000e-004, RtPwr: 0.250, P S/R: 4.0e-002	0.000002
RCR07G152JS	R57-59	Qual: S	0.000199
RN55C2740F	R60,61	Qual: Mil-Spec, OpPwr: 0.033, RtPwr: 0.100, P S/R: 33.0, Type: High Stability (RN, RNR)	0.005991
RN55D8660F	R62	Qual: Mil-Spec, OpPwr: 0.007, RtPwr: 0.125, P S/R: 5.4, Type: High Stability (RN, RNR)	0.001187
RN55C3320F	R63	Qual: Mil-Spec, OpPwr: 0.005, RtPwr: 0.100, P S/R: 4.7, Type: High Stability (RN, RNR)	0.001026
RCR07G332JS	R79	Qual: S	0.000066
RCR07G471JS	R80	Qual: S	0.000066
RCR07G331JS	R82	Qual: S, OpPwr: 6.140e-006, RtPwr: 0.250, P S/R: 2.0e-003	0.000000
RCR07G472JS	R78	Qual: S, OpPwr: 0.005, RtPwr: 0.250, P S/R: 2.1	0.000004
RCR07G102JS	R77	Qual: S, OpPwr: 1.000e-005, RtPwr: 0.250, P S/R: 4.0e-003	0.000000
RCR07G221JS	R74,40,37,43,-53	Qual: S, OpPwr: 1.000e-004, RtPwr: 0.250, P S/R: 4.0e-002	0.000003

Relex

Reliability Prediction
Specific Part Data

File Name: Bus Interface Controller BIC.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.444329
MTBF (hrs): 290,332
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
RCR07G221JS	R76,42,56	Qual: S, OpPwr: 9.200e-006, RtPwr: 0.250, P S/R: 4.0e-003	0.000001
RCR07G221JS	R35,39	Qual: S, OpPwr: 0.113, RtPwr: 0.250, P S/R: 45.2	0.000059
RCR07G131JS	R75	Qual: S, OpPwr: 0.089, RtPwr: 0.300, P S/R: 29.8	0.000020
RCR07G131JS	R38,41,55	Qual: S	0.000199
182154	P1-3	Qual: Commercial	0.262593

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Reliability Prediction
Specific Part Data

File Name: IO Buffer.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 3.396088
MTBF (hrs): 294,456
Temperature: 25
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
CK05BX103K	C2-C10	Qual: Mil-Spec, Op DC: 5.00, RtVt: 100.00, V S/R: 5.0, Cap: 10.000, Units: nF	0.001963
M39003/01-2409	C1	Qual: Mil-Spec, Op DC: 5.00, RtVt: 75.00, V S/R: 6.7, Cap: 3.300, Units: uF, Series: >0.8	0.001042
SN74LS14N	U1	Type: LSTTL, Qual: Commercial, Pi Q: 10.00, Gates: 6, Pins: 14, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.064, ThRes: 28.000, Junct: Case, TRise: 1.8	0.033934
SN75175N	U4-U7,U14-U-19	Qual: Commercial, Pi Q: 10.00, Pins: 16, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.150, ThRes: 100.000, Junct: Air, TRise: 15.0	0.695901
SN75LS113	U9-U13,U19--U25	Qual: Commercial, Pi Q: 10.00, Pins: 16, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.400, ThRes: 100.000, Junct: Air, TRise: 40.0	2.359261
SN7437N	U8	Type: TTL, Qual: Commercial, Pi Q: 10.00, Gates: 4, Pins: 14, Type: Nonhermetic: DIPs, PGA, SMT, Yrs: >=2.0, OpPwr: 0.077, ThRes: 28.000, Junct: Case, TRise: 2.2	0.033926
RCR07G153JS	U2,U3	Qual: Mil-Spec, OpPwr: 0.002, RtPwr: 0.250, P S/R: 0.7	0.000941
RCR07G150JS	R2-R5,R16-R-32	Qual: S, OpPwr: 0.167, RtPwr: 0.250, P S/R: 66.8	0.001124
RCR07G102JS	R1,R14	Qual: S, OpPwr: 0.018, RtPwr: 0.250, P S/R: 7.4	0.000007
RCR07G221JS	R7-8,R11-12,-R33.R35	Qual: S, OpPwr: 0.011, RtPwr: 0.250, P S/R: 4.6	0.000032
RN55C3740F	R13	Qual: Mil-Spec, OpPwr: 0.022, RtPwr: 0.100, P S/R: 22.3, Type: High Stability (RN, RNR)	0.002285
RCR07G681JS	R9-10,R34	Qual: Mil-Spec, OpPwr: 0.037, RtPwr: 0.250, P S/R: 14.7	0.003076
RCR07G153JS	R6	Qual: S, OpPwr: 0.002, RtPwr: 0.250, P S/R: 0.7	0.000002
182154	P1-3	Qual: Commercial	0.262593

Relex

Reliability Prediction
Specific Part Data

File Name: DSA Board.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 2.955715
MTBF (hrs): 338,328
Temperature: 30
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
681-10339	C1,2	Qual: C, T	0.000034
CZ20C104M	C3-52	Qual: Mil-Spec	0.076353
A-10.000000-18	X1		0.031967
5309K1	D1		0.003565
XC3064-100PP132C	IC1,25	Type: MOS, Qual: Commercial, Gates: 4750, Yrs: >=2.0	0.121879
MC3486	IC9,10,12-14	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.181550
MC3487	IC16,17,19,20--22	Type: TTL, Qual: Commercial, Gates: 6, Yrs: >=2.0	0.217860
NMC27C010Q-120	IC2	Qual: Commercial, Bits: 1, Units: Mb, Yrs: >=2.0	0.116712
MC34064P-5	IC23	Qual: Commercial, Xstrs: 50, Yrs: >=2.0	0.095144
IDT72215LB25J	IC3	Type: SRAM, Type: CMOS, Qual: Commercial, Bits: 9216, Units: b, Yrs: >=2.0	0.079345
74HC245AN	IC26-31,33-37	Type: MOS, Qual: Commercial, Gates: 18, Yrs: >=2.0	0.623491
SN74LS38N	IC32	Type: LSTTL, Qual: Commercial, Gates: 4, Yrs: >=2.0	0.039246
GAL22V10B-15LP	IC38	Type: ASTTL, Qual: Commercial, Gates: 350, Yrs: >=2.0	0.113445
IDT7133SA55J	IC3-8		0.060407
100-096-033	P1,2		0.087531
CR25130R	R8-19,20-23	Qual: Commercial, Type: Chip (RM)	0.585285
CR251M0	R1	Qual: Commercial, Type: Chip (RM)	0.036580
CR251K0	R2,35,36,39	Qual: M	0.014632
CR25300R	R24-33	Qual: Commercial, Type: Chip (RM)	0.365803
CR2510K	R3-7,37,38,47-,48	Qual: M	0.032922
CR254K7	R34		0.003658
PGM132-1A1414-V	XIC1,25		0.000001
316-AG19DC	XIC9,10,12-14-,16,17,19-22		0.000004
PCS-068A-1	XIC3-8,24		0.024530
320-AG19DC	XIC26-31,33-37		0.000004
314-AG19DC	XIC32		0.000000
324-AG10DC	XIC38		0.000000
TSW-103-07-G-S	J1-17		0.018600

Relex

Reliability Prediction
Specific Part Data

File Name: DSA Board.rfp
Assembly: System
Ref Des:
Description:

Failure Rate: 2.955715
MTBF (hrs): 338,328
Temperature: 30
Environment: GB, GC - Ground Benign, Controlled

Part Number	Reference Designator	Specific Part Data	Failure Rate
TSW-108-07-G-S-	CN1-12,16		0.014224
TSW-106-07-G-S-	CN17,18		0.002188
UTH14X2P	CN13,14		0.002188
105-0852-001	CN15,19,24,25		0.004377
105-0853-001	CN22,23		0.002188